

MONOLITHIC PROGRAMMABLE STATE-VARIABLE BIQUADRATIC OTA-CAPACITOR (TAC) FILTERS

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ABSTRACT

A continuous-time filter structure derived from the KHN active-RC state-variable filter using Operational Transconductance Amplifiers and Capacitors (TAC) is presented. The filter has simultaneously a highpass output, a bandpass output, and a lowpass output. The parameters ω_o , Q and peak voltage gains can be independently programmed. All of the OTA have a grounded input which makes a conversion to a fully-differential version possible. Design considerations for a fully monolithic implementation of this circuit are discussed.

I. INTRODUCTION

State-Variable realizations of biquadratic transfer functions using resistors, capacitors and operational amplifiers are popular [1]-[3]. They are easy to tune, the bandpass bandwidth, ω_o/Q , and the pole frequency, ω_o , can be independently controlled. The passive ω_o and Q sensitivities are low. Another attractive property of the three-op amp biquads is their ability to provide the basic lowpass, bandpass and highpass filtering functions at different outputs in the same circuit.

We present an alternative to using the conventional op amp based active-RC approach for implementing the state-variable biquad based upon operational transconductance amplifiers (OTAs) and capacitors. The proposed approach can be used for either discrete or monolithic implementations. The OTA based approach offers some advantages in programmable, high frequency and monolithic applications [4].

The proposed OTA-Capacitor (TAC) structure has six OTAs and two capacitors. The highpass, bandpass and lowpass outputs are simultaneously available. Each of the six OTAs has a grounded input making a fully-differential version of the filter possible. Furthermore, due to the nature of the structure and the external controllability of the OTA transconductances, the filter can be easily electronically programmed.

II. FILTER BLOCK DIAGRAM AND CIRCUIT BLOCKS

The development of the filter block diagram follows the conventional "analog computer" approach. Consider a second-order highpass transfer function expressed in the form

$$V_{OH} = -\frac{1}{Q} \frac{V_{OH}}{(s/\omega_o)} - \frac{V_{OH}}{(s/\omega_o)^2} + KV_{in} \quad (1)$$

A block diagram of a structure which implements this transfer function is shown in Fig. 1 where the characteristic equation, $D(s)$, is given by

$$D(s) = s^2 + A_1 K_2 s + A_o K_1 K_2 \quad (2)$$

From (2) it follows that ω_o and Q satisfy the expressions

$$\frac{\omega_o}{Q} = A_1 K_2 \quad \text{and} \quad \omega_o^2 = K_1 K_2 A_o \quad (3)$$

In addition to implementing the highpass function of (1) at the node labeled V_{OH} in Fig. 1, it can be observed that the lowpass and bandpass outputs are also available at the nodes labeled V_{OL} and V_{OB} . This block diagram can be used to characterize the state-variable KHN filter structure and hence the circuit that follows which is synthesized from this block diagram will be termed a state-variable filter.

From the block diagram of Fig. 1, it can be observed that only two circuit building blocks are needed. These are a multiple-input summer and an inverting integrator. The summer must implement the expression

$$V_{OH} = +A_1 V_{OB} - A_o V_{OL} + K V_{in} \quad (4)$$

The OTA based summer circuit of Fig. 2 can be used to implement the summing function. For this circuit

$$A_1 = \frac{g_{a1}}{g_{m_r}}, \quad A_o = \frac{g_{a_o}}{g_{m_r}}, \quad K = \frac{g_K}{g_{m_r}} \quad (5)$$

The implementation of a simple OTA based inverting integrator is shown in Fig. 3. The transfer function is given by

$$\frac{V_2}{V_1} = \frac{-g_m}{sC} \quad (6)$$

The sign of g_m can be changed by simply interchanging the $-$ and $+$ terminals of the OTA.

III STATE-VARIABLE TAC FILTER STRUCTURE

A circuit realization of the block diagram of Fig. 1 based upon the OTA summer and integrator of Figs. 2 and 3 is shown in Fig. 4. The corresponding transfer functions for each of the outputs are

$$T_{HP}(s) = \frac{V_{OH}}{V_{in}} = \frac{s^2 g_K / g_{m_r}}{D(s)} \quad (7)$$

$$T_{BP}(s) = \frac{V_{OB}}{V_i} = \frac{-s g_K g_{m_2} / (g_{m_r} C_2)}{D(s)} \quad (8)$$

$$T_{LP}(s) = \frac{V_{OL}}{V_i} = \frac{g_K g_{m_1} g_{m_2} / (g_{m_r} C_1 C_2)}{D(s)} \quad (9)$$

where

$$D(s) = s^2 + \frac{g_{m_2} g_{a1}}{C_2 g_{m_r}} s + \frac{g_{a_o} g_{m_1} g_{m_2}}{g_{m_r} C_1 C_2} \quad (10)$$

$$\omega_o = \left\{ \frac{g_{a_o} g_{m_1} g_{m_2}}{g_{m_r} C_1 C_2} \right\}^{\frac{1}{2}} \quad \text{and} \quad Q = \frac{1}{g_{a1}} \left\{ \frac{g_{a_o} g_{m_1} g_{m_r} C_2}{g_{m_2} C_1} \right\}^{\frac{1}{2}} \quad (11)$$

A simple set of design equations is obtained when $g_{m_1} = g_{m_2} = g_{a_o} = g_{m_r} = g_m$ and $C_1 = C_2 = C$. In this case (11) simplifies to

$$\omega_o = \frac{g_m}{C} \quad \text{and} \quad Q = \frac{g_m}{g_{a1}} \quad (12)$$

The scale factor can be expressed as $K = g_K / g_m$.

A tuning sequence useful for discrete implementations of this circuit follows:

- i) Adjust g_m so the bandpass output peaks at the desired $\omega = \omega_o$. Simultaneous g_m adjustment is readily achievable in many published OTA circuits by simultaneously adjusting the tail current of the differential input stages with a multiple-output current mirror. This tuning step will set the ω_o of the poles to the desired value.
- ii) The Q can be adjusted by setting the input frequency to

$$\omega = \omega_o \sqrt{1 + \frac{1}{2Q^2} \pm \sqrt{\frac{1}{Q^2} + \frac{1}{4Q^4}}} \approx \omega_o (1 \pm \frac{1}{2Q}) \quad (13)$$

and then adjusting g_{a1} so that the bandpass output, V_{OB} , becomes $|V_{OB}(\omega_o)|/\sqrt{2}$ where $V_{OB}(\omega_o)$ is the peak value of the bandpass output established at Step i.

- iii) g_K determines the peak gain voltage. Thus by adjusting g_K the desired voltage gain at $\omega = \omega_o$ can be obtained. It should be noted that the adjustment of g_{a1} in Step ii) has no effect on ω_o . Also note that adjustment of g_K in Step iii) has no effect on ω_o nor on the bandwidth.

IV. A FULLY DIFFERENTIAL STATE-VARIABLE TAC FILTER

Unlike op amp based active filters, the transfer characteristic of the TAC filter of Fig. 4 is directly dependent upon the gain of the amplifier, g_m . This direct dependence dictates designing OTAs which have good linearity to maintain good signal swings and dynamic range in the TAC filters. Considerable effort has been expended in linearizing the gain of the OTAs in recent years [5], [6].

One method of improving the linearity of TAC filters through the use of fully differential transconductance amplifiers and filter structures will be considered here. The advantages of fully-differential filters have been discussed elsewhere including [7], [8]. A fully differential version of the TAC state-variable biquad derived from the circuit of Fig. 4 appears in Fig. 5.

The design of fully differential OTAs will now be considered. A fully differential source-coupled pair is shown in Fig. 6. This differs from the standard source-coupled pair in the way the common source node is terminated. In the circuit of Fig. 6, the sources are terminated in a dc voltage source, V_{ee} , rather than in a high impedance dc tail current source. Although common-mode input range and CMRR are sacrificed with this structure, improvements in linearity are obtained with this approach. The degradation of common-mode input range and CMRR can be tolerated since the structure will be used in a fully differential circuit. The linearity characteristics of this input stage will now be investigated. If both devices are assumed operating in the saturation region and modeled by the Sah equation one obtains

$$I_1 = \beta(V_1 - V_{ee} - V_t)^2 \quad (14a)$$

$$I_2 = \beta(V_2 - V_{ee} - V_t)^2 \quad (14b)$$

where $\beta = \frac{1}{2} \mu C_{ox} \frac{W}{L}$ and V_t is the zero bias threshold voltage. The differential output current is:

$$I_{out} = I_2 - I_1 = \beta[(V_2^2 - V_1^2) - 2(V_t + V_{ee})(V_2 - V_1)] \quad (15)$$

For purely differential input signals ($V_1 = -V_2$), the output expression simplifies to:

$$I_{out} = 4\beta(V_t + V_{ee})V_1 \quad (16)$$

The differential output current is a purely linear function of the input voltage, given that Sah's equation is an accurate model of the MOSFET large signal behavior. This is in contrast to the linearity degradation which occurs in the tail current biasing scheme due to signal modulation of the common source voltage.

The block diagram of an OTA based upon the fully differential input stage of Fig. 6 is shown in Fig. 7. One of the advantages of OTAs is their topological and structural simplicity. A second advantage of the OTA is the improved performance at high frequencies which can be primarily attributed to the absence of any internal high impedance nodes in the OTA itself.

Flexibility in the choice of the current mirrors still exists. Tradeoffs between output impedance, bandwidth, area and signal swing must be made when selecting a mirror structure

and sizing the devices in the mirror. An implementation of the fully differential OTA is shown in Fig. 8. Stacked current mirrors are used to provide large output resistance. The p-channel mirrors are enhanced Wilson mirrors for maximum current gain bandwidth and linearity, and the n-channel mirrors are cascode mirrors for accurate current matching. The devices along the V_{SS} rail are included to provide common mode bias feedback [7].

SPICE level 2 simulations show less than .45% full scale error in I_{out} for a $4 V_{p-p}$ input range. Percent full scale error is the percentage difference between the measured output current and a linear regression fit of the output divided by the output current for a full scale input. This OTA was fabricated in a 3μ p-well CMOS process. Fig. 9 shows the measured nonlinearity. Due to random statistical mismatches between nominally matched devices the fabricated OTA shows slightly more nonlinearity than the SPICE simulations. The fabricated OTA shows less than .85% full scale error for a $4 V_{p-p}$ input range. The fully balanced filter of Fig. 5 is currently under fabrication in a 3μ CMOS process. The circuit has been designed for a nominal $f_o = 1$ MHz and $Q = 3$. Experimental results will be presented in the near future.

V. CONSIDERATIONS FOR MONOLITHIC IMPLEMENTATION

An exact realization of the biquadratic transfer functions of (7-9) requires OTAs which behave as ideal voltage controlled current sources. Finite output resistance, excess phase from high frequency singularities, and parasitic capacitance must be considered, as they will limit the range of applications and/or require compensation.

The primary complication caused by finite output resistance in a state-variable OTA-based filter is the coupling between transfer function coefficients. A transconductance variation which ideally influences only one filter parameter (ω_o , Q , or H_{max}) will also affect other filter parameters as well. This places a design constraint on the OTA, that the OTA output resistance should be much larger than the other impedances in the filter, including those of both resistor-connected OTAs and load capacitors (at signal frequencies). The use of stacked mirrors in the OTA output with appropriate consideration to maintaining high output resistance is useful for minimizing these effects.

The OTA integrator of Fig. 3 will ideally exhibit exactly 90° phase shift. However, high frequency parasitic poles from the subcircuits used to compose the OTA will cause the integrator phase to exceed its nominal value at high frequencies. Since very small amounts of excess phase ($< 1^\circ$) cause serious deviations in filter performance, some form of compensation is required to operate at high frequencies. One technique which can be used to compensate for the excess phase is the addition of a MOSFET in series with the load capacitor. This ohmic device will add a left half plane zero to the integrator transfer function with its position adjustable by the applied gate voltage, allowing first-order cancellation of the excess phase at the filter critical frequency.

Parasitic capacitors will influence the design in at least two ways. The integrated capacitors (C_1 and C_2) should be adjusted to compensate for the loading by OTA input / output capacitances, interconnect parasitics and buffer input capacitances. Second, the V_{OH} output node in Fig. 4 is not loaded by a specific design capacitor like the other two nodes, but will be subject to loading by several parasitic capacitances. The V_{OH} node capacitance, designated C_P , is due to the output capacitance of four OTAs, the input capacitance of one OTA, the interconnect capacitance present in the layout, and the load from a buffer used to drive the output signal off-chip. C_P may become a sizable capacitance that can cause excess phase shift or even instability by introduction of a third pole to the open loop transfer function below the frequency of the zero caused by the multiple feedback paths. Calculating the filter transfer function including the parasitic (assumed linear) C_P capacitance and subsequent application of the Routh-Hurwitz stability test shows that the limiting value of C_P for stability is

$$C_P(\text{limit}) = C_1 \frac{g_m r_{a1}}{g_{a0} g_{m1}} \quad (17)$$

When the equal g_m , equal C design summarized by (12) is used, the limiting value of $C_P(\text{limit}) = C_1/Q$. This stability requirement will restrict implementations to moderate Q values and reasonably large C_1 . The excess phase introduced by C_P in stable filters can be compensated using the phase compensation scheme outlined earlier. Proper layout and OTA design (to minimize the output capacitance) will allow implementation of moderate Q filters without excessive C_1 values.

VI. CONCLUSIONS

A circuit topology of a second-order TAC filter which simultaneously implements a low-pass, bandpass, and highpass function has been reported. Both single-ended and fully differential versions of this circuit were presented. Design considerations for realizing a monolithic version were discussed. Theoretical and experimental performance of a fully differential transconductance amplifier which can be used in the fully differential state-variable TAC filter was reported.

REFERENCES

- [1] W.J. Kerwin, et.al, "State-Variable Synthesis for Insensitive Integrated Circuit Transfer Functions", *IEEE J. Solid-State Circuits*, SC-2, pp. 87-92, Sept. 1967.
- [2] D. Åkerberġ and K. Mossberg, "A Versatile Active RC Building Block with Inherent Compensation for the Finite Bandwidth of the Amplifier", *IEEE Trans. Circuit Theory*, CAS-21, pp. 75-78, Jan. 1974.
- [3] A. Sedra and P. Brackett, *Filter Theory and Design: Active and Passive*, Portland, Matrix Publishers, 1978.
- [4] R. Geiger and E. Sánchez-Sinencio, "Active Filter Design Using Operational Transconductance Amplifiers; A Tutorial", *IEEE Circuits and Devices Mag.*, 1, pp. 20-32, March 1985.
- [5] A. Nedungadi and T. Viswanathan, "Design of Linear CMOS Transconductance Elements". *IEEE Trans. on Circuits and Systems*, CAS-31, pp. 891-894, Oct. 1984.
- [6] E. Seevinck and R. Wassenaar, "A Versatile CMOS Linear Transconductor / Square-Law Function Circuit," *IEEE J. Solid-State Circuits*, SC-22, pp. 366-377, June 1987. Improved Linearity", *Proc. 27th Midwest Symposium on Circuits and Systems*, pp. 63-66, June 1984.
- [7] D. Senderowicz, et.al, "A Family of Differential NMOS Analog Circuits for a PCM Codec Filter Chip", *IEEE J. Solid-State Circuits*, SC-17, pp. 1014-1023, Dec. 1982.
- [8] K. Hsieh, et.al., "A Low-Noise Chopper-Stabilized Differential Switched Capacitor Filter Technique", *IEEE J. Solid-State Circuits*, SC-16, pp. 708-715, Dec. 1981.

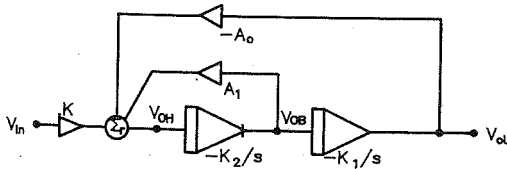


Fig. 1 Block Diagram Representation of High-Pass Filter.

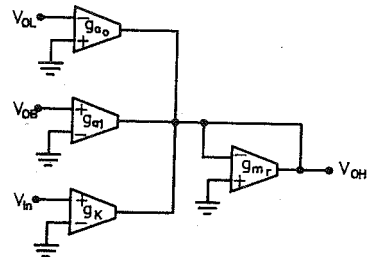


Fig. 2 A Multiple-Input OTA-Based Summer

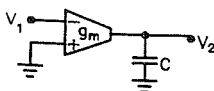


Fig. 3 An OTA-Based Lossless Integrator

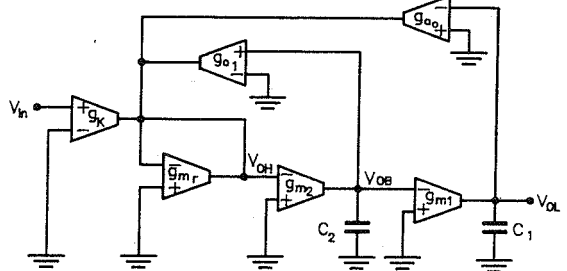


Fig. 4 A Single-Ended State Variable Filter.

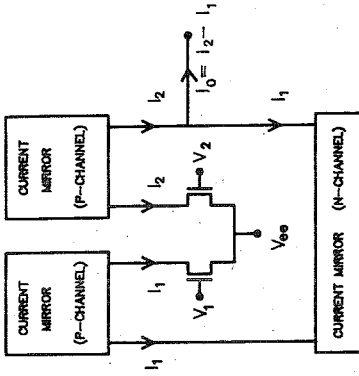


Fig. 7 Fully Differential OTA Block Diagram

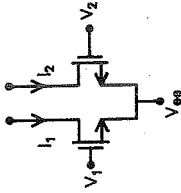


Fig. 6 Fully Differential Input Stage

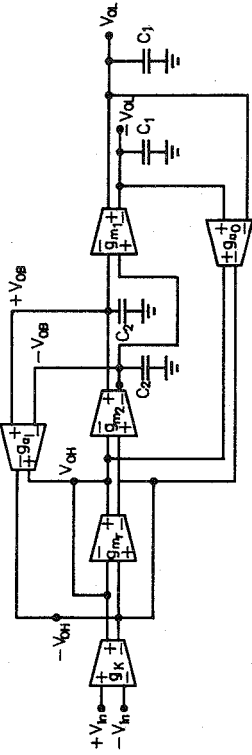


Fig. 5 Fully-Differential State Variable Filter.

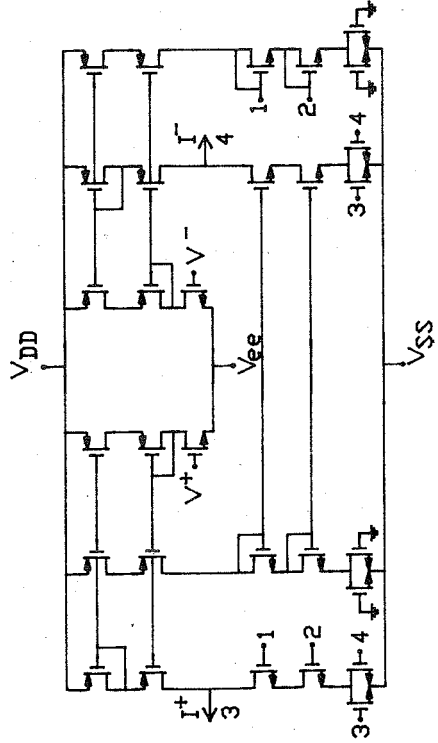


Fig. 8 Fully Differential CMOS OTA Schematic

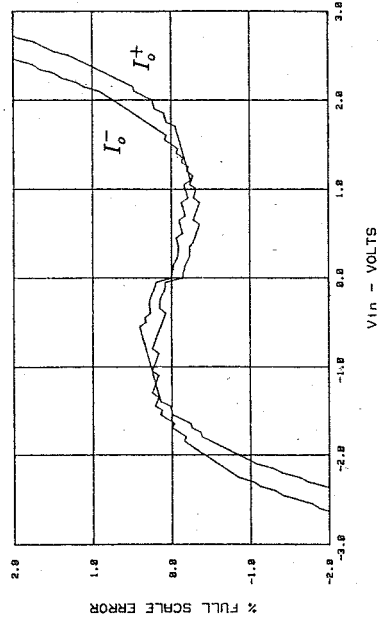


Fig. 9 Measured Nonlinearity For Fully Differential OTA.