A RECONFIGURABLE BIQUADRATIC BUILDING BLOCK FOR DIGITALLY-CONTROLLED CONTINUOUS-TIME SIGNAL PROCESSING

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Abstract

A reconfigurable biquadratic continuous-time building block suitable for applications in digitally-controlled analog signal processing systems is presented.† Using linearized CMOS transconductance elements, digital-analog converters and associated digital logic, the biquad has the potential of being tuned over a three decade frequency range between 2 kHz and 2 MHz with Qs as high as 50. Details of the biquad implementation are presented along with experimental results obtained from a fabricated circuit.

Introduction

Recently, a design methodology for precision high-frequency monolithic continous-time signal processing has been introduced[1]. Termed Digitally Controlled Analog Signal Processing (DCASP), the approach employs an intelligent digital controller to precisely control a continuous-time signal processing block. The resulting processor is inherently insensitive to fabrication process variations, component matching, temperature variations, aging, and circuit parasitics, and can potentially be used to implement in-field self-testing and/or correcting algorithms.

Crucial to the realization of the DCASP approach, is the implementation of a continuous-time Controlled-Signal Processor (CSP)[1] which allows for digital control of a number of key transfer-function parameters. The structure adopted here is a cascade of biquadratic building blocks (biquads)[2], which is connected to common digital and analog busses. Each biquad block is digitally controllable and addressable, and its inputs and outputs are connected to common excitation/response busses through appropriate digital control signals and MOS analog switches. This structure allows for control algorithms which tune each biquad separately, in combination, or which functionally tune the entire cascade. The following paper discusses the design considerations involved in realizing a reconfigurable biquadratic (biquad) building block for DCASP applications, and presents preliminary experimental results.

Basic Biquad Architecture

Fig. 1 shows the the overall circuit configuration of the reconfigurable biquad building block. It basically employs five operational transconductance amplifiers (OTAs) g_{m1}–g_{m5}, two integrating capacitors C_6, C_7, and several analog switches that configure the topology of the network and determine the form of the realized transfer-function. A unity gain voltage buffer is included to enable the circuit to drive succeeding stages and off-chip loads. The basic circuit is essentially a two-integrator-loop OTA based filter[3] which ideally implements the general biquadratic transfer function

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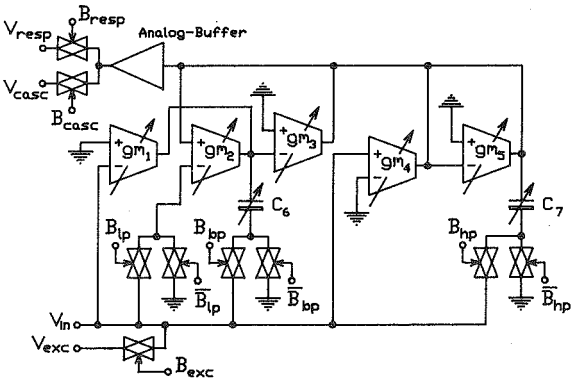

Fig. 1. Biquad block diagram.

$$\frac{V_{out}}{V_{in}} = \frac{B_{hp}s^2 + \frac{g_{m4}-g_{m3}B_{bp}}{C_7}s + a_o}{s^2 + (\frac{g_{m5}}{C_7})s + (\frac{g_{m2}g_{m3}}{C_6C_7})} \qquad (1a)$$

$$a_o = \frac{g_{m1}g_{m3} + g_{m2}g_{m3}B_{lp}}{C_6C_7} \qquad (1b)$$

Here, B_{lp}, B_{bp} and B_{hp} are digital control bits that have values of either 0 or 1, depending on the actual transfer function to be realized. These bits form part of a 6-bit digital control word stored in a latch not shown. The remaining three bits, B_{exc}, B_{resp}, B_{casc} determine how this biquad will be connected to other biquads and input and output ports in the overall CSP system.

The various transfer functions realizable with the circuit of Fig. 1 are listed in Table 1, along with the required combinations for the control bits and transconductance values for each case. Once the biquad configuation has been set and the filter transfer function chosen, the individual transconductance values g_{m1}–g_{m5} and capacitors C_1 and C_2 are digitally programmed. Transconductance adjustment is achieved through the use of digitally controlled transconductance amplifiers (CTAs), while programmable capacitance arrays allow adjusment of C_1 and C_2. The design and implementation of these digitally controllable blocks are discussed next.

Table 1. Biquad settings for common transfer functions.

	B_{hp}	B_{bp}	B_{lp}	Special Conditions
Highpass (HP)	1	0	0	$g_{m1} = g_{m4} = 0$
Bandpass (BP)	0	0 or 1	0	$g_{m1} = 0$
Lowpass (LP)	0	0	0 or 1	$g_{m4} = 0$
Allpass (AP)	1	1	1	$g_{m1} = g_{m4} = 0$ $g_{m3} = g_{m5}$
Lowpass Notch (LPN)	1	0	1	$g_{m4} = 0$ $g_{m1} > g_{m2}$
Highpass Notch (HPN)	1	0	0	$g_{m4} = 0$ $g_{m1} < g_{m2}$

between ω_{o0} and ω_{oN}, N capacitors are required. For the present design, a tuning range of one decade ($\omega_{o0} = 10\omega_{oN}$) and $N = 20$ were chosen. This requires an array of 20 capacitors, each given by $\hat{C}_i = \hat{C}_0(1.13)^i$, $i = 0, \ldots, 19$.

The implementation of uniformly spaced component values on a linear axis using binarily weighted component values is widely used. Since the structures used here are intended to be programmable over a wide range of frequencies, uniform spacing of component values on the logarithmic axis was adopted. This logarithmic spacing requirement complicates the implementation. A direct implementation of the geometric weighting scheme given above would require excessive silicon area due to the geometric increase in capacitor values required. This problem is alleviated by realizing only the incremental capacitances C_i where $C_0 = \hat{C}_0$ and $C_i = \hat{C}_i - \hat{C}_{i-1}$, and switching these in one by one in parallel. By doing this, the total capacitance and the corresponding area required are reduced.

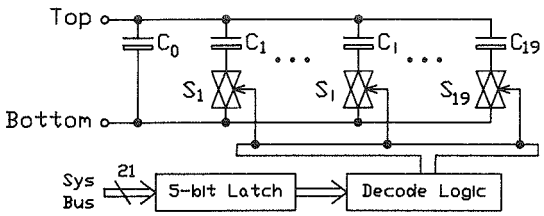

Fig. 4. Capacitor array block diagram.

A block diagram of the programmable capacitor array is shown in Fig. 4. The array is programmed with a 5-bit digital control word which is stored in a latch and decoded by requisite predecode and decode logic. The resulting control bits drive 19 analog switches in a manner such that, for the Mth state, the first M switches are closed while the remaining switches are open. This provides a total capacitance in the Mth state given by

$$C_M = C_0 + \sum_{i=1}^{M} C_i, \quad M = 0, \ldots, 19 \tag{2}$$

Note that the minimum obtainable capacitance value is C_0 which, along with the maximum transconductance, determines the upper frequency limit of the realizable poles and zeros in the filter. For the present design a design value of $C_0 = 2.39\ pF$ was used, giving an ideal upper limit of approximately 3 MHz.

Tuneable Range of Frequency and Bandwidth

Equation (1) may be written in terms of the pole and zero frequencies ω_z ω_p and bandwidths BW_p and BW_z as

$$\frac{V_{out}}{V_{in}} = \frac{B_{hp}s^2 + BW_z s + \omega_z^2}{s^2 + BW_p s + \omega_p^2} \tag{3a}$$

$$\omega_p = \sqrt{\frac{g_{m2}g_{m3}}{C_6C_7}}, \quad \omega_z = \sqrt{\frac{g_{m1}g_{m3} + g_{m2}g_{m3}B_{lp}}{C_6C_7}}$$
$$BW_p = \frac{g_{m5}}{C_7}, \quad BW_z = \frac{g_{m4} - g_{m3}B_{bp}}{C_7} \tag{3b}$$

A coarse and fine control of BW_p are provided by the control of g_{m5} using the CTA control scheme described earlier. Similarly BW_z is controlled by varying g_{m4} and/or g_{m3}. The independent fine control of ω_z and ω_p is provided by the control of g_{m1} and g_{m2} respectively. Note also that a coarse control of ω_z and ω_p is provided by the control of g_{m3} and g_{m2} in addition to programmable capacitors C_6 and C_7.

Fig. 5 shows the range of pole bandwidths and pole frequencies ideally attainable with the proposed biquad using a combination of coarse and fine control schemes. It is seen that over 3 decades of adustment is possible in each case. It is difficult to determine the exact pole location resolution because the fine adjustment ranges are intentionally overlapped to guarantee complete coverage after fabrication. A very conservative estimate of pole location resolution involves using the sensitivities of ω_{op} and BW_p with respect to a single 'fine tune' parameter. Using sensitivity analysis, it can be shown that

$$\left|\frac{\Delta\omega_{op}}{\omega_{op}}\right| < 0.5\%, \quad \left|\frac{\Delta BW_p}{BW_p}\right| < 1\% \tag{5b}$$

Identical results can be obtained for the sensitivities of ω_{oz} and BW_z as function of their fine tune controls.

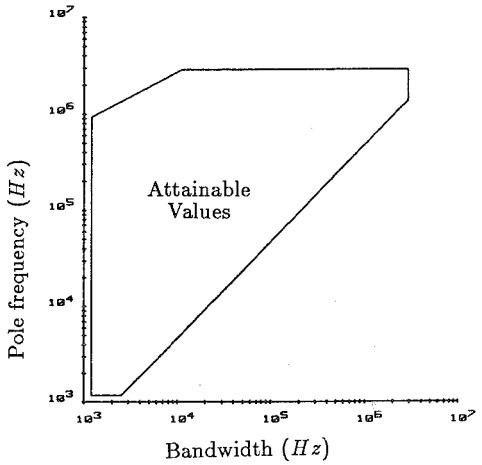

Fig. 5. Attainable pole frequencies and bandwidths.

Experimental Results

A prototype CSP consisting of a cascade of 3 biquad stages, along with associated control and measurement circuitry, was fabricated in a 3μ double-poly p-well process[5].

In order to test the fabricated chip and to apply the required digital control signals that configure and tune the CSP, a digital controller was designed based upon a commercial Hitachi HD68P01 microcomputer chip. Different test programs were written and stored in EPROM in order to test different filter configurations and to study the tuning characteristics of the CSP. Some initial test results are presented here.

First, the realizability of different second-order filter functions was tested by using the different control combinations listed in Table 1 for a single biquad stage. Here, nominal values of transconductances and capacitances were used by adjusting the corresponding control signals to values midway between their maximum and minimum values. The measured frequency reponses obtained for the bandpass, lowpass, highpass and lowpass notch configurations are shown in Fig. 6. The nominal value of f_o here is approximately 750 kHz. Due to a design error in the OTA output stage and the D/A block, the range of available transconductances in the pro-

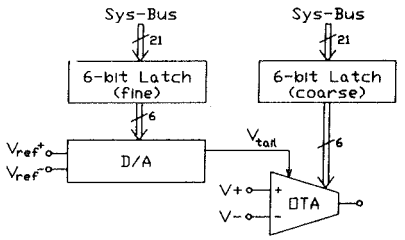

Fig. 2. CTA block diagram.

Controlled Transconductance Amplifier

A block diagram of the CTA is shown in Fig. 2. It contains an OTA whose transconductance parameter can be fine-adjusted by controlling the output of the D/A, V_{tail}. A course adjustment is also incorporated in the output stage of the OTA. The latches shown are used to store the digital control words that program the overall transconductance of the CTA. The actual circuit implementation of the OTA and the coarse adjustment scheme is discussed below.

Fig. 3 shows the circuit diagram of the OTA employed here. The circuit is a slightly modified version of a recently reported approach for designing CMOS OTAs[4]. It employs a linearized input stage consisting of a simple source-coupled pair M_1, M_2 biased dynamically by a compensating current component which is proportional to the square of the differential input voltage. This square-law compensating current (generated by M_3–M_6) is used to counter the inherent quadratic nonlinearities of the source-couped differential pair itself. By properly scaling the W/L ratios of the source-coupled pair and the cross-coupled devices, the nonlinearities of the input stage can be largely cancelled out over a wide input voltage range[4]. The control voltage V_{tail} sets the bias currents and determines the transconductance of the input stage. The output currents obtained from this linearized stage are subtracted using current mirrors. Both n-channel and p-channel output mirrors employ multiple output stages as shown in Fig. 3. Depending on the state of the coarse control bits A_0–A_5, one or more of these output stages are connected in parallel, resulting in a digitally controlled coarse scaling of the overall transconductance value. The range of scale factors obtained with this scheme extends from unity to less than 0.01.

The W/L ratios of the six output stages were selected to allow g_m to be incremented by factors of 1.618. For example, assume that the gain of the first stage (M_{28}–M_{33} in Fig. 3) is $(1.618)^{-10}$. If the second stage (M_{34}–M_{39}) is enabled while all others are disabled, the gain is $(1.618)^{-9}$. If the first and second stages are enabled, the gain is $(1.618)^{-10} + (1.618)^{-9} = (1.618)^{-8}$. Table 2 completes this example. The factor 1.618 is optimal is that it is a solution of the equation $1 + x = x^2$. Thus, gains such as $(1.618)^{-8}$ may be obtained by enabling the $(1.618)^{-10}$ and $(1.618)^{-9}$ stages rather than requiring a separate stage.

To ensure that there are no undesirable gaps in the obtainable values of g_m, the fine-control voltage V_{tail} is varied over a range that adjusts the g_m value by a factor of approximately 1.87. In order to maintain a resolution of at least 1 % over this range, a logarithmic D/A was implemented in which the control voltage V_{tail} was obtained at the different taps in a string of 63 logarithmically weighted resistors. Here, varying adjacent resistors in the string by a factor of 1.0086 gives the desired logarithmic variation in g_m over the range of interest.

Table 1. Gain of OTA as a function of coarse control digital input assuming gain of first stage is equal to $(1.618)^{-10}$.

A_0	A_1	A_2	A_3	A_4	A_5	Gain
1	0	0	0	0	0	$.00813 = (1.618)^{-10}$
0	1	0	0	0	0	$.01316 = (1.618)^{-9}$
1	1	0	0	0	0	$.0213 = (1.618)^{-8}$
0	0	1	0	0	0	$.0344 = (1.618)^{-7}$
1	1	1	0	0	0	$.0557 = (1.618)^{-6}$
0	0	1	0	0	0	$.0902 = (1.618)^{-5}$
1	1	1	1	0	0	$.1459 = (1.618)^{-4}$
0	0	0	0	1	0	$.236 = (1.618)^{-3}$
1	1	1	1	1	0	$.382 = (1.618)^{-2}$
0	0	0	0	0	1	$.618 = (1.618)^{-1}$
1	1	1	1	1	1	$1.000 = (1.618)^{0}$

Programmable Capacitance Array

To allow coarse control over the realized poles and zeros (ref. Eq. (1)), each capacitor in the biquad is made programmable by switching in one or more capacitors in a parallel array depending on the value of a digital control word. For a nominal transconductance value g_m, the minimum and maximum capacitance values required are given respectively by $\hat{C}_0 = g_m/\omega_{o0}$ and $\hat{C}_N = g_m/\omega_{oN}$, where ω_{o0} and ω_{oN} are, respectively, the maximum and minimum integrator frequencies desired. For N logarithmically spaced frequencies

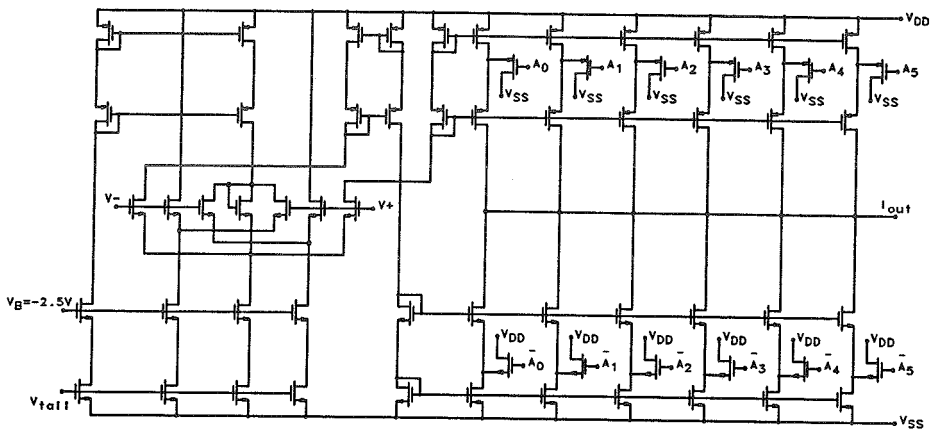

Fig. 3. OTA with a 6-bit coarse control schematic.

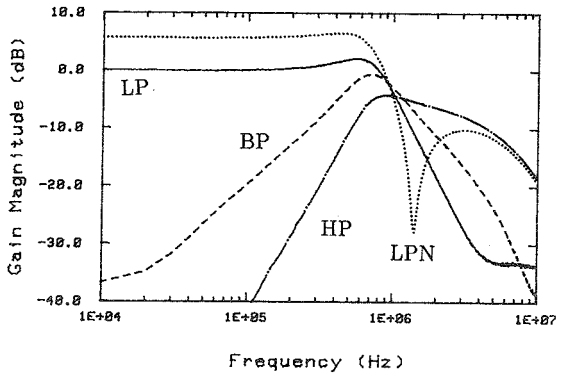

Fig. 6. Various filter transfer functions.

totype CSP was limited to values approximately between 48 and $65\mu A/V$. Thus, for $C_5 = C_6$, this limited the maximum available Q to approximately 1.35. Using extremes of capacitance values, the Q is still restricted to about 4. The above errors have since been corrected and a new version of the circuit has been submitted for fabrication. This new circuit is expected to provide the full control range and resolution capabilites specified earlier. A summary of the nominal lowpass and bandpass characteristics measured for the prototype biquad is provided in Table 3.

Table 3. Summary of measured filter performance.

	Lowpass	Bandpass
Passband Noise Density ($\eta V/\sqrt{Hz}$)	270	250
3 dB Bandwidth (kHz)	760	580
Total Inband Noise (mV_{rms})	0.23	0.20
1% Distortion Level (V_{rms})	1.0	1.2
Dynamic Range (dB)	73	76

Fig. 7 shows the effect of varying the capacitances C_6 and C_7 over their entire range (while keeping $C_6 = C_7$) for the bandpass configuration. Although 20 values of f_o are generated within this range corresponding to the 20 states of the programmable capacitor arrays, only 4 responses are shown for clarity. Fig. 8 illustrates the capability of realizing higher-order filters by cascading one or more biquads. The three bandpass filter responses generated by biquads 1–3 are shown along with fourth-order and sixth-order responses obtained by cascading Biquads 1 and 2, and Biquads 1, 2 and 3, respectively.

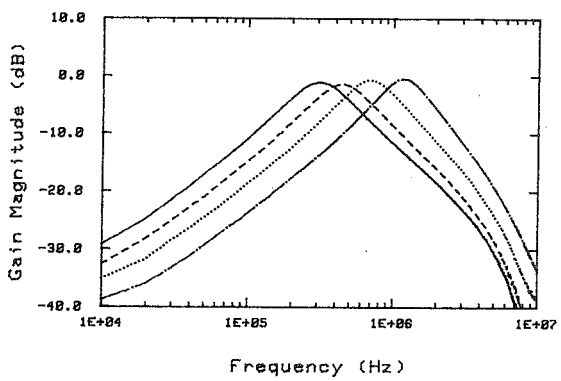

Fig. 7. 2nd Order Bandpass filter with various center frequencies.

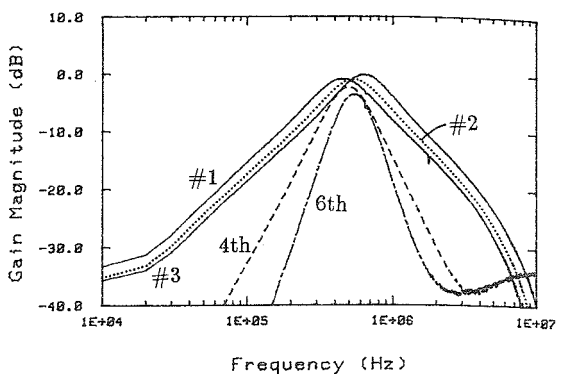

Fig. 8. Higher-Order Bandpass filters.

Conclusion

A reconfigurable biquadratic building block has been designed for applications in digitally controlled analog signal processing systems. The basic biquad is based on a two-integrator-loop OTA structure where the transconductances of each OTA as well the values of the integrating capacitors are digitally controlled. Design details have been discussed and experimental results obtained from a fabricated prototype test chip have been presented. The results show that the basic design is functional and capable of realizing bandpass, lowpass, highpass as well as notch transfer functions. The pole and zero frequencies are tunable between approximately 300 kHz and 1.2 MHz, although the maximum Q is limited to about 4. The possibility of realizing higher-order transfer functions by cascading the individual biquads has been demonstrated. A second generation design, which is expected to provide wider control range and higher values of Q, is presently under fabrication.

References

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