A 10 MHz CMOS CONTINUOUS–TIME PROGRAMMABLE BANDPASS FILTER

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Introduction

Recently, several continuous–time high frequency filters have been reported in the literature [1]-[3]. These structures use the transconductance amplifier instead of a conventional op amp to take advantage of the inherently better high frequency performance of the transconductance structures. Although the transconductance amplifier offers better high frequency performance than the op amp, the performance of this device also deteriorates at high frequencies limiting the performance of reported monolithic filters employing these devices to a few megahertz. The major limitation in the high frequency performance of typical transconductance amplifier architectures are attributed to the limited bandwidth of internal current mirrors. Two groups have recently investigated simpler transconductance amplifiers in which the current mirror has been eliminated to improve the high frequency performance. Khorram-abadi and Gray [1] use a single stage "transconductor". However, the lack of an active Q control scheme restricts the application of this structure to low Q filters. The dynamic range of this structure was modest and operation was limited to the 500 KHz range. More recently, Park and Schaumann reported [3] a 4 MHz bandpass filter using a CMOS inverter–like single stage transconductor. Although they were successful at improving the operating frequency range, the dynamic range was still quite limited.

In this paper, a new integrator structure is proposed which employs a CMOS inverter–based single stage fully balanced transconductor and the intrinsic capacitances of the MOS transistors. This structure operates at higher frequencies and offers improvements in dynamic range over existing schemes. Employing the proposed integrators, a programmable 16 MHz bandpass filter has been designed and fabricated in a 3μ double metal CMOS process.

Design of a programmable Integrator

A fully balanced transconductor–based integrator is shown in Fig. 1. The fully balanced structure is employed to improve the linear input range. If the input pairs are matched, it is well known that even order harmonics in the output cancel out with this structure.
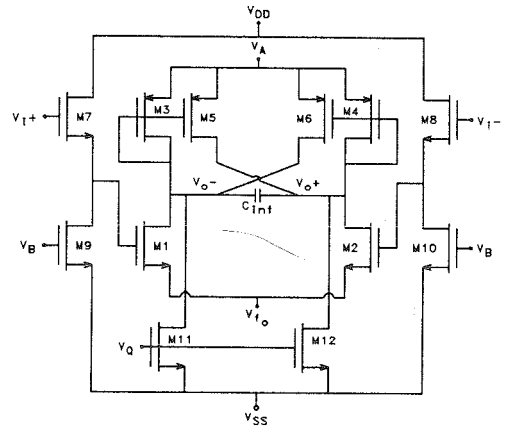

Fig. 1 A cross–coupled load, fully balanced integrator.

If the drain junction capacitances and parasitic layout capacitances are neglected and all transistor pairs are assumed to be matched, the transfer function of this integrator is approximately given by

$$\frac{V_o(s)}{V_i(s)} \cong \frac{-g_{m_1}}{g_o + sC_L} \tag{1}$$

where $g_o = g_{m_3} - g_{m_5} + g_{ds_1} + g_{ds_3} + g_{ds_5}$, $C_L \cong C_{gs_3} + C_{gs_5} + 2C_{int}$. Here, g_{m_1}, g_{m_3}, g_{m_5} are transconductances, g_{ds_1}, g_{ds_3}, g_{ds_5} are output conductances, C_{gs_3} and C_{gs_5} are gate–source capacitances of the transistors, and C_{int} is the extrinsic integrating capacitor. For high frequency operation, C_{int} is purposely omitted. Substituting parameters from the device model equations for g_{m_1}, C_{gs_3}, and C_{gs_5}, the integrator unity gain frequency is then approximately given by

$$\alpha_o \cong \frac{3}{2} \frac{\overline{\mu_n}(W_1/L_1)(V_{GS_1} - V_{TH_1})}{W_3 L_3 + W_5 L_5} \tag{2}$$

where μ_n is the electron mobility, W_1, W_3, and W_5 are widths of the transistors, L_1, L_3, and L_5 are lengths of the transistors, V_{GS_1} is the gate–source bias voltage, and V_{TH_1} is the threshold voltage of M1. It can be seen that α_o is determined by the transistor sizes and further controlled by the voltage V_{GS_1}. In this structure, the

source voltage, V_{f_o}, controls V_{GS_1} and thus α_o. If the same device length is used for all load transistors, the expression (2) can be rewritten as

$$\alpha_o \cong \frac{3}{2} \frac{\overline{\mu_n}(W_1/L_1)(V_{GS_1} - V_{TH_1})}{W_3 L_3 (1 + r)} \tag{3}$$

where $r = W_5/W_3$

The nonzero lossy conductance term in the denominator of (1), which is normally dominated by g_{m_3}, introduces a leading phase which degrades the integrator Q. In the proposed integrator structure, the width ratio, r, of the two load transistors M3 and M5 (or M4 and M6) is properly determined so that the leading phase can be effectively cancelled out. Alternatively, the lossy conductance term can also be set to any desired value by appropriately sizing M3–M6 to implement a lossy integrator. Although the compensation scheme considerably reduces the leading phase of the integrator, it is often necessary to intentionally lower the integrator Q to compensate for parasitic induced excess lagging phase which tends to seriously enhance the integrator Q at high frequencies for high Q filters. The voltage controlled current sources M11 and M12 are used to adjust the integrator Q by pulling currents from the load devices, M3–M6, thus adjusting the lossy conductance value. Transistors M7–M10 are used as a buffer to reduce the effect of the input capacitances on the output of the previous stages and are also used as a level shifter to improve the signal handling capability.

Design of a tunable biquadratic filter

The complete block diagram of a fully differential integrator–based second–order filter which can utilize the integrator of Fig. 1 is shown in Fig. 2. This structure has both bandpass and lowpass outputs. The first and third stages are a lossy integrator and an ideal integrator respectively implemented as was described previously except for a few changes. Another set of buffer is used in the first stage integrator to provide a summing input for the feedback signal. In the third stage lossless integrator, the common sources of input devices, M1–M2, and those of the load devices, M3–M6 are connected V_{DD} and V_{SS} respectively instead of V_A and V_{f_o}. The second stage is an inverting wide band amplifier which is used to provide common mode stability. Fig. 3 shows a wide band amplifier configuration which is basically the same as that of the integrator except for the including of two load transistors M13 and M14 which are operating in ohmic region. From the first–order model, the small signal half circuit resistance of this additional load can be obtained as

$$r_o = \frac{1}{\beta_o(V_{GS_{13}} - V_{TH_{13}})} \tag{4}$$

The resistance values of these load devices are designed to be low enough to guarantee a constant gain in the frequency range of interest. Then, the gain of the wide

band amplifier is approximately given by
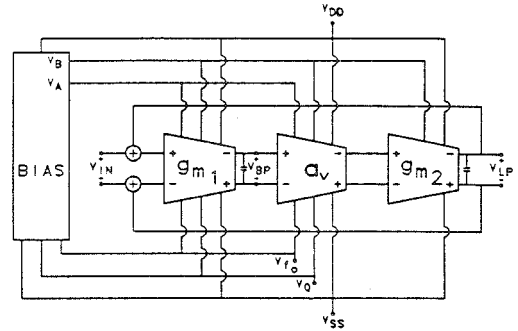
$$a_v = -g_{m_1} r_o \tag{5}$$

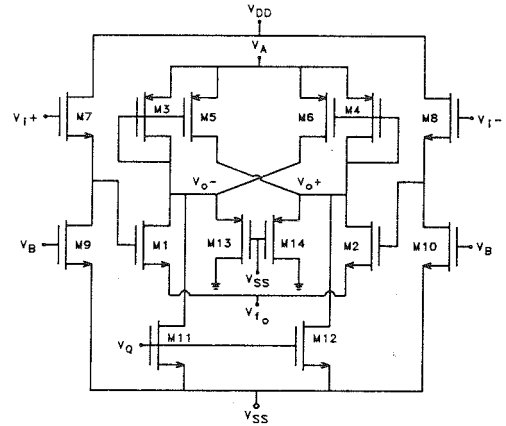Fig. 2 A complete block diagram of a fully balanced integrator based filter.

Fig. 3 A wide band amplifier

The voltage transfer functions of the first, second, and the third stage are respectively given by the equations (6), (7), and (8).

$$A_{v_1} = \frac{-\alpha_{o_1}\omega_{g_1}}{(s + \omega_{p_1})(s + \omega_{g_1})} \cong \frac{-\alpha_{o_1}}{s + \omega_{p_1}} \tag{6}$$

$$A_{v_2} = \frac{-a_v \omega_{g_2} p_a}{(s + \omega_{g_2})(s + p_a)} \cong -a_v \tag{7}$$

$$A_{v_3} = \frac{-\alpha_{o_2}\omega_{g_3}}{(s + \omega_{p_2})(s + \omega_{g_3})} \cong \frac{-\alpha_{o_2}}{s + \omega_{p_2}} \tag{8}$$

where α_{o_1}, α_{o_2} are the unity gain frequencies of the first and third stage integrators, ω_{p_1}, ω_{p_2} are the 3dB frequencies of the first and third stage integrators, ω_{g_1}, ω_{g_2}, and ω_{g_3} are the effective high frequency poles of each stage, p_a is the 3dB pole frequency of the second

stage wide band amplifier, and a_v is the gain of the second stage amplifier. From the approximate equations of (6)–(8), the bandpass filter transfer function can be derived as

$$A_v(s) \; = \; \frac{-\alpha_{o_1}(s + \omega_{p_2})}{s^2 + (\omega_{p_1} + \omega_{p_2})s + \omega_{p_1}\omega_{p_2} + a_v\alpha_{o_1}\alpha_{o_2}} \quad (9)$$

The third stage integrator can be made lossless if ω_{p_2} is eliminated by compensating for the leading phase as was discussed previously. Thus, assuming the third stage integrator is lossless, the filter resonant frequency and the filter Q are given by

$$\omega_o \; \cong \; \sqrt{a_v\alpha_{o_1}\alpha_{o_2}} \quad (10)$$

$$Q \; \cong \; \frac{\omega_o}{\omega_{p_1}} \quad (11)$$

In Fig. 2, α_{o_1} and a_v are used to set the filter resonant frequency, whereas Q is controlled by ω_{p_1}. In the practical filter, the high frequency poles, ω_{g_1}, ω_{g_2}, ω_{g_3}, and p_a introduce the excess lagging phase shift in each stage which consequently result in an enhancement in the filter Q. Hence, it is often necessary to increase ω_{p_1} of the first stage lossy integrator to compensate for the excess phase induced Q enhancement.

In Fig. 4, a bias circuit is shown. The transistors MB1, MB2, MB4, MB5 are sized to have the same W/L ratio of M7, M9, M1, and M11 of the first stage integrator respectively, whereas the W/L ratio of MB3 is the same as the combined W/L ratio of M3 and M4. Since the output node of the inverter MB3–MB4 is connected to the virtual ground of the op amp, the output operating point of the integrator can also be set at around zero potential. Note that, with the help of bias circuit, the currents of integrator input transistors, M1 and M2, do not change as the Q control voltage, V_Q, is adjusted. This makes the Q control independent of the frequency control.
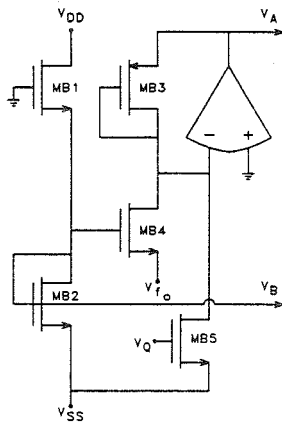
Fig. 4 A bias circuit

Experimental results

This filter was designed to have the nominal cut off frequency of 10 MHz, and a nominal Q of 10, and fabricated using 3μ CMOS double metal process. In Fig. 5, the photomicrograph of the experimental chip including bias circuit and an on–chip output buffer is shown. The total chip area is 602 x 495 μm^2. Excluding the buffer, the filter and bias circuitry require an area of 546 x 170 μm^2. Tested with a ±5 volt power supply, the filter and bias circuitry consumed 69 mW of power.
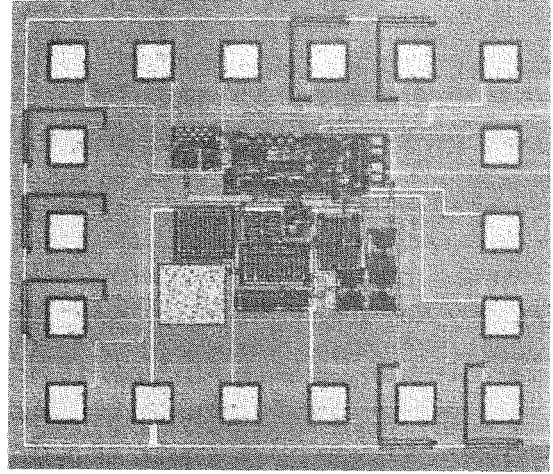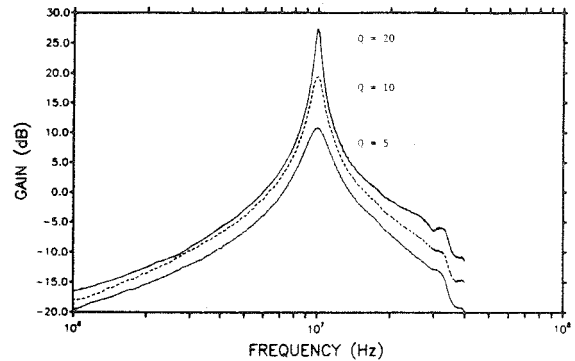
Fig. 5 A photomicrograph of the second–order filter

Fig. 6 shows the measured frequency responses of the second–order bandpass filter for different values of the control variables. Experimental results exhibited a maximum output swing of 883 mV_{rms} at 1% THD with a total in band noise of 1.46 mV_{rms} and a corresponding dynamic range of 55.6 dB when programmed to operate with $f_o = 10MHz$ and $Q = 10$. The center frequency of this filter was adjustable throughout a range from 1.76 MHz to 16.86 MHz and Q adjustable range of 0.5 ~ 68.9 was obtained. In Fig. 7, the measured f_o and Q control domain of this filter is plotted.
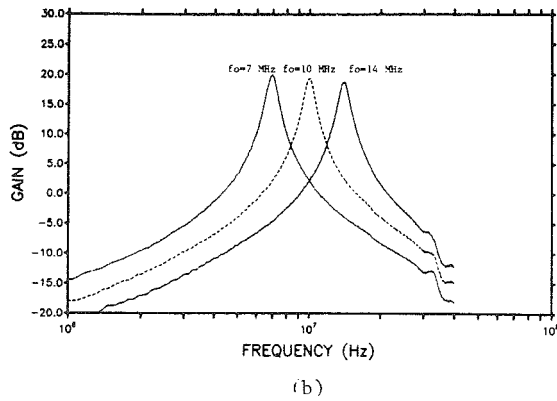
(a)

(b)

Fig. 6 Measured variations in the frequency response of bandpass filter: (a) for constant $f_o = 10$ MHz, (b) for constant $Q = 10$.
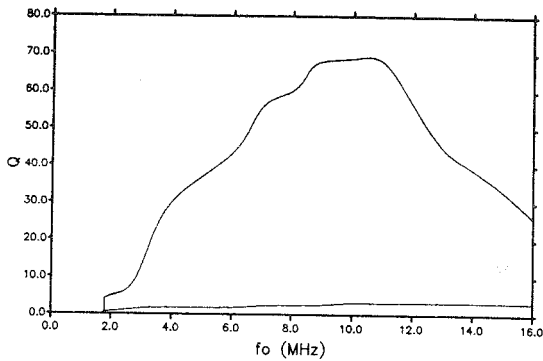

Fig. 7 The measured f_o and Q control domain of the second-order bandpass filter

Conclusion

A continuous-time high frequency monolithic filter has been implemented which operates at a nominal cut off frequency of 10 MHz and Q of 10 using a new single stage transconductor-based integrator. It is shown experimentally that wide control range for both cut off frequency and Q can be obtained with this technique.

References

[1] H. Khorramabadi and P.R. Gray, "High-Frequency CMOS Continuous-Time Filter," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 939–948, Dec. 1984.

[2] A. P. Nedungadi and R. L. Geiger, "High-Frequency Voltage-Controlled Continuous-Time Lowpass Filter Using Linearized CMOS Integrators," *Electron. Lett.*, vol. 22, pp. 729–731, July 1986.

[3] C. S. Park and R. Schaumann, "Design of an Eighth-Order Fully Integrated CMOS 4 MHz Continuous-Time Bandpass Filter with Digital/Analog Control of Frequency and Quality Factor," in *Proc. Int. Symp. Circuits and Systems*, 754–757, Philadelphia, PA, May 1987.