THE CHARGE AMPLIFIER, AN ALTERNATIVE FOR SWITCHED-CAPACITOR STAGES

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Abstract - This paper describes a very fast, low-power, linear sample/hold amplifier, to be used in complex discrete-time systems like filters or analog/digital converters. The gain is realized by amplifying a charge rather than a voltage, using a current-mirroring scheme based on a comparator and switcheable current sources. The scheme has several advantages over switched-capacitor stages. It is very robust and can be realized in (rad-hard) bipolar technology.

Basic Operation

The main components of the charge amplifier are shown on figure 1. An initial charge Q_{init} is held on capacitor C. To this charge corresponds a voltage V, such that $Q_{init} = \int_0^V C(v)\,dv$. For an approximately linear capacitor, this could be simplified to $Q_{init} \approx C\,V$. The top plate of the capacitor is connected to a fast comparator, whose output controls the two switcheable current sources, I_1 and I_2. As long as V exceeds the reference level V_{ref}, the comparator output is high and both current sources are ON. As a result, capacitor C is linearly discharged, while capacitor C^{next} is linearly charged, according to the relations ($Q_{ref} = \int_0^{V_{ref}} C(v)\,dv$)

$$Q = Q_{init} - \int_0^t i_1(t)\,dt \quad \text{and} \quad Q^{next} = Q^{next}_{init} + \int_0^t i_2(t)\,dt \quad (1)$$

If we assume that both currents are constant while the sources are ON, this can be simplified to

$$Q = Q_{init} - I_1\,t \quad \text{and} \quad Q^{next} = Q^{next}_{init} + I_2\,t \qquad (2)$$

The time T during which the sources are ON, is determined by the comparator. Neglecting switching delays and parasitic offsets, T can be expressed as

$$T = \frac{(Q_{init} - \int_0^{V_{ref}} C(v)\,dv)}{I_1} = \frac{(Q_{init} - Q_{ref})}{I_1} \qquad (3)$$

The final charge on capacitor C^{next} will be

$$Q^{next}_{fin} = Q^{next}_{init} + I_2\,T = Q^{next}_{init} + \frac{I_2}{I_1}\,(Q_{init} - Q_{ref}) \qquad (4)$$

It is clear that the initial charge of C, Q_{init}, is copied (and amplified) onto C^{next}, as the charge Q^{next}_{fin}. The charge gain A_q is expressed by I_2/I_1. The output-refered offset is given by

$$Q^{out}_{off} = Q^{next}_{init} - A_q\,Q_{ref} \qquad (5)$$

Gain and offset can be set to any value by proper choice of initial charges, reference level and currents. An inverting charge amplifier can be implemented by reversing the direction of I_2. The charge amplification process *does not* rely on the linearity (or even the exact values) of the capacitors. Accuracy of the gain is determined only by the extent to which the two current sources maintain a fixed current ratio. It should be noted that the comparator output is a digital signal, which represents the initial charge in pulse width modulated (PWM) form, since the ON-time, T, is proportional to Q_{init}.

Clocking Scheme

Practical application of the charge amplifier requires synchronization of the charge transfers. This is accomplished by a multi-phase, non-overlapping clock. At least three phases are needed, although a fourth phase is normally added for offset cancellation. Two additional phases are necessary to use the charge amplifier within an analog/digital converter (ADC) stage. The six phases will be discussed next.

Figure 2 shows one charge amplifier stage, clocked using a three-phase scheme. Input as well as output are in PWM form. During phase Φ_1 (the "pre-charge" phase), capacitor C is charged (or discharged, depending on the direction of the current) to a fixed voltage V_p, with associated charge Q_p. During phase Φ_3 (the "load" phase), the PWM input is activated through AND gate N_1, and a signal charge $Q_s = I_1\,T_{in}$ is added onto C. During phase Φ_6 (the "final discharge" phase), C is discharged down to reference level V_f, using the comparator and AND gate N_2. Assuming ideal components, the output pulse width, T_{out}, is related to the input pulse width T_{in} according to

$$T_{out} = \frac{Q_p + Q_s - Q_f}{I_2} = \frac{I_1}{I_2}\,T_{in} + \frac{Q_p - Q_f}{I_2} \qquad (6)$$

It is clear that the gain of the stage can be modified by adjusting the current ratio, and the offset by changing V_p or V_f. This makes it possible to use the charge amplifier as a basic component of tunable, self-calibrating or programmable systems.

The basic scheme has shortcomings: neither Q_p nor Q_f can be controlled accurately. The actual precharge voltage may be slightly different from V_p due to clock feed-through introduced by the switch. The actual final discharge voltage may be different from V_f due to a systematic comparator offset, or the finite switching time t_d of the comparator (the capacitor will consistently undershoot the reference voltage by a small amount, with corresponding charge $Q_u = t_d\,I_2$). In addition, the comparator may be subject to noise, which can be modeled either as an input-refered noise voltage, or an equivalent jitter on the parasitic switching delay t_d (figure 3).

The unpredictability of Q_p and Q_{ref} can be greatly reduced by adding an auto-zero scheme during clock phase Φ_2. This is shown on figure 4. During Φ_1, C is pre-charged to a voltage V_p', slightly above the desired V_p. During Φ_2 (the "initial discharge" phase), C is partially discharged, using the comparator and reference voltage V_p. During Φ_3, Q_s is applied and during Φ_6, the capacitor is discharged to the final level V_f. Ideally, the relationship between input and output pulse width is still given by equation 6. However, due to the initial discharge operation, Q_p is not affected by clock feed-through anymore. In addition, the effect of systematic offsets in the comparator is canceled, since the terms Q_p and Q_f are both subject to the same offset. In a similar way, the effect of finite comparator switching delay is canceled, since the undershoot charge $t_d\,I_2$ affects Q_p and Q_f to the same extent.

(It should be noted that since I_2 is constant, the slew rate dV/dt at the comparator input is the same, which normally implies similar switching characteristics.) Low-frequency comparator noise components (or alternatively: time jitter) are reduced as well, since the input-refered noise does not change much during the short time between Φ_2 and Φ_6 (typically less than 100 ns). Functionally, the combination of initial and final discharge phases implements correlated double sampling. The mechanism is crucial in ultra-fast systems, where signal pulse widths become comparable to the comparator delay.

Switching Transients

So far, it was implied that the current sources could switch ON or OFF in a negligible time. In practice, the currents exhibit a transient behavior, caused by finite clock transition times and the limited speed of comparator, switches and logic gates. Although the transient waveforms are hard to predict, it can be assumed that every time a source is turned ON or OFF, the transient will be the same. This is motivated by the fact that the clock signals are periodic, and that the comparators in the system always switch under identical conditions (same reference voltage, same dV/dt on the capacitor). If the charge stage is designed so that the minimum pulse width of any signal is always longer than the transition times (typically $5-10$ ns), no gain error or non-linearity (signal-dependent error) will be introduced, but at most a small offset error. This offset is insignificant in many applications and can be minimized by carefully matching the characteristics of I_1 and I_2. This works best for inverting amplifiers, where the directions of I_1 and I_2 are the same. Further reduction would probably require some external adjustments.

A/D Converter Stages

The charge amplifier was specifically developed in an attempt to realize a digitally self-calibrated 14-bit, 5 MHz pipeline in 1μ CMOS technology. The block diagram of one pipeline stage is shown on figure 5. An implementation using a charge amplifier with gain of -2 and two comparators (1.6 bits per stage) is shown on figure 6. At the end of phase Φ_3, a charge proportional to the input signal is present on holding capacitor C. Two comparators (K_2 and K_3) compare the voltage (approximately proportional to the charge) against two reference levels and produce a thermometer code. The reference levels are generated by using a resistive reference string to create pre-charge levels on auxiliary capacitors C_1 and C_2 (phase Φ_1). During Φ_2, an initial discharge operation is realized with K_4 and I_3 in order to match the initial discharge operation on C (*minor* errors on the comparator levels are irrelevant, since digital error correction is applied throughout the pipeline by overranging [1,2]. During Φ_4 ("latch phase"), the outputs of K_2 and K_3 are latched. During Φ_5 ("DAC" phase), a fixed charge is subtracted from C, according to the comparator outputs. This is accomplished using current sources I_5 and I_6, controlled by a comparator output, Φ_5 and a pulse that is generated by the discharge of C_2.

Current Sources

The main requirements on the current sources are an extremely constant ON-state current and fast switching. In order to obtain 12-14 bit linearity, the output impedance of the sources needs to be at least several $G\Omega$. Such output impedances can be obtained with triple cascode (figure 7) or regulated cascode (figure 8) sources. The latter scheme is preferable for its slightly better voltage range, and the possibility to be switched very reliably. When the control signal to the gate of transistor M_7 is low, the source operates normally. The output current is set by current mirror M_1/M_2. When the control signal goes high, the gate of M_3 is shorted to ground and the output current collapses very quickly. When it goes low again, the current from M_5 pulls M_3 out of its cut-off state and the main current flow is re-established. Circuit simulations revealed transition times in the $5-10$ ns range. They also showed that the steady-state current is not significantly affected by high slew rates (20 $V/\mu s$) at the output, and that charge injection onto C due to gate-drain overlap capacitance of M_3 is not significantly signal-dependent. Another advantage of this switching method, is that the combination of AND and OR gates needed to control the current sources can be implemented directly by replacing M_7 by a series/parallel combination of active pull-down devices.

Various Considerations

Linearity

The linearity of the charge amplification is mainly determined by the output impedance of the current sources, under high dV/dt at the output. Other factors affecting linearity are current switching transients (if the transients are not allowed to die out for short pulse widths, severe distortion may occur), gate-drain overlap of the output transistors within the current sources (minor effect: a very small amount of signal-dependent charge may be injected onto C) and potentially signal-dependent leakage currents within transistors (either drain to source, or to substrate).

Speed

The charge amplifier is extremely fast. It gets a significant speed advantage over switched-capacitor stages from several fronts. First, the holding capacitor is discharged in a linear (constant dV/dt) fashion, rather than through exponential settling, which normally requires up to 10 time constants to reach a sufficiently accurate steady-state value. Secondly, the comparators used in the system only need to drive single (minimum-sized) logic gates, with input capacitances typically in the 10 fF range (CMOS). As a result, these devices are tiny, and fast. Thirdly, none of the comparators needs to be internally compensated. Finally, the holding capacitor is charged and discharged extremely efficiently, making optimal use of a given power budget.

Power Consumption

During Φ_1, the holding capacitor is pre-charged using a single switch (or an equivalent set-up in bipolar technology). This process is 100% efficient, since all the current from the switch ends up on the capacitor. During the other phases, the capacitor is discharged using one of the current sources. Neglecting the amplifier current in the regulated cascodes and the comparators, this process is 100% efficient as well. The total charge drawn from the power supply during one clock cycle, is equal to the difference between the maximum possible charge (signal-dependent for a non-inverting scheme) and the final charge Q_f. For a $1pF$ holding capacitor and $2V$ range, this is typically about $1-2pC$. From this point of view, the charge amplifier works as efficiently as the best class AB opamp [3].

Input and Output Stages

A drawback of systems based on the charge amplifier is that input and output signals are PWM coded. This may be acceptable for certain (e.g. speech) applications, but normally a "translation" from or to voltage is required. The input section can be realized using a regular sample/hold amplifier to sample the signal onto a holding capacitor. Conversion to PWM can then be accomplished using a comparator/current source combination. At the output, a current source can be used to convert the PWM signal to a charge, stored on a capacitor. A voltage follower buffers the (approximately proportional) capacitor voltage to the output.

Multiplexing Reference Levels

Comparator reference levels are different during the initial and final discharge phase. An analog multiplexer, controlled by the clock, is used to choose the appropriate voltage. In CMOS technology, it can be as simple as two single or complementary switches. In bipolar technology, slightly more elaborate schemes could be used, e.g. based on forcing different currents

through a resistor.

Noise

Noise is introduced in three ways. During the precharge phase, kT/C noise is injected onto the holding capacitor. This noise is normally canceled by the initial discharge operation. During the switching operation at the end of the initial and final discharge phases, noise is introduced by the sequence of comparator, logic gates and current source. This noise can be modeled as equivalent input-refered comparator noise, of which the low-frequency components are strongly attenuated by the correlated double sampling.(Time jitter on the comparator delay is an alternative way to discuss the same phenomenon.) The third kind of noise is introduced during the ON condition of the current sources. The output noise current is mainly determined by the noise of transistors M_1 and M_2 (figure 8). The effect of M_1 can be minimized if current sources I_1 and I_2 share the same reference voltage (gate of M_1). The effect of M_2 is reduced by the fact that the transistor is periodically cut off (reset). When the current comes back on, the noise does not get time to build up to significant levels. The current noise has two implications. During the time the current source is ON, the noise is integrated onto the holding capacitor. This effect is normally minor, since the ON time is small ($20nsrange$). A more important effect is that over many clock periods, the steady-state output current itself may drift (despite the reseting of M_2), thus affecting current ratios and gains. This would mainly be due to low-frequency noise components, like 1/f noise in MOSFETS. It could be counteracted by periodic recalibration of the current ratios, using additional circuitry [4].

Supply Noise Rejection

If supply noise reaches the holding capacitor, it is mainly through a supply-dependent variation in comparator offset and logic thresholds. The effect is normally limited, especially since low-frequency components are rejected by the correlated double sampling. Another favorable aspect of the charge amplifier, is that very little supply noise is *generated*. During the pre-charge phase, supply current is drawn, but the pattern is perfectly repetitive and signal-independent, and hence does not cause any cross-talk to other stages. During successive discharge phases, current sources and capacitors are connected in a loop, and no current variations reach the supplies.

Ruggedness

The charge amplifier does not require linear capacitors. In general, it is fairly insensitive to leakage currents, as long as they are not signal-dependent. The scheme is not subject to any stability issues (actually, at the end of a discharge operation, the comparator, logic gates and current source form a feed-back system, but this system is strictly unidirectional; although in small-signal sense it may be unstable, a definite, zero-current equilibrium point is always reached). The gain can be set accurately through a *ratio* of reference currents. Finally, since this scheme does not *require* MOS switches, it can be implemented in bipolar technologies, which are less sensitive, especially to radiation.

Discrete-Time Filters

The charge amplifier can be used to realize complex analog discrete-time filters, instead of switched-capacitor stages. However, there is a distinction. In a switched-capacitor (SC) filter, a combination of MOS switches and capacitors are normally used to emulate resistors between low-impedance nodes, thus turning an opamp with feed-back capacitor into an integrator [5]. The charge amplifier implements a fixed transfer function of the form $A\ z^{-1}$ in the Z domain. Blocks with such transfer function can be combined into higher-order filters, in a way similar to fully digital filters rather than traditional SC filters.

Conclusion

The basic principle of the charge amplifier was introduced. The scheme was extended to include correlated double sampling, and further into an actual pipelined ADC stage. Various considerations were briefly discussed, like linearity, speed, power consumption, noise and ruggedness. From these, it appears that the charge amplifier has several advantages over switched-capacitor stages.

Acknowledgements

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References

(1) S. Lewis et al., "CMOS Pipelined 5 Msample/s 9b ADC with Digital Correction", IEEE Journal of Solid-State Circuits, pp. 954-961, December 1987.
(2) E. Soenen, P. VanPeteghem et al., "Bridging the Gap between Design and Testing of Analog Integrated Circuits", Proceedings of IEEE International Symposium on Circuits and Systems, New Orleans, May 1990.
(3) R. Castello, P. Gray, "A High-Performance Micropower Switched-Capacitor Filter", IEEE Journal of Solid-State Circuits, pp. 1122-1132, December 1985.
(4) W. Groeneveld et al. "A self-Calibration Technique for Monolithic High-Resolution D/A Converters", Proceedings of IEEE International Solid-State Circuit Conference, San Fransisco, February 1989.
(5) R. Gregorian, K. Martin, G. Temes, "Switched-Capacitor Circuit Design", Proceedings of the IEEE, pp. 941-966, August 1983.

Figures

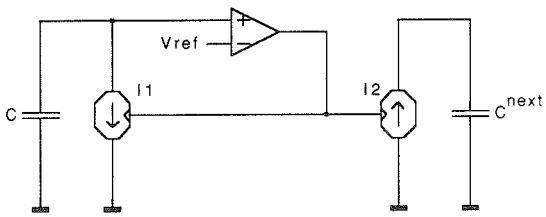

Figure 1:
Basic Charge Amplifier Components

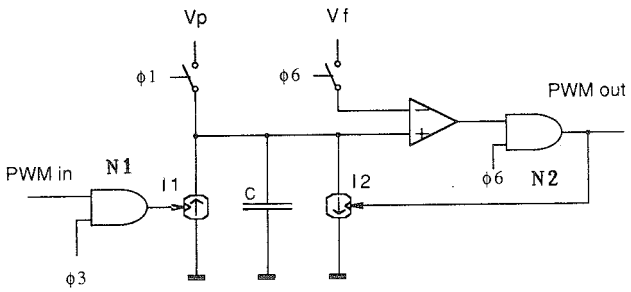

Figure 2: Three-Phase Scheme

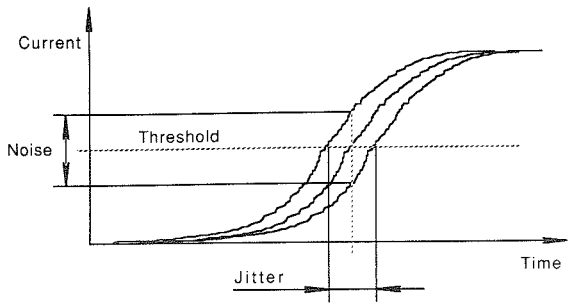

Figure 3:
Effect of Noise on the Switching

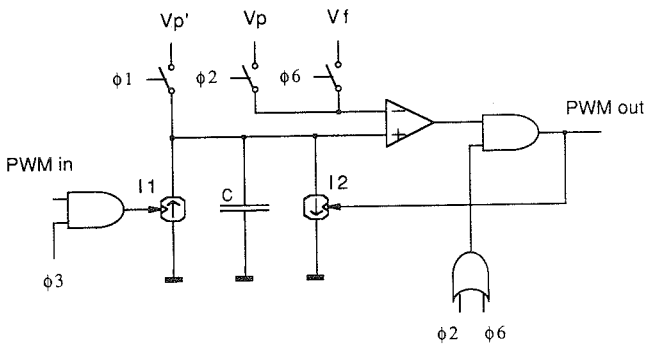

Figure 4: Four-Phase Scheme

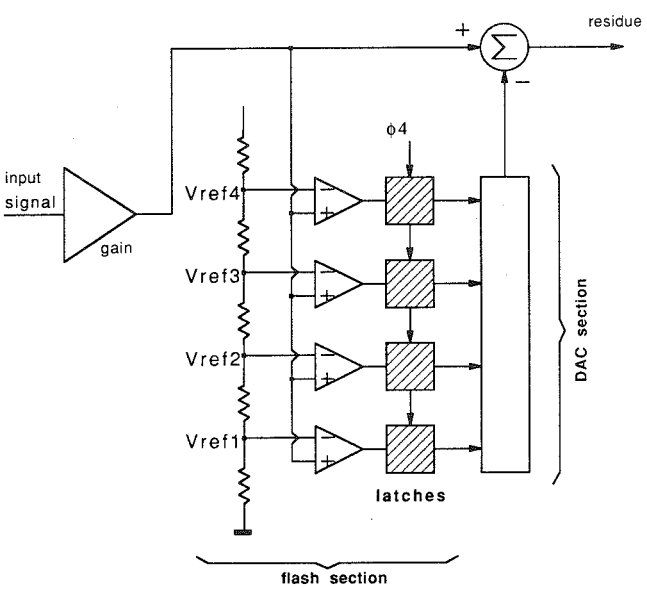

Figure 5:
Block Diagram of A/D Converter Stage

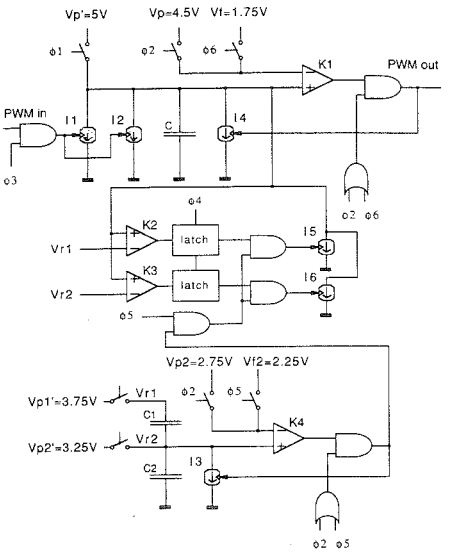

Figure 6:
Charge-Based A/D Converter Stage

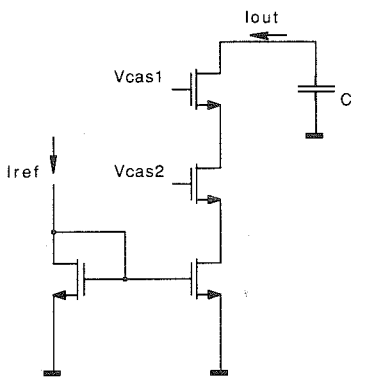

Figure 7:
Triple Cascode Current Source

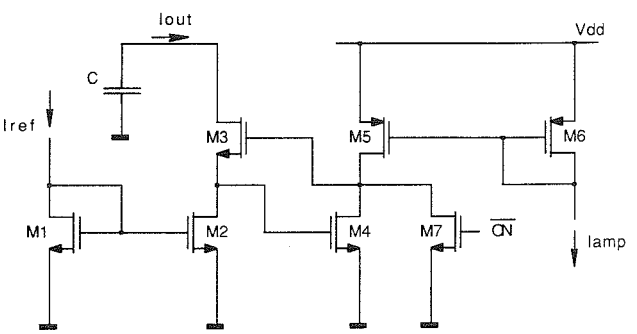

Figure 8:
Regulated Cascode Current Source