PRECISION OFFSET COMPENSATED OP-AMP WITH PING-PONG CONTROL

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Introduction

In many op-amp applications, offset cancellation or reduction is critical because an amplifier input offset voltage limits the capability of the system. For continuous-time integrated applications, a number of offset cancellation schemes have been presented [1]-[3]. Commonly used auto-zero techniques use analog switches to implement low-offset amplifiers. The offset cancellation of these techniques is limited to the $1mV$ range by the charge injection due to auto-zero switches. The schemes have noise in switching and typically have 50% duty cycles, making them unsuitable for continuous-time applications.

In this paper a digital correction technique is presented to keep the noise of the offset compensation circuit small. A ping-pong architecture is employed to obtain an useful 100% duty cycle. The objective is to compensate for inherent matching-induced offsets in the $-30mV$ to $+30mV$ range to achieve an useful op-amp with an offset voltage of less than $1mV$. The proposed architecture is available to achieve even much lower offsets.

Offset Tuning Strategy

To reduce offset voltages a programmable current mirror instead of a simple current mirror is used as the load of the differential input stage of a two-stage CMOS op-amp in Fig.1. The transistor MP1 and MP2 are biased to operate in their linear regions such that they can behave as variable resistors. By changing the bias voltages VTB and VT, we can get various current mirror gains. This can reduce the offset voltage. The way to correct the offset is clear and simple. First, the output voltage of the op-amp is compared to zero when both input terminals are grounded. Next, the bias voltages of the transistors MP1 and/or MP2 are changed in the direction of reducing the offset. The procedure is repeated until the op-amp output voltage crosses zero.

Fig.2 shows the simulated offset correction of the op-amp in Fig.1. We assume that the input referred offset voltage is 30mV. The bias voltage VTB is fixed at 1.7V. It can be seen that the op-amp initially has an offset voltage of +30mV when VT=1.7V, but very small offset can be obtained by decreasing VT to around 1.1V. The performance of the offset reduction will depend upon the resolution of the bias voltage. The offset adjustable range varies with the transistor sizes of the programmable current mirror. The offset adjustable op-amp consists of three blocks: an op-amp block, a timing signal generator, and an offset tuning block.

Op-amp Block

The op-amp block shown in Fig.3 consists of two identical op-amps and several analog switches which are used for implementing a ping-pong structure. The ping-pong structure can obtain a 100% duty cycle by switching. Only one of the op-amps is used for signal processing at any one time while the other is used for offset tuning. The switches should be carefully switched when interchanging their roles. Fig.4 shows the 4-bit timing diagram of the timing signal generator which produces the four-phase clock signals P1–P4 for the ping-pong structure. Q1–Q4 are the outputs of the 4-bit counter which is the key component of the timing signal generator.

For 8 clock periods OPA1 processes an input signal while OPA2 is tuned. At the 8th clock falling edge $P3$ first goes to high such that the signal input is connected to OPA2. After the transient in OPA2 diminishes the other three phase switches

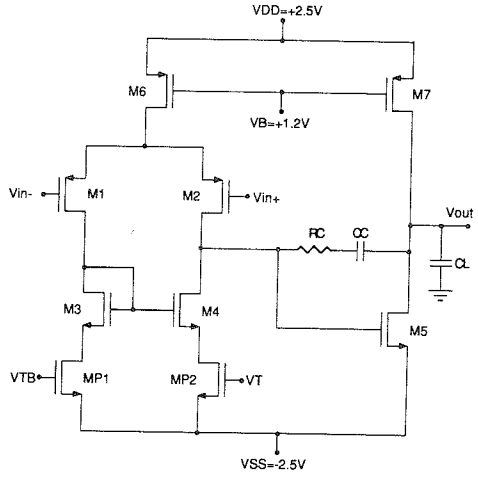

Figure 1: Offset adjustable CMOS op-amp

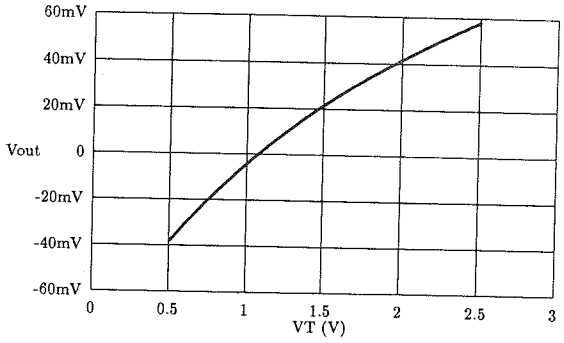

Figure 2: Offset adjustable range (VTB=1.7V)

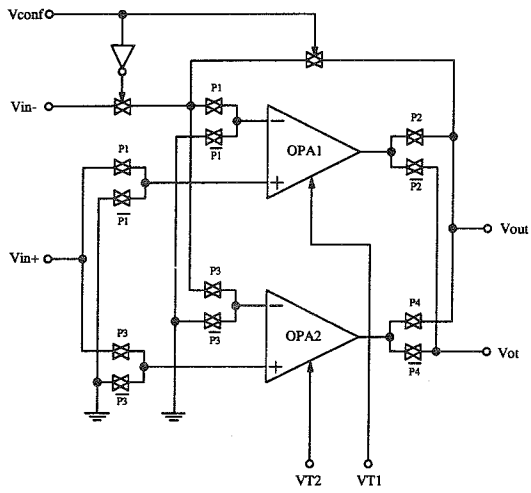

Figure 3: Op-amp block (Ping-pong structure)

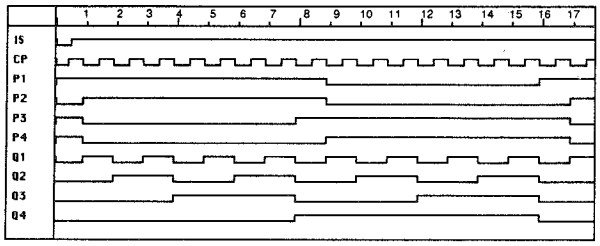

Figure 4: Timing diagram of the timing signal generator

change their states at the 9th clock falling edge. At this time the transient in OPA1 to be used for tuning doesn't affect the tuning because updating the bias voltage is made after one clock period, and one clock period is long enough for the op-amp to finish its transient. In many applications, including interstage amplification in pipelined A/D converters, the tuning phase can be made phase-coherent with the conversion clock, thus eliminating any transients or dead time associated with the ping-pong operation.

Offset Tuning Block

The block diagram of the offset tuning block is shown in Fig.5. This block consists of a comparator, a zero crossing detector (ZCD), two 8-bit up/down counters (UDC block), and two small 8-bit D/A converters (DAC). This block detects the output voltage V_{ot} of the op-amp to be tuned and then provides an updated bias voltage VT such that the offset voltage is reduced. The phase $\overline{P1}$ and $\overline{P3}$ generated from the timing signal generator determine which op-amp will be tuned, so only one of the two up/down counters is enabled to count. The counters are initially set through the signal IS to the half value of the full scale. This is done to accommodate for the inherent bipolarity of the offset voltages.

The negative input of the comparator V_{comp} is connected to ground to make the offset zero. If the comparater output is high, indicating that the offset is greater than zero, then the down signal of the up/down counter is set to '1', so that the counter counts down to decrease the bias voltage VT. The current mirror gain of the programmable current mirror is then decreased,

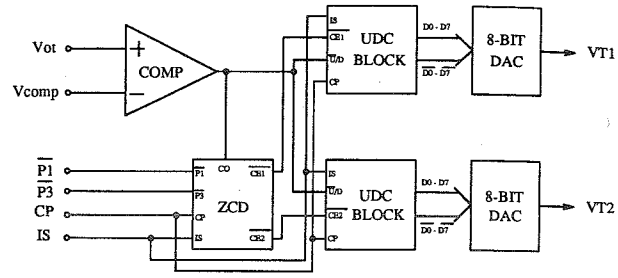

Figure 5: Block diagram of offset tuning block

and the op-amp output voltage is also decreased, i.e., the offset voltage is reduced. As long as the comparater output doesn't change this procedure is repeated until the phase $\overline{P1}$ or $\overline{P3}$ is changed. If the comparater output goes to '0' before the phase is changed, then the zero crossing detector detects this change and set the count enable signal CE to '0' to prevent the op-amp output from oscillating. A change of the comparater output means that the op-amp output crosses zero, and the minimum offset is achieved. Thus, no further update of the bias voltage is required.

A simple R and 2R resistor ladder network is used for an 8-bit DAC. The resistor ladder is implemented by MOS transistors. One advantage of this simple structure is that the area is very small compared to other structures and increases linearly as the number of bits increases. In our application a DAC does not require excellent linearity or even monotonicity. Thus, the simple structure has been chosen from the area point of view. The simulated offset adjustable range of the designed op-amp is from -28mV to 68mV. Due to the nonlinearity of both the DAC and the programmable current mirror the simulated worst-case resolution is 0.57mV when the offset adjustable range is -28mV to $+30$mV, which is different from the theoretical resolution 0.38mV. The resolution can be easily improved by increasing the number of bits of the DAC and counters at the cost of only small area.

Conclusions

In this paper a digital offset correction method for a CMOS op-amp was presented. A programmable current mirror was used for controlling the offset voltage. A ping-pong structure was employed to obtain a 100% duty cycle. Simulated results show that the designed op-amp can be digitally adjusted to have an input offset voltage of less than 0.57mV with an adjustable range of -28mV to $+30$mV. The resolution can be readily improved by increasing the number of bits of the DAC and counters. It will cost only small additional area. The designed circuits will be fabricated soon using a $1\mu m$ process.

Referencess

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