An Inverting MOS Active Attenuator for Monolithic Applications

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ABSTRACT

A MOS active attenuator particularly useful in analog monolithic applications is presented. The attenuator has attractive characteristics including nearly infinite input impedance, low power consumption, small circuit area, low noise, low THD, and precisely controllable attenuation ratio over a wide range. In particular, this attenuator has offset adjustability that was not possible with the former attenuator investigated by the authors [1]. The analysis, design, and performance of the attenuator are discussed. An attenuator which has signal to THD ratio of 85.6 dB at 100 mV input voltage, maximum input swing of 0.7 V, dynamic range of 74.2 dB at 0.037% THD, and power dissipation of 99.6 μW for an attenuation ratio of 1:10 is readily designable with two transistors smaller than 100X24 μm^2.

I. Introduction

Voltage attenuators have useful applications in discrete as well as integrated analog circuits. Some of the applications are in data converters and in the input stages of transconductance amplifiers as well as in the feedback loops of feedback amplifiers. In discrete applications, voltage dividers consisting of resistors connected in series are widely used. However, the resistor attenuators are not very attractive in integrated circuits for several reasons. First, the area required to fabricate a resistor of sufficiently high resistance to have a practical input impedance is large. Second, the power dissipation is generally too high to be practical. Third, nonlinearities associated with diffused resistors are high. Finally, distributed parasitic capacitances may cause undesirable frequency dependence.

Active attenuators suitable for monolithic applications using two MOSFETs fabricated in seperate wells and in a common substrate have been investigated [1-4]. Those attenuators exhibited many attractive characteristics such as small size, nearly infinite input impedance, precisely controllable attenuation ratio, low power consumption, good linearity, and good noise and frequency characteristics, but they do not have offset adjustability. The attenuator presented here, originally proposed as an amplifier [5], has offset adjustability independent of attenuation ratio in addition to most of the merits of the former active attenuators. This attenuator can also be fabricated in a common substrate. This attenuator requires small area and makes it possible to fabricate both n-channel and p-channel attenuators monolithically in a standard CMOS process.

The principle of operation, harmonic distortion analysis, random noise analysis, and design and performance characterization including power consumption and size considerations of the attenuator are presented.

II. Operation Principle

Two variants of the active attenuator consisting of two n-channel MOSFETs are shown in Fig. 1. Each circuit is to operate as an inverting attenuator when both of the transistors are in the saturation region. This condition will be met provided

$$V_{TON2} < V_B , \tag{1}$$

and

$$V_{TON1} < V_I < V_O + V_{TON1} . \tag{2}$$

Under this condition, the drain currents of the transistors are given by

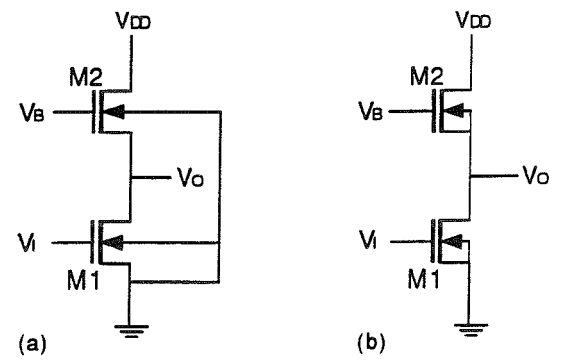

Fig. 1. The circuit diagrams of the active attenuators consisting of two n-channel MOSFETs.

$$I_{D1}=K'\frac{W_1}{2L_1}(V_I-V_{TON1})^2 , \quad (3)$$

and

$$I_{D2}=K'\frac{W_2}{2L_2}(V_B-V_O-V_{T2})^2 \quad (4)$$

where

$$V_{T2}=V_{TON2}+\gamma\left(\sqrt{\phi+V_O}-\sqrt{\phi}\right). \quad (5)$$

Because the two drain currents should be the same, the transfer characteristic relating V_I and V_O is obtained from Eq. (3-5). Assuming $V_{TON1}=V_{TON2}=V_{TON}$ (This will be assumed henceforce),

$$V_I=\frac{1}{R}V_B+\left(1-\frac{1}{R}\right)V_{TON}-\frac{1}{R}\left\{\gamma\left(\sqrt{\phi+V_O}-\sqrt{\phi}\right)+V_O\right\} \quad (6)$$

where

$$R=\sqrt{\frac{W_1/L_1}{W_2/L_2}} . \quad (7)$$

If $\gamma=0$ in Eq. (6) which is the case of the circuit (b) in Fig. (1), the equation (6) becomes linear. The dc transfer characteristics between V_I and V_O calculated from Eq. (6) within the range restricted by Inequality (2) for $\gamma=0.5255\ V^{1/2}$, $R=0.1149$, $V_B=3.9932$ V, $\phi=0.6$ V and $V_{TON}=0.777$ V, and for $\gamma=0$, $R=0.1$, $V_B=3.4493$ V and the same V_{TON} are shown in Fig. 2. Note that, the curve for $\gamma=0.5255V^{1/2}$ which is standard for 2μ p-well CMOS process coincides with the straight line for $\gamma=0$ within the accuracy of the figure, that is, the dc transfer characteristic of the attenuator given by Eq. (6) for $\gamma=0.5255V^{1/2}$ is still very linear while the equation itself is seemingly nonlinear. The high degree of linearity shown in Fig. 2 suggests applications in high performance applications. A more detailed analysis is in order to quantify the performance potential of the attenuator.

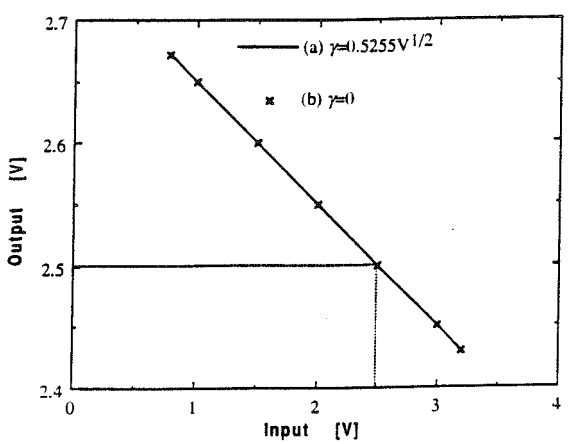

Fig. 2. dc transfer characteristics of the attenuators when (a) $\gamma=0.5255V^{1/2}$ and (b) $\gamma=0$.

In order to analyze the small signal attenuation factor and the harmonic distortion, the dc transfer characteristic given by Eq. (6) is expanded into Taylor's series about an operating point. For an input of $V_I=V_{IQ}+v_i$, the output, V_O, is expanded as

$$V_O=H(V_I)=V_{OQ}+H'(V_{OQ})v_i+\frac{1}{2}H''(V_{OQ})v_i^2+... \quad (8)$$

where $V_{OQ}=H(V_{IQ})$ is given from Eq. (6), and

$$H'(V_{OQ})=\left(\frac{dV_O}{dV_I}\right)_{V_{OQ}}\equiv\alpha=-R\left(\frac{\gamma}{2\sqrt{\phi+V_{OQ}}}+1\right)^{-1} \quad (9)$$

and

$$H''(V_{OQ})=\left(\frac{d^2V_O}{dV_I^2}\right)_{V_{OQ}}=R^2\frac{\gamma}{4}\left(\frac{\gamma}{2}+\sqrt{\phi+V_{OQ}}\right)^{-3}. \quad (10)$$

α defined by Eq. (9) is the small signal attenuation factor of the attenuator. Thus, once α and operating point are given for a desired attenuator, the necessary R for a given attenuation factor is determined using Eq. (9) and then the necessary V_B to make the dc transfer characteristic curve pass through the given operating point is determined using Eq. (6). If we want to have equal operating voltages for the input and output, and assuming $V_{IQ}=V_{OQ}>V_{TON}(2-\alpha)/(1-\alpha)$, then from Inequality (2) and Eq. (6), the maximum swing (Q-point to peak amplitude), A_{max}, for the input is approximately given by

$$A_{max}\cong\frac{V_{TON}}{1-\alpha} . \quad (11)$$

III. Harmonic Distortion Analysis

For $v_i=A\sin\omega t$, from Eq. (8), we obtain

$$V_O\cong h_0+h_1\sin\omega t+h_2\cos 2\omega t \quad (12)$$

where

$$h_0=V_{OQ}+\frac{1}{4}H''(V_{OQ})A^2, \quad (13)$$

$$h_1=H'(V_{OQ})A=\alpha A , \quad (14)$$

and

$$h_2=-\frac{1}{4}H''(V_{OQ})A^2. \quad (15)$$

In these expressions, h_0 is the total dc, h_1 is the "desired" ac signal, and h_2 is the 2nd harmonic component of the ouput of the attenuator. Thus, the signal to 2nd harmonic ratio of the output is given by

$$\frac{h_1}{h_2}=\frac{4\alpha}{H''A} \quad (16)$$

where A is the input amplitude, α is the attenuation factor, and H^* given by Eq. (10) depends on α through R and the operating point.

IV. Random Noise Analysis

A noise equivalent circuit of the attenuator based on noiseless transistors and output referred noise sources and the equivalent small signal circuits are shown in Fig. 3. At a given quiescent point, the gate-channel transconductance, g_{m2}, and the bulk-channel transconductance, g_{mb2}, of M2 are, from Eq. (4-5), given by

$$g_{m2}=\left(\frac{\partial I_{D2}}{\partial V_{GS2}}\right)_{V_{OQ}}$$

$$=K'\frac{W_2}{L_2}\left\{V_B-V_{TON}-V_{OQ}-\gamma\left(\sqrt{\phi+V_{OQ}}-\sqrt{\phi}\right)\right\} \quad (17)$$

and

$$g_{mb2}=\left(\frac{\partial I_{D2}}{\partial V_{BS2}}\right)_{V_{OQ}}=g_{m2}\frac{\gamma}{2\sqrt{\phi+V_{OQ}}}. \quad (18)$$

Since both M1 and M2 are in the saturation region, the respective noise current spectral density is given by

$$S_{I1}=S_{IT1}+S_{If1}=\left(4kT\right)\frac{2}{3}g_{m1}+\frac{2K_fK'I_{DQ1}}{C_{ox}L_1^2f}, \quad (19)$$

and

$$S_{I2}=S_{IT2}+S_{If2}=\left(4kT\right)\frac{2}{3}g_{m2}+\frac{2K_fK'I_{DQ2}}{C_{ox}L_2^2f} \quad (20)$$

where the transconductance of M1, g_{m1}, is, from Eq. (3), given by

$$g_{m1}=\left(\frac{\partial I_{D1}}{\partial V_{GS1}}\right)_{V_{IQ}}=K'\frac{W_1}{L_1}\left(V_{IQ}-V_{TON}\right). \quad (21)$$

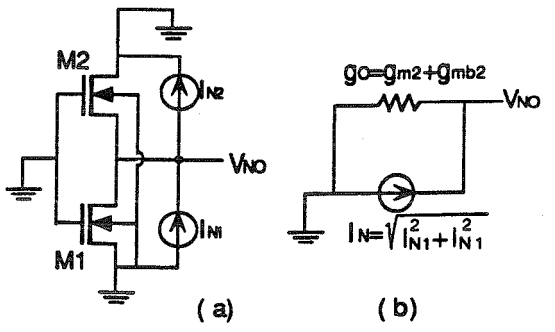

Fig. 3. (a) The noise equivalent circuit of the attenuator based on noiseless transistors and output noise sources. (b) The noise small signal equivalent circuit.

From Fig. 3 (b), the output noise voltage(rms), V_{NO}, is given by

$$V_{NO}=\frac{I_N}{gO}=\frac{\sqrt{I_{N1}^2+I_{N2}^2}}{g_{m2}+g_{mb2}}=\frac{\sqrt{\int_{f1}^{f2}S_{I1}+S_{I2}df}}{g_{m2}+g_{mb2}}. \quad (22)$$

Substituting Eq. (17-21) into Eq. (22), we obtain

$$V_{NO}=\left[\frac{L_2}{W_2}\left\{M+N\left(\frac{1}{L_1^2}+\frac{1}{L_2^2}\right)\right\}\right]^{\frac{1}{2}} \quad (23)$$

where M and N are functions of R, operating point, and noise band. Thus, once R required for a given attenuation factor is determined, and the desired operating point are given, using Eq. (17-23), we can calculate the output noise voltage(rms) for a given set of L_1, W_1, L_2, W_2, and a given noise band.

V. Design and Performance

Based on the analyses above, the design and performance of the attenuator for a given attenuation factor, α, and operating point are considered in this section. As an example for quantitative calculations, we will use the case where α=-0.1, $V_{IQ}=V_{OQ}=V_Q$ =2.5 V, and V_{DD}=5 V.

As explained in Section II, for a given α, first the necessary R is calculated using Eq. (9). For α=-0.1, and for γ=0.5255 $V^{1/2}$, ϕ=0.6 V and V_{TON}=0.777 V which are standard for 2μ p-well CMOS process, R=0.1149. Then using Eq. (6), the required V_B for a given operating point is calculated. V_B=3.9932 V for V_Q=2.5 V. Now, we can determine the harmonic distortion by calculating H^* given by Eq. (10). At the above conditions, $H^*=2.094\times10^{-4}$ V^{-1} and the signal to 2nd harmonic ratio of the output given by Eq. (16) is 85.6dB for 100 mV input amplitude.

Once R given by Eq. (7) is determined for a given α, the respective W_1, L_1, W_2, and L_2 can be designed for minimum output noise or for minimum power dissipation under the condition of Eq. (7) and within a given range of L and W. The output noise is related to L_1, W_2, and L_2 by Eq. (23) where M and N can be calculated when R, V_Q, and the noise frequency band are given. From Eq. (23), for minimum output noise, we set $L_1=W_2=L_{max}$, and $L_2=L_{2,opt}$ where $L_{2,opt}$ is given by

$$L_{2,opt}=\sqrt{\frac{N}{M+\frac{1}{L_1^2}N}}. \quad (24)$$

L_{max} [μm]	(a) Optimized for minimum V_{NO}				(b) Optimized for minimum power			
	W_1[μW] L_1 [μW]	W_2 [μW] L_2 [μW]	V_{NO}[V_{rms}]	P_d [μW]	W_1[μW] L_1 [μW]	W_2 [μW] L_2 [μW]	V_{NO}[V_{rms}]	P_d [μW]
10	0.2709 10	10 4.876	3.25E-5	11.4	2 10	10 0.6604	6.30E-5	84.1
100	23.69 100	100 5.576	9.61E-6	99.6	2 100	100 66.04	2.35E-5	8.41
1000	2365 1000	1000 5.585	3.04E-6	994	2 1000	151.4 1000	7.38E-5	0.841
10000	226500 10000	10000 5.585	9.60E-7	9940	2 10000	151.4 10000	2.34E-4	0.0841

Table 1. The sizes of the transistors, the output noise voltages, V_{NO}, and the power dissipations, P_d, of the optimally designed attenuators with respect to (a) the output noise and (b) the power dissipation. α=-0.1 V_Q=2.5 V, V_{DD}=5 V, and W_{min}=2 μm

The remaining W_1 is now calculated such that Eq. (7) is satisfied.

The power dissipation of the attenuator, P_d, is given by $P_d=I_{D1}XV_{DD}$ where I_{D1} is given by Eq. (3). If we now want to minimize the power dissipation, from Eq. (3), we need to minimize W_1/L_1. Thus, we set $W_1=W_{min}$, and $L_1=L_{max}$ for minimum power dissipation. Then the remaining W_2 and L_2 should be chosen such that Eq. (7) is satisfied.

The designed sizes of the transistors, and output noise and power dissipation of the attenuator when it is optimized (a) for minimum output noise and (b) for minimum power dissipation as described above at the conditions used earlier in this section and for W_{min}=2 μm and a set of L_{max} are shown in Table 1. As an example of the design for minimum output noise, let's consider the case of L_{max}=100 μm. We first set $L_1=W_2$=100 μm, and then calculate L_2 using Eq. (24). At the same conditions as used earlier in this section, and for $K'=5.663X10^{-10}$ A/V^2, $C_{ox}=8.125X10^{-4}$ F/m^2, $K_f=3X10^{-24}$ V^{2}F which are also standard for 2μm CMOS process, and for f_1=100 Hz, f_2=1MHz, and T=298°K, then from Eq. (17-23), $M=8.2560X10^{-10}$ V^2 and $N=2.5752X10^{-20}$ V^{2}m^2. Then, from Eq. (24), L_2=5.576 μm. The remaining W_1 is calculated to match the required R value and, in this case, W_1=23.69 μm. From Eq. (23) and $P_d=I_{D1}XV_{DD}$ where I_{D1} is given by Eq. (3), the attenuator consisting of the transistors of these sizes has output noise, V_{NO}, of $9.61X10^{-6}$ V_{rms} and power dissipation, P_d, of 99.6 μW.

For α=-0.1 and V_{TON}=0.777 V, the maximum applicable input amplitude, A_{max}, given by Eq. (11) is approximately 0.7 V. At that maximum input and output noise voltage of $9.61X10^{-6}$ V_{rms}, the dynamic range, DR, which is output signal to random noise ratio is 74.2 dB and the signal to THD ratio given by Eq. (16) is 0.037 % (68.7 dB).

VI. Conclusion

The operation principle, harmonic distortion and random noise analyses of an active voltage attenuator suitable for monolithic applications have been investigated. The design schemes of the attenuator for minimum output noise and for minimum power dissipation within a given range for the sizes of the transistors comprising the attenuator have been presented. Quantitative calculations at a given set of operating conditions showed that an attractive attenuator having signal to THD ratio of 85.6 dB at 100 mV input voltage, maximum input swing of 0.7 V, dynamic range of 74.2 dB at 0.037 % (68.7 dB) THD, and power consumption of 99.6 μW for an attenuation ratio of 1:10 was readily designable with two transistors smaller than 100X24 μm^2. The attenuator presented here has offset adjustability as well as precisely controllable attenuation ratio over a wide range of attenuation factors and large maximum input swing which makes it very attractive in many applications, particularly in the feedback loops of feedback amplifiers. Together with the noninverting attenuators investigated by the authors before, this attenuator forms a useful set of attenuators for analog integrated circuit applications.

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