Accurate Testing of Analog-to-Digital Converters Using Low Linearity Signals With Stimulus Error Identification and Removal

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***Abstract*—Linearity testing of analog-to-digital converters (ADCs) can be very challenging because it requires a signal generator substantially more linear than the ADC under test. This paper introduces the stimulus error identification and removal (SEIR) method for accurately testing ADC linearity using signal generators that may be significantly less linear than the device under test. In the SEIR approach, two imprecise nonlinear but functionally related excitations are applied to the ADC input to obtain two sets of ADC output data. The SEIR algorithm then uses the redundant information from the two sets of data to accurately identify the nonlinearity errors in the stimuli. The algorithm then removes the stimulus error from the ADC output data, allowing the ADC nonlinearity to be accurately measured. For a high resolution ADC, the total computation time of the SEIR algorithm is significantly less than the data acquisition time and therefore does not contribute to testing time. The new approach was experimentally validated on production test hardware with a commercial 16-bit successive approximation ADC. Integral nonlinearity test results that are well within the device specification of ± 2 least significant bits were obtained by using 7-bit linear input signals. This approach provides an enabling technology for cost-effective full-code testing of high precision ADCs in production test and for potential cost-effective chip-level implementation of a built-in self-test capability.**

***Index Terms*—Analog-to-digital converters (ADCs), integral nonlinearity (INL), linearity test, stimulus error identification and removal (SEIR).**

I. Background

THE "histogram method" is a standard approach for quasi-static linearity testing of analog-to-digital converters (ADCs) [1]–[3]. However, during the past decade, linearity testing of ADCs has not received much research attention for several reasons. As long as best practices are followed, modern mixed-signal automated test equipment (ATE) can be used to make quasi-static linearity testing of ADCs a fairly straightforward production task for low-to-medium resolution ADCs [4]. High-precision delta-sigma ADCs are inherently sufficiently linear and do not require linearity testing. In the communications circuit area, high-speed pipelined ADCs are widely used and are usually production tested with high-frequency input signals [2], whereas quasi-static linearity testing is primarily used for debugging [5] or calibration [6]. Probably the biggest reason, however, can be attributed to the challenges associated with generating highly linear or spectrally pure test signals with no major technological breakthroughs occurring in this area in the past decade.

Nevertheless, quasi-static linearity testing remains a test challenge for the production of certain classes of high performance ADCs, and the increasing downward production cost pressures are making the convenient use of expensive mixed-signal ATEs for testing low and medium resolution ADCs more difficult to justify. In this paper, emphasis will be placed on the more challenging task of quasi-static linearity testing of high performance ADCs with little mention of the low and medium resolution devices, but application of the concepts introduced here for the production testing of low and medium resolution devices is straightforward and in some applications may provide a more cost-effective test flow for low and medium resolution devices that does not require time on expensive mixed signal ATEs.

In a high performance ADC, specifications like 16-bit or higher resolution, 1 MSPS or higher conversion rate, little or no output latency, and an input signal frequency exceeding the ADCs Nyquist rate are common. Recent examples include 16-bit 1.25 MSPS and 18-bit 500 KSPS successive approximation register (SAR) ADCs and a 16-bit 5 MSPS multibit delta-sigma ADC [7]. These ADCs employ techniques such as precision laser trimming or dynamic element matching to achieve high linearity at relatively high sampling speeds. These high performance ADCs are typically used in medical applications including ultrasound and computer aided tomography as well as precision industrial process control and ATEs that serve the testing industry.

To better appreciate the challenges in quasi-static linearity testing of high precision ADCs, the performance requirements on the signal sources used to generate the input to the ADC under test will be reviewed. Conventional wisdom dictates that signal sources must be significantly more linear than the ADC under test. Usually, an acceptable test procedure would provide test accuracy to within 10% of the device specification. An ADC with a ± 2 least significant bit (LSB) maximum linearity error specification would require test accuracy to be well within ± 0.2 LSB. Considering that one LSB is around 76 μV for a 16-bit ADC with a 5 V supply, source linearity of better than 15.2 μV (0.2 LSB) is required and providing this degree of source linearity is an extremely challenging task. The task is even more

Manuscript received September 11, 2003; revised November 4, 2004.

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Digital Object Identifier 10.1109/TIM.2005.847240

challenging when testing an 18-bit ADC. Some applications dictate that all codes of the ADC be tested in production, resulting in long test times that often run several minutes on an expensive mixed signal ATE. The long test time is usually required to average out the effects of input noise in the test environment. However, requiring the source to remain stationary (low drift) during such long tests presents another challenge for linearity testing. Source architectures used in ATE equipment that provide good linearity, like the delta-sigma structures, are not known for good drift performance, and vice versa. In addition, linear sources often have slow settling characteristics, and the source settling often dominates acquisition and test time. Practical test solutions for future high precision ADCs require a relaxation of the performance requirements on the signal source, an apparent paradoxical expectation.

II. Introduction

In this paper, a new approach for ADC testing is developed that relaxes the requirement on source linearity. If the source is allowed to be nonlinear with no stringent requirements on the specific linearity characteristics and no need for prior knowledge on the characteristics of the nonlinearity, the design requirements for the source will be dramatically reduced. Such sources can be designed to have better drift characteristics and to work faster, properties which are key to improving accuracy and reducing ADC test time. Furthermore, such nonlinear sources can be placed on the device interface board (DIB) to reduce requirements and cost of the ATE or even incorporated on chip with a small die area to facilitate use in a design for test (DFT) or a built-in self-test (BIST) environment. Recent research using the concept of using nonlinear excitations for ADC testing can be found in [8], [9], [11]–[13], and [15]–[17]. As a proof of concept, two different approaches were discussed in the authors' previous work [8]. One of these approaches was sensitive to device noise, making applications to precision ADCs difficult. The second included an algorithm that requires a matrix inversion with computational complexity proportional to the cube of the total number of ADC output codes, which is not computationally effective for high-resolution ADCs. With both algorithms, low-spatial-frequency nonlinearities in the signal source, a property that can be readily attained, were assumed. An application of one of these algorithms to testing 10-bit ADCs is reported in [9]. Ten-bit resolution appeared to be a practical performance limit on the specific algorithm used in the previous work.

This paper presents the stimulus error identification and removal (SEIR) method for accurate and robust testing of ADC quasi-static linearity performance. The SEIR approach uses two imprecise nonlinear signals, one shifted with respect to the other by a constant voltage offset, to excite the ADC and obtain two sets of ADC outputs. By matching the signal levels corresponding to the same ADC transition level, a set of equations involving only the stimulus error components is established. This separates the signal source nonlinearity from the nonlinearity inherent in the ADC under test. By parameterizing the signal source nonlinearity using a set of basis functions, a set of equations linear in the parameterization coefficients are obtained. Standard least square (LS) methods can then be used to accurately identify the coefficients and thus identify the nonlinearity errors in the stimuli. The SEIR algorithm subsequently removes the stimulus error from the ADC output data, allowing the ADC nonlinearity to be accurately measured.

Both simulation results and experimental test results obtained from commercially available ADCs are presented. Experimental results confirm the fact that the identification and removal of the effects of input nonlinearity can be performed as a digital signal-processing task during production by a tester computer with reasonably short time. Production test hardware typically used for high performance 16-bit SAR ADCs, which is a real challenge in the analog and mixed-signal linearity testing area, has been used to verify the method. Full code testing results from this new method are successfully correlated with those obtained in an industry laboratory using state of the art production test equipment for mixed-signal circuits. The test time required for implementation of the proposed testing approach is short, making it viable for use in a production test environment.

III. ADC Linearity Testing Using Nonideal Stimuli

In this section, a mathematical formulation of the SEIR algorithm will be presented. First, the modeling of an ADC based on transition levels [18] and the nonlinear input signals along with the definition of transition times are presented. This is followed by a discussion on integral nonlinearity testing. Finally, a mathematical formulation that is used to estimate and remove the effects of input nonlinearity is given and a new ADC characterization approach using nonlinear input signals is described.

A. ADC and Input Nonlinearity Modeling

Let us consider an n-bit ADC with $N = 2^n$ output codes. The static input–output characteristic of such a device can be modeled as

$$D(x) = \begin{cases} 0, & x \le T_0 \\ k, & T_{k-1} < x \le T_k, k = 1,2 \ldots N-2 \\ N-1, & T_{N-2} < x \end{cases} \quad (1)$$

where D is the digital output code, x is the analog input voltage, and T_k, $k = 0, 1, \ldots, N-2$ are transition levels of the ADC. If the input signal voltage is less than T_k, the output digital code will be less than or equal to k. If the input signal voltage is larger then T_k, the output digital code will be greater than k. Although the transition levels are generally indexed from 1 to $N-1$, we use indexes 0 to $N-2$ to number them in this paper. This will make it a bit easier for us to give definitions of some other terms later. The choice of indexes does not change the meaning of the transition levels. Equation (1) is valid under the assumption that the ADC is monotonic and has no missing codes. This assumption is justifiable for most commercial ADCs.

Linearity testing of an ADC corresponds to investigating how linearly transition levels of an ADC are distributed. An ideally linear ADC with the same terminal transition levels T_0 and T_{N-2} has transition levels uniformly spaced between T_0 and T_{N-2} with a constant voltage increment of $Q = (T_{N-2} - T_0)/(N-2)$. This increment is called an LSB. Transition levels

of the ideally linear ADC are called terminal-based ideal transition levels and denoted as I_k. They can be expressed as

$$I_k = T_0 + \frac{T_{N-2} - T_0}{N-2}k, \quad k = 0, 1 \ldots N-2. \tag{2}$$

Equation (2) is called a terminal-based fit line. It represents a straight line connecting the terminal transition levels of the ADC. For linearity testing, true transition levels of an ADC will be compared to the corresponding terminal-based ideal transition levels. The terminal-based integral nonlinearity for code k (INL_k) is defined to be the difference between the true and terminal-based ideal transition levels. Expressing INL_k in LSB, we obtain

$$\mathrm{INL}_k = \frac{T_k - I_k}{Q} = \frac{T_k - T_0}{T_{N-2} - T_0}(N-2) - k(\mathrm{LSB}), \quad k = 1, 2 \ldots, N-3. \tag{3}$$

The overall terminal-based INL is then defined by the expression

$$\mathrm{INL} = \max_k \{|\mathrm{INL}_k|\}. \tag{4}$$

A larger value of terminal-based INL indicates that an ADC has higher nonlinearity. For simplicity the word "terminal-based" will not be carried in the following part of this paper, but all the nonlinear parameters INL and INL_k used in this paper are based on the terminal transition levels and the corresponding terminal-based ideal transition levels.

An ideal ramp signal, as assumed in traditional linearity testing, can be visualized as a signal that increases linearly with time t, whereas a more realistic ramp signal always has some nonlinearity that makes it deviate from a straight line. A real ramp signal can be modeled as

$$x(t) = x_{os} + \eta t + F(t) \tag{5}$$

where x_{os} is a dc offset voltage, ηt is the linear part of the signal, and $F(t)$ is the nonlinear component. Defining the transition time t_k to be the time at which the value of the analog ramp signal is equal to the kth transition level of the ADC, we obtain

$$T_k = x(t_k), \quad k = 0, 1 \ldots, N-2. \tag{6}$$

Monotonicity of the signal source is assumed in this paper, and hence the output codes sampled before time t_k will be always less than or equal to k. Effects of the noise in the input signal will be discussed in Section IV. To simplify the derivation, we perform some linear operations on (5) which will not affect the final test results. First, we denote the first transition time to be the origin of time scale, i.e., $t_0 = 0$. Secondly, we normalize the time intervals so that the last transition time corresponds to the unit time, i.e., $t_{N-2} = 1$. By doing so, we have scaled and translated the time axis to be unit free so that our algorithm will look the same for all clock frequencies and will be independent of the actual time when tests are conducted. The linear component ηt of the signal is defined such that the nonlinearity in the input signal is zero at both $t = 0$ and $t = 1$, that is

$$F(0) = F(1) = 0. \tag{7}$$

These operations are equivalent to choosing

$$x_{os} = T_0 \quad \text{and} \quad \eta = T_{N-2} - T_0. \tag{8}$$

Substituting (8) into (5), we obtain

$$x(t) = T_o + (T_{N-2} - T_0)t + F(t), \quad 0 \le t \le 1. \tag{9}$$

Equation (9) represents a signal whose magnitude is equivalent to the first and last transition levels of the ADC at the normalized times 0 and 1, respectively. With this notation, the nonlinearity of the input signal is completely characterized by $F(t)$.

Assuming no prior knowledge about the general form of $F(t)$, we try to identify this input nonlinearity independently during the test. As a first step, we expand $F(t)$ over a complete set of basis functions denoted by $\{F_j(t), j = 1, 2, 3, \ldots\}$. By identifying a finite number of the major coefficients of the basis functions for this expansion, we can estimate the value of $F(t)$ to an accuracy higher than the resolution of the ADC under test. To simplify the derivation, we choose familiar and widely used trigonometric functions on $[-1, 1]$ to be the set of basis functions. Applying odd extension on $F(t)$ to cover the interval $[-1, 1]$, which includes a mathematically negative time, we obtain

$$\widetilde{F}(t) = \begin{cases} F(t), & 0 \le t \le 1 \\ -F(-t), & -1 \le t < 0. \end{cases} \tag{10}$$

$\widetilde{F}(t)$ can be expanded in terms of trigonometric functions as

$$\widetilde{F}(t) = \sum_{j=1,2\ldots} a_j \sin(j\pi t) + \sum_{j=0,1\ldots} b_j \cos(j\pi t), \quad -1 \le t \le 1 \tag{11}$$

where a_j, $j = 1, 2, \ldots$, and b_j, $j = 0, 1, 2, \ldots$, are the coefficients of the jth harmonic. Since the extended function is odd, the coefficients of the cosine functions are all zero and only sine functions are needed to express the nonlinearity. On $[0, 1]$, $F(t)$ can thus be parameterized as

$$F(t) = \sum_{j=1}^{M} a_j \sin(j\pi t) + e(t). \tag{12}$$

Since we are only interested in a finite accuracy expansion of $F(t)$, only the first M basis functions are included in (12) and thus $e(t)$ is the residue of the nonlinearity that is not modeled by the M basis functions. By completeness of the basis function set, M can always be appropriately chosen so that the residue is small to any desired level. $F(t)$ is said to be identified if we can determine the value of a_j, $j = 1, 2, \ldots, M$. For simplicity, we will not carry the term $e(t)$ most of the time in the following derivations. The effect of neglecting the term $e(t)$ will be analyzed in Section IV. Other choices for a set of basis functions $\{F_j(t), j = 1, 2, 3, \ldots\}$ can also be used to approximate $F(t)$,

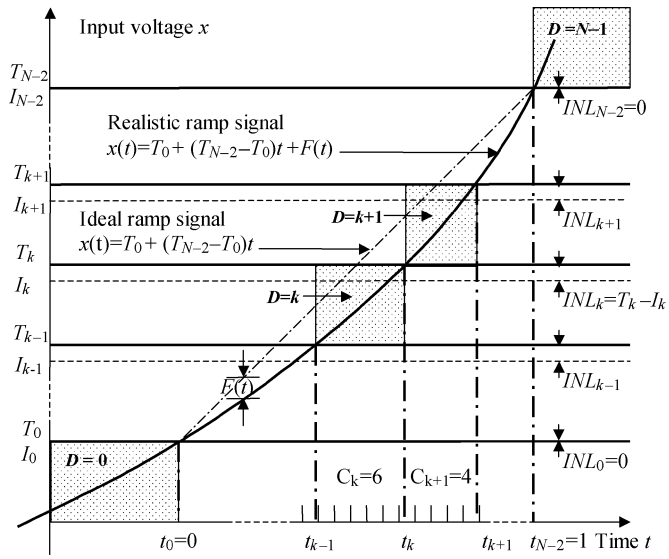

Fig. 1. Basic terminology in ADC linearity testing.

and each element of the set should vanish at $t = 0$ and $t = 1$. Formally, they will satisfy the relationships

$$\begin{aligned} F(t) &\cong \sum_{j=1}^{M} a_j F_j(t), \quad 0 \le t \le 1 \\ F_j(0) &= F_j(1) = 0, \quad j = 1, 2 \ldots M. \end{aligned} \tag{13}$$

An example of an alternative set of basis functions is the set of polynomial functions

$$\begin{aligned} F_1(t) &= t(t-1) \\ F_2(t) &= t(t-1)(t-0.5) \\ F_3(t) &= t(t-1)(t-0.5)(t-0.25) \\ F_4(t) &= t(t-1)(t-0.5)(t-0.25)(t-0.75) \\ &\ldots . \end{aligned} \tag{14}$$

Using the expanded nonlinear component, the input signal can be written as

$$x(t) \cong T_o + (T_{N-2} - T_0)t + \sum_{j=1}^{M} a_j F_j(t), \quad 0 \le t \le 1. \tag{15}$$

Fig. 1 illustrates the relationships between the true and terminal-based fit line transition levels, the input and output of an ADC, and the ideal and a realistic ramp signal. The horizontal axis corresponds to time with transition time points labeled. The vertical axis corresponds to the input voltage with transition levels labeled. The region corresponding to different output codes are denoted as dotted areas. The output code of an ADC will be a digital code k when time is between transition times t_{k-1} and t_k and correspondingly the input signal value is between the transition levels $T_{k-1} = x(t_{k-1})$ and $T_k = x(t_k)$.

B. Linearity Testing for ADCs

The goal of ADC linearity testing is to identify transition levels and determine the INL of an ADC. However, transition levels of an ADC cannot be measured directly from the ADC output. An alternative is to measure transition times and calculate the values of transition levels by using (6). Substituting (15) into (6), we have

$$T_k \cong T_o + (T_{N-2} - T_0)t_k + \sum_{j=1}^{M} a_j F_j(t_k), \quad 0 \le t_k \le 1. \tag{16}$$

Equation (3) can then be used to express INL_k as a function of the associated transition time and coefficients of the nonlinear component a_j

$$\mathrm{INL}_k \cong (N-2)t_k + \sum_{j=1}^{M} a_j F_j(t_k) - k, \quad k = 1, 2, \ldots, N-3. \tag{17}$$

In (17), coefficient a_j is in terms of LSBs.

Transition times of an ADC can be measured by using the traditional histogram test. Let C_k, $k = 0, 1, 2, \ldots, N-1$, represent the bin counts obtained in a histogram test for each code. If the sampling period of an ADC is a constant, the time when a sample is taken is linearly proportional to the number of samples that have been taken so far. So the number of samples can be viewed as a measurement of time. For instance, C_1 samples of code 1 will have been taken since $t = 0$ when the output code changes from 1 to 2, indicating that C_1 sampling periods of time have elapsed. Similarly, $C_1 + C_2$ samples will have been taken when the output code changes from 2 to 3. In general, $C_1 + C_2 + \cdots + C_k$ sampling periods of time will have elapsed since $t = 0$ when the output code changes from k to $k+1$. This leads to the following time instances:

$$\hat{t}_k = T_c \sum_{i=1}^{k} C_i, \quad k = 1, 2, \ldots, N-2 \tag{18}$$

where T_c is a scaling factor that scales the time period measured in terms of the number of samples to the normalized time defined earlier. Since the output code changes from $N-2$ to $N-1$ when $t = 1$, the total number of samples taken between $t = 0$ and $t = 1$ is given by

$$C_1 + C_2 + \ldots + C_{N-2} = \sum_{i=1}^{N-2} C_i. \tag{19}$$

Therefore an appropriate scaling factor is given by

$$T_c = \left(\sum_{i=1}^{N-2} C_i \right)^{-1}. \tag{20}$$

Since by definition $\hat{t}_k$ is the last sampling instance before the output code changes from k to $k+1$, we have

$$x(\hat{t}_k) \le T_k \quad \text{and} \quad T_k < x(\hat{t}_k + T_c). \tag{21}$$

Since $x(t)$ is assumed to be a monotonically increasing function of time, we have

$$\hat{t}_k \le t_k < \hat{t}_k + T_c. \tag{22}$$

Thus estimating the kth transition time using the time instance defined in (18) involves an uncertainty of at most one clock period as shown in (22). The magnitude of this uncertainty can be

reduced by increasing the number of samples taken so that T_c is sufficiently small. In such a case, it is safe to assume that the approximation error is insignificant and

$$t_k \cong \hat{t}_k = T_c \sum_{i=1}^{k} C_i. \tag{23}$$

Substituting (20) into (23), we have

$$\hat{t}_k = \frac{\sum_{i=1}^{k} C_i}{\sum_{i=1}^{N-2} C_i}. \tag{24}$$

Using (17), we have an estimate for INL_k

$$\hat{\mathrm{INL}}_k = (N-2)\hat{t}_k + \sum_{j=1}^{M} a_j F_j(\hat{t}_k) - k, \quad k = 1, 2, \ldots, N-3. \tag{25}$$

If input nonlinearity were known in a parameterized form, (24) and (25) would relate the bin counts C_k to the INL_ks of an ADC. However, input nonlinearity is typically not known beforehand and cannot be determined from (25). Equation (25) comprises a set of $N-3$ linear equations in the $N-3$ INL_k values and the M nonlinearity coefficients representing a total of $N+M-3$ unknowns. Thus the set of equations given in (25) are, in general, insufficient to solve for all of the unknowns. The traditional histogram method for determining $I\hat{N}L_k$ is a special case of the situation above for which the input signal is assumed to be ideally linear so that all $a_j = 0$ and (25) can be simplified to

$$\hat{\mathrm{INL}}_k = (N-2)\hat{t}_k - k, \quad k = 1, 2, \ldots, N-3. \tag{26}$$

The assumption is good only when the maximum input nonlinearity is much smaller than 1 LSB. However, if the input nonlinearity is comparable to or larger than 1 LSB, it will introduce significant errors in the INL_k estimation if (26) is used to estimate the INL_k. The estimation error can be obtained by subtracting (26) from (17) and is given as

$$\hat{\mathrm{INL}}_k - \mathrm{INL}_k = -\sum_{j=1}^{M} a_j F_j(\hat{t}_k) + d(\hat{t}_k - t_k), \ k = 1, 2, \ldots, N-3. \tag{27}$$

The first term on the right-hand side of (27) is the result of input nonlinearity and the second term comes from the errors in transition time approximation. The input nonlinearity gets included in the estimated values of INL_k. This will result in misinterpretation of the true linearity performance of an ADC if neglected. For example, if we use an input source with 10-bit linearity to test a 16-bit ADC with a true 1-LSB INL, (26) will estimate the ADC to have about 64-LSB INL. The second term in (27), $d(\hat{t}_k - t_k)$, is the effect of quantization error in the transition time. However, with a reasonable number of samples per code, this error is usually a small fraction of 1 LSB and much smaller than the error caused by the input nonlinearity. The effects of the above terms will be discussed in detail in Section IV.

C. ADC Linearity Testing With Multiple Nonlinear Stimuli

In (25), nonlinearities from the ADC and from the input signal are coupled with each other and the task of identifying them simultaneously is not apparently doable. One possible approach toward solving this problem is to separate and identify the input nonlinearity first and then test the ADC linearity performance with that knowledge. The SEIR approach involves testing the ADC with two input signals. The two signals are otherwise identical except an unknown but fixed offset α between them. Following the form of (9), the two input signals can be expressed as

$$x_1(t) = T_0 + (T_{N-2} - T_0)t + F(t) \tag{28}$$

$$x_2(t) = T_0 + (T_{N-2} - T_0)t + F(t) - \alpha. \tag{29}$$

The linear and nonlinear components in the two signals are the same with the only difference being the dc offset voltage. As described earlier for a single input case, each of the two input signals can define a set of transition times as in (6)

$$T_k = x_1\left(t_k^{(1)}\right) \tag{30}$$

$$T_k = x_2\left(t_k^{(2)}\right). \tag{31}$$

Since the two signals are used to test the same ADC, the transition levels referred to in (30) are the same as those referred to in (31). However, the two sets of transition times are different because of the offset change and have been denoted differently with superscripts 1 and 2, respectively. For example, if α is positive, it will take a longer time for the second signal to reach a transition voltage than it will take for the first signal to reach the same transition voltage, i.e., $t_k^{(1)} < t_k^{(2)}$. If we equate the right-hand sides of (30) and (31) with respect to the same transition level, the ADC nonlinearity, which is embodied by the transition levels T_k, will disappear, and we will get equations involving only the input nonlinearity. These equations can be used to identify the input nonlinearity.

Let $C_k^{(1)}$ and $C_k^{(2)}$, $k = 0, 1, \ldots, N-2$, be the histogram data collected by using x_1 and x_2 as inputs to the ADC, respectively. Transition times can be estimated by using the bin counts as in (24)

$$\hat{t}_k^{(1)} = \frac{\sum_{i=1}^{k} C_i^{(1)}}{\sum_{i=1}^{N-2} C_i^{(1)}}, \ k = 1, 2, \ldots, N-2 \tag{32}$$

$$\hat{t}_k^{(2)} = \frac{\left[\sum_{i=1}^{k} C_i^{(2)} - \left(C_0^{(1)} - C_0^{(2)}\right)\right]}{\sum_{i=1}^{N-2} C_i^{(1)}}, \ k = 0, 1 \ldots N-2. \tag{33}$$

In order for the two sets of transition times to have the same unit, both (32) and (33) are scaled and shifted by the same scaling factor and offset amount that are defined for the first signal, with origin at $\hat{t}_0^{(1)} = 0$ and unit time at $\hat{t}_{N-2}^{(1)} = 1$. The second signal having an offset in time is compensated in the numerator

to resolve this issue as in (33). Similar to (25), we can then estimate the INL_k values using the estimated transition times

$$\hat{\mathrm{INL}}_{\mathrm{k}}^{(1)} = (N-2)\hat{t}_k^{(1)} + \sum_{j=1}^{M} a_j F_j\left(\hat{t}_k^{(1)}\right) - k, \quad k = 1,2,\ldots,N-3 \tag{34}$$

$$\hat{\mathrm{INL}}_k^{(2)} = (N-2)\hat{t}_k^{(2)} + \sum_{j=1}^{M} a_j F_j\left(\hat{t}_k^{(2)}\right) - \alpha - k, \quad k = 1,2,\ldots,N-3, \quad \hat{t}_k^{(2)} \le 1. \tag{35}$$

Notice that in (34) and (35), we only included those INL_k estimates for which the corresponding transition times are within the domain of definition for the basis functions. Because of this, the total number of equations available is $N-3$ in (34) and $N-3-\alpha$ in (35) if $\alpha > 0$ (this is assumed below). It will be shown that for reasonable offset values, this reduction in the number of equations will not affect the performance of the proposed method.

Equations (34) and (35) constitute the body of the SEIR algorithm. As discussed earlier, we have a total of $N+M-2$ unknowns. They are $N-3$ INL_ks, Ma_js, and the unknown offset α. However, since two related input signals are used to test the ADC, we have $2(N-3)-\alpha$ linear equations, nearly doubling of the number of unknowns. We are thus left with many more equations in (34) and (35) than the number of unknowns. Since INL_ks in both equations are for the same ADC and must be equal at the same index k, by equating the individual INL_ks in (34) and (35), we obtain a set of equations involving only input nonlinearity in a linear parameterization form

$$(N-2)\hat{t}_k^{(1)} + \sum_{j=1}^{M} a_j F_j\left(\hat{t}_k^{(1)}\right) = (N-2)\hat{t}_k^{(2)} + \sum_{j=1}^{M} a_j F_j\left(\hat{t}_k^{(2)}\right) - \alpha \ldots. \tag{36}$$

Moving all the known terms to the left-hand side and all terms with unknowns to the right-hand side, we obtain

$$(N-2)\left(\hat{t}_k^{(2)} - \hat{t}_k^{(1)}\right) = \sum_{j=1}^{M} a_j\left(F_j\left(\hat{t}_k^{(1)}\right) - F_j\left(\hat{t}_k^{(2)}\right)\right) + \alpha, \quad k = 1,2,\ldots,N-3, \quad \hat{t}_k^{(2)} \le 1. \tag{37}$$

For testing high resolution ADCs, typical values of M and α (in LSB) are much smaller than N. Thus the number of equations in (37), $N-3-\alpha$, is much larger than $M+1$, the number of unknowns a_j, $j = 1,2,\ldots,M$, and α. When the number of equations is larger than the number of unknown parameters, the system of equations comprising (37) is overconstrained and the unknowns can be estimated by using the LS method. For example, an ADC with more than 10-bit resolution will always have thousands of output codes while the number of parameters needed to model the nonlinearity in the excitation is usually less than 20, as we will discuss later. The LS method has an attractive property of effectively averaging out the noise or errors in (37). The LS solution for estimating the unknowns can be expressed as

$$\{\hat{a}_1, \hat{a}_2, \ldots, \hat{a}_M, \hat{\alpha}\} = \arg\min\left\{\sum_{k=1,\hat{t}_k^{(2)}\le 1}^{N-3}\left((N-2)\left(\hat{t}_k^{(2)} - \hat{t}_k^{(1)}\right) - \left[\sum_{j=1}^{M} a_j\left(F_j\left(\hat{t}_k^{(1)}\right) - F_j\left(\hat{t}_k^{(2)}\right)\right) + \alpha\right]\right)^2\right\}. \tag{38}$$

Once the input nonlinearity is identified from (38), ADC linearity testing becomes a straightforward job. Substituting solutions from (38) into either (34) or (35) or their combination, we can estimate the INL_k of an ADC. Using (34), for example, we have

$$\hat{\mathrm{INL}}_k = (N-2)\hat{t}_k^{(1)} + \sum_{j=1}^{M} \hat{a}_j F_j\left(\hat{t}_k^{(1)}\right) - k, \quad k = 1,2,\ldots,N-3. \tag{39}$$

Equation (39) shows that the linearity performance of an ADC can be tested without being affected by input nonlinearity.

IV. Error Analysis

There are several sources of errors that will affect the performance of the SEIR approach. Among them, additive noise at the input to an ADC, the unmodeled error of the input signal nonlinearity as in (12), and the quantization error of transition times as in (27) have the most significant effects on the linearity testing results. Using the first signal as an example and considering the effects of noise and errors, the relationship between transition levels and the estimated transition time can be written as

$$T_k = T_o + (T_{N-2} - T_0)\hat{t}_k^{(1)} + \sum_{j=1}^{M} a_j F_j\left(\hat{t}_k^{(1)}\right) + e\left(\hat{t}_k^{(1)}\right) + n\left(\hat{t}_k^{(1)}\right) + d\left(\hat{t}_k^{(1)} - t_k^{(1)}\right) \tag{40}$$

where $e(\hat{t}_k^{(1)})$ is the unmodeled error, $n(\hat{t}_k^{(1)})$ is from the additive noise, and $d(\hat{t}_k^{(1)} - t_k^{(1)})$ is from the quantization error in transition times. Without specific mention, we assume in the following part of this section that these noise and errors will not affect the LS estimation for $\hat{a}_j$s such that they can be assumed to be the same as a_js. This is a fair assumption based on the following justifications. First, by definition, the unmodeled error is orthogonal to the first M sinusoidal functions. Secondly, the additive noise and quantization error usually change very fast as a function of time and hence have little correlation to the first M low frequency basis functions. Third, the LS method has the ability to average out the effects of noise and errors. Therefore the error between the true INL_k and that calculated in (39) can be written as

$$e_{\mathrm{INL}_k} = \mathrm{INL}_k - \hat{\mathrm{INL}}_k = e\left(\hat{t}_k^{(1)}\right) + n\left(\hat{t}_k^{(1)}\right) + d\left(\hat{t}_k^{(1)} - t_k^{(1)}\right). \tag{41}$$

If there is no systematic error in the measurement process, all the errors can be assumed to be from normal distributions with zero mean and the estimation of INL_k is unbiased

$$E\{e_{\mathrm{INL}_k}\} \approx 0. \tag{42}$$

The variance of the error in the INL_k estimation can then be determined from (41), which is the summation of the variance of the unmodeled error, the variance of noise effects, and that of the quantization effects

$$\mathrm{Var}\{e_{\mathrm{INL}_k}\} = \sigma_e^2 + \sigma_n^2 + \sigma_d^2. \tag{43}$$

The three types of error sources will be further discussed in the following sections.

A. Effects of the Unmodeled Error in Input Signals

The magnitude of $e(\hat{t}_k^{(1)})$ is dependent on the number of basis functions used in parameterization, i.e., M, and on the nonlinearity of the input signal itself. This error term can be reduced to an arbitrarily small level by increasing M. Since signal generators with low spatial frequency can be easily realized practically, the nonlinearity in the input, though it may be large, can be parameterized with a reasonably small number of basis functions and still guarantee that the residue error is small.

B. Effects of the Additive Noise in Input Signals

Let us assume the additive noise at the input to an ADC is stationary with zero mean and variance σ^2. The noise may cause the output code to be different from its expected value thereby changing the bin counts. Larger variance of the noise makes the code more likely to be different from its expected value. However, with a reasonably large number of samples per code, a change of one or two samples' value will not have a significant effect on the total number of samples for a code. Intuitively, the variance of $n(\hat{t}_k^{(1)})$ should increase with the variance of the additive noise but decrease with the average number of samples per code. By writing out the probability of a sampled voltage with noise larger than a specific transition level, which is a Bernoulli random variable, the variance of this random variable can be calculated. The variance of the error from additive noise of the transition level is the summation of variances of all different sampled voltages weighted by the probability. The probability of each sampled voltage is the same, but the variance is small if a sampled voltage is far away from the transition level of interest and large if it is close. With detailed statistic analysis, it can be shown that the following general relationship is true:

$$\sigma_n^2 = A\frac{\sigma}{N_s} \tag{44}$$

where N_s is the average number of samples per code and A is a constant dependent on the distribution of the noise, which can be determined numerically. For Gaussian additive noise, A is 0.5642. This sensitivity to noise is a fundamental problem in conventional histogram-based ADC test methods, and the effects here are comparable to those experiences when ideal linear ramps are used for testing.

C. Effects of the Quantization Error in Transition Times

The quantization error of transition times is bounded by (22). A smaller T_c means a larger average number of samples per code, i.e., a larger N_s, which in turn leads to smaller quantization errors. Assuming uniform distribution of the quantization noise, the variance of the quantization error can be expressed in terms of N_s as

$$\sigma_d^2 = \frac{1}{12N_s^2}. \tag{45}$$

The quantization error is also a problem in traditional histogram-based testing and comparable to that associated with this approach.

Typically, in an all codes production test environment, N_s is between 20 and 100 samples per code. The magnitude of the additive noise determines which term of (44) and (45) is more important to the testing result. If the standard deviation of the additive noise is comparable to 1 LSB, the effect of the quantization error will be much smaller than that of the additive noise. For high resolution ADCs, up to 1 LSB root mean square noise is typical. This was the rationale behind neglecting the effect of quantization in the earlier part of the discussion.

D. Effects of the Offset Between Two Signals

The value of the offset voltage α between the two input signals also affects the final INL estimation results. If the offset is too small, the difference between the nonlinearity of the two input signals at the same code level will be very small and noise will have significant effects on the LS method. The assumption that estimated parameters $\hat{a}_j$, $j = 1, 2, \ldots, M$ are close to the true value does not hold any more, and the numerical behavior of the LS method is no longer reliable in that situation. On the other hand, the offset cannot be too large either. As mentioned earlier, the last α equations in (37) will not be used in estimating the parameters, and hence the LS result is only optimal for part of the input nonlinearity and not necessarily optimal for the nonlinearity on the whole interval of [0, 1]. Analysis shows that offsets of 0.1 to 1% of full range are appropriate for the proposed method. Both simulation and experimental results support this conclusion. Furthermore, the SEIR method estimates the amount of offset, so no prior knowledge on the amount of offset is assumed.

In the discussion until now, it has been assumed that the two input signals are identical except for a fixed offset. This may become difficult to guarantee in a real testing environment. Various time varying effects such as drift in the reference voltage could result in slight variations in the offset value. The signal source may change from one run to another, which will introduce gain error and different nonlinearity between two signals. These nonstationarity effects can be eliminated to a certain extent by well-designed measurement procedures, if not completely eliminated. In both simulation and experimental measurement results provided in this paper, the effects of reference voltage drift are considered. Part of the problem has been solved by interleaving the two input signals in time to excite the ADC and collect histogram data. Simulation and experimental results

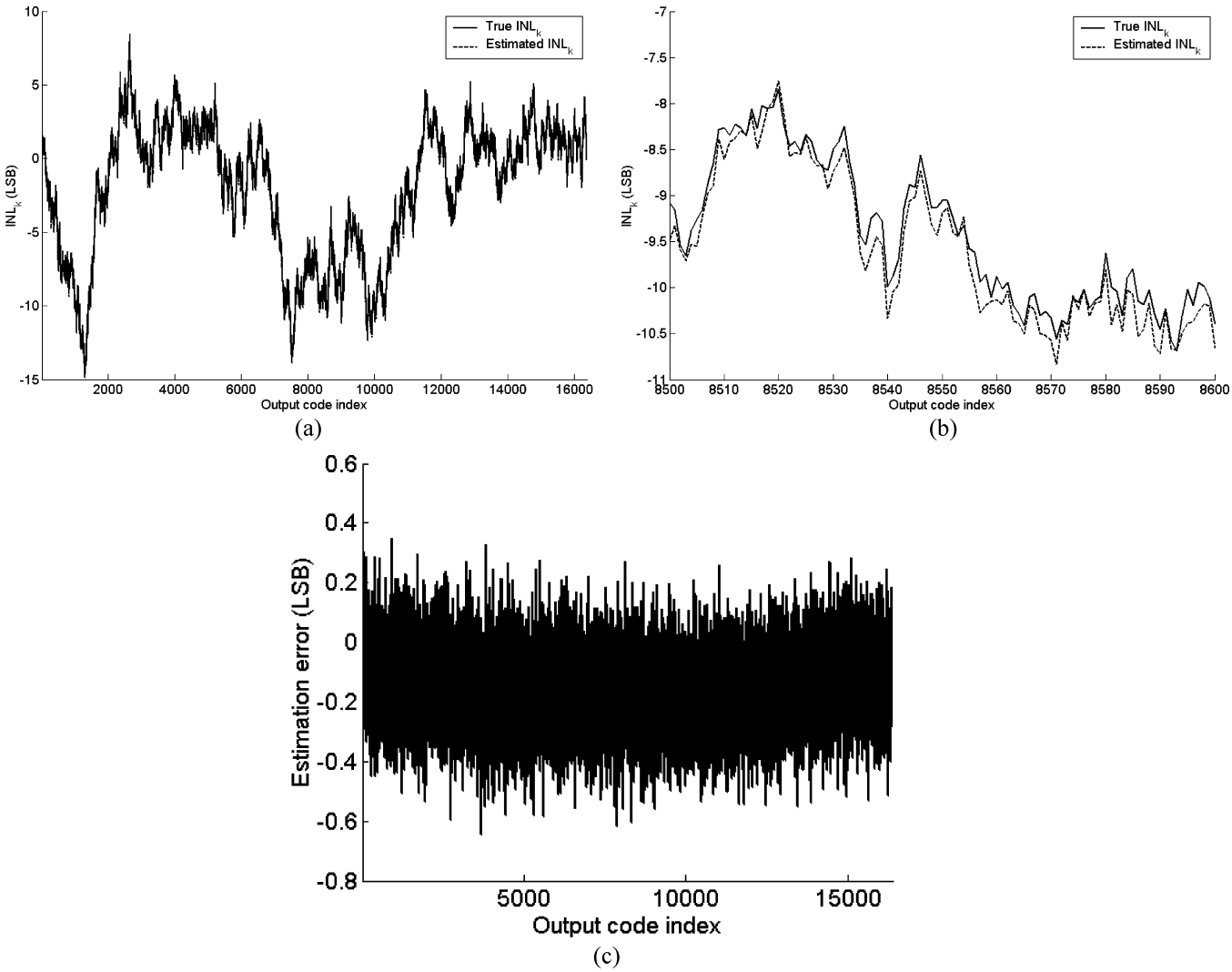

Fig. 2. INL_k estimation for a simulated 14-bit ADC. (a) True and estimated INL_k for all codes. (b) True and estimated INL_k zoomed in for codes from 8500 to 8600. (c) Error in INL_k estimation.

show that by interleaving the two signals with a "common-centroid" sequence, most of the nonstationary effects can be cancelled.

V. Simulation Results

To verify the performance of the SEIR approach, simulation has been done on ADCs of different resolutions and structures. Simulation results show that the SEIR approach can accurately identify INL of an ADC by using nonlinear excitations under various situations. Results for a 14-bit simulated ADC under different noise levels and average numbers of samples per code are summarized in this section. For the purpose of simulation, the nonlinear input signal is modeled as

$$x_1(t) = v_{os} + \eta\left[t + 0.04 * (t^2 - t)\right] + n(t). \qquad (46)$$

The maximum nonlinearity specified in (46) is 1% of the total input range. This corresponds to 7-bit linearity of the input signal. The offset between the first and second signals is 128 LSBs. However, as mentioned earlier, these data are unknown to the algorithm. In the simulation, 20 sinusoidal basis functions were used in the parameterization of the input signal. The reference voltage has a time-dependent drift with a linear gradient of 100 ppm over the total test time. This is to duplicate the effect of voltage drift in the real test environment. The two input signals are time-interleaved during data capture. The true INL_k of the simulated 14-bit ADC is plotted as a solid line in Fig. 2(a). The INL of the ADC is 14.88 LSB, resulting in a 10-bit linear device. With an additive noise of a 0.8 LSB standard deviation and an average sample density of 32 samples per code, the INL_k estimated by the proposed approach is plotted as a dashed line in Fig. 2(a). The true and estimated curves, in solid and dashed lines, respectively, match very well and are difficult to differentiate from each other. A zoomed-in version of the two curves for codes from 8500 to 8600 is plotted in Fig. 2(b), and we can see there are very little errors between the solid and dashed lines. The difference between the true and estimated INL_k, which reflects the error in prediction using the algorithm, is plotted in Fig. 2(c). The error in prediction is a fraction of 1 LSB with the maximum error being less than 0.7 LSB. The estimated INL of the ADC is 14.74 LSB, with a 0.14 LSB error from the true INL.

For the same ADC as shown in Fig. 2, simulation under different combinations of the average number of samples per code

TABLE I
MAXIMUM ERROR IN INL_k ESTIMATION FOR DIFFERENT N_s, σ, AND M_b

1% input nonlinearity, $\alpha = 4$ %, 100 ppm V_{ref} drift					
M_b =20, σ=3 LSB		N_s =64, M_b =20		N_s =64, σ=3 LSB	
N_s	INL_k error (LSB)	σ(LSB)	INL_k error (LSB)	M_b	INL_k error (LSB)
16	1.69	0.50	0.35	5	1.40
32	1.13	1.00	0.49	10	0.95
64	0.81	2.00	0.67	20	0.80
128	0.57	4.00	0.98	40	0.82

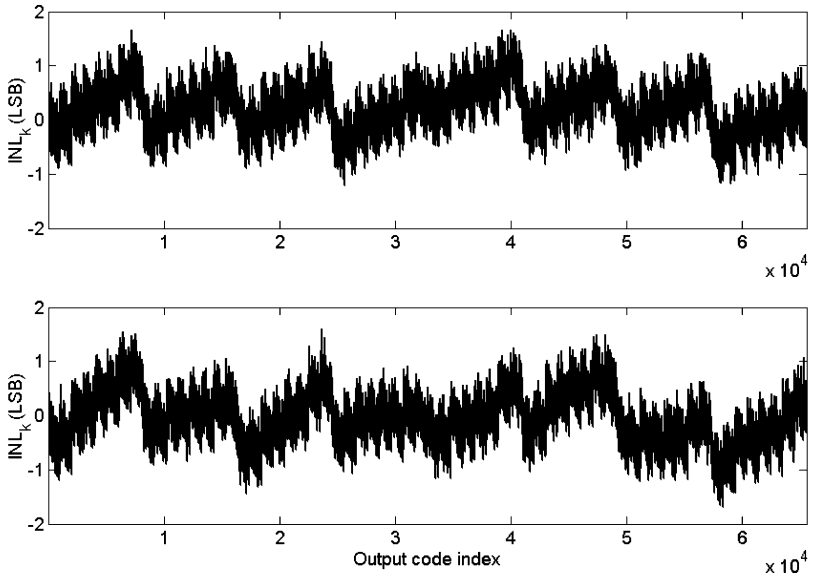

Fig. 3. INL_k estimation of a 16-bit SAR DAC with true INL 1.66 LSB. Top: estimated using the traditional histogram method with a linear stimulus. Bottom: estimated using the SEIR approach with nonlinear stimuli.

N_s, standard deviation of the noise σ, and the number of basis functions M_b were performed, and the results are summarized in Table I. For each entry of the INL_k error reported in Table I, the simulation was repeated 16 times and the average value of maximum INL_k errors is listed. It can be observed from Table I that when N_s is increased by four times, the estimation error is reduced by about 50%. When the standard deviation of the additive noise is increased by four times, the error in estimation is increased by two times. These statistics are in agreement with what is predicted by (44). When the number of basis functions M_b is increased from five to 20, the estimation error is reduced by 40% and no further improvement is seen beyond the 0.8 LSB level, implying that the error in estimation is dominated by noise and error effects. From simulation results it was observed that using 20 basis functions to model the input nonlinearity is a reasonable choice.

VI. TEST RESULTS FROM A 16-BIT SAR ADC

Commercially available 16-bit ADCs were tested to verify the performance of the new method. The sample used as the device under test (DUT) was a laser trimmed 16-bit ADC with excellent linearity performance with typical INL of about 1.5 LSB, which is a known test challenge. The test hardware used for the verification of the SEIR method is the same as used in the production test of the device.

A. Test Setup

Verification of the full performance of this ADC requires extreme attention to test hardware design. A 12-layer handler interface board is used with extensive ground, supply, and reference coverage. Extreme care is given to reduce ground loops and to obtain proper bypassing. High performance contactors, high precision resistors, high performance capacitors, and precision op-amps were used throughout the board. Latching relays were used to reduce temperature gradients generating metal to metal contact noise effects. The digital outputs were damped and buffered properly to avoid current surges. The test platform was a Teradyne A580 advanced mixed signal tester. The source generating both the linear and the synthetic nonlinear excitations was a 20-bit multibit delta-sigma digital-to-analog converter with 2 ppm typical linearity error, 100 μV/min typical

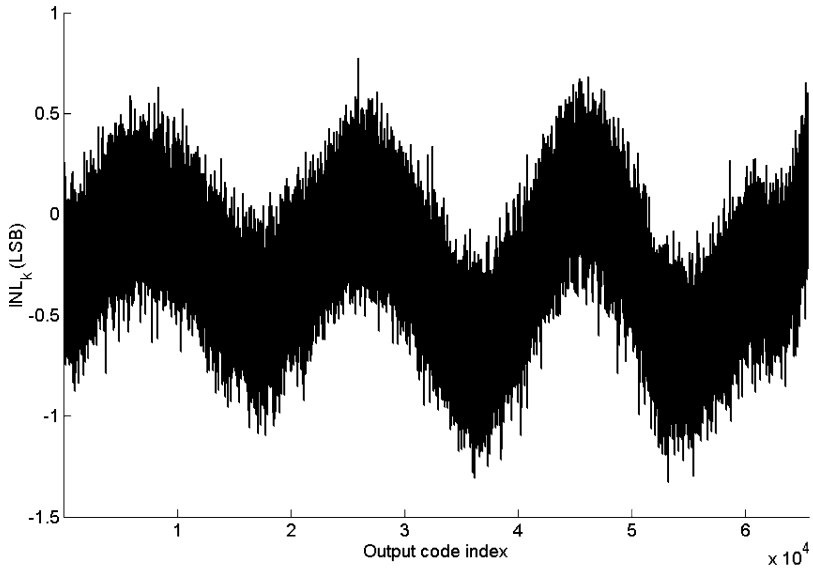

Fig. 4. Difference between the estimated INL_k by using linear and nonlinear signals.

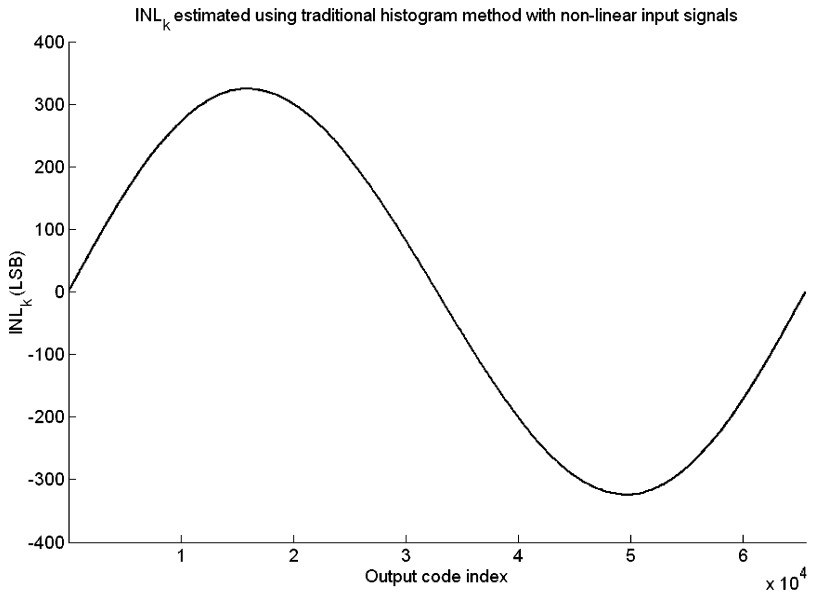

Fig. 5. INL_k of a 16-bit SAR DAC with true INL 1.66 LSB. Estimated using the traditional histogram method with a nonlinear stimulus.

drift characteristics, and 2 kHz bandwidth. This source was a typical example demonstrating that an expensive signal generator is not always good enough to provide low drift, high speed, and good linearity all at the same time. The dc offset of the nonlinear excitation was generated using an analog summing circuit. In the experiment, the capture of histogram data using nonlinear signals and identification of INL_k using the proposed method were done on different platforms. The tester setup, including the shape of input nonlinearity and offset between the two signals, were not known to the identification algorithm. Only two sets of histogram bin counts were fed to the analysis program.

B. Test Data Collection and Analysis

The INL_k of the ADC was first tested by using the traditional histogram method using a highly linear ramp excitation generated by the tester. Thirty-two samples per code were used to keep the test time reasonable. The INL_k plot is given on top in Fig. 3. We will term this the "measured" INL_k. The corresponding measured INL is 1.66 LSB. This measured INL_k and INL will be used as a benchmark to evaluate the performance of the proposed algorithm. Two nonlinear signals were synthetically generated by programming the source memory with a nonlinear digital waveform. The dc offset was chosen to be 33 LSB. The histogram was obtained with the new nonlinear input and was analyzed using the proposed method. The estimated INL_k is plotted on the bottom of Fig. 3. The estimated INL using the nonlinear input signals is also 1.66 LSB. From Fig. 3, we can see that the INL_ks estimated using linear and nonlinear input signals are really close. The difference between them is shown in Fig. 4. The error in prediction is less than 1 LSB and is an acceptable solution as far as 16-bit converters are concerned.

The "low frequency" errors in INL_k estimation, as can be seen in Fig. 4, come from the nonstationarity of the signal

source. The nonstationarity errors could not be completely eliminated by the proposed algorithm since they introduce different nonlinearities into the two ramps signals, but we tried to minimize their effects in the experiments by interleaving the two ramps signals. The "high frequency" residue errors come from the additive noise in the testing system. In a previous study on this device, the performance of all-code histogram test was compared to the performance of a reduced code test with a servo-loop. At each code, differences up to 0.7 LSB were found during the comparison, giving further justification to the premise that discrepancies indicating poor test capability do occur at the 16-bit level. This "high frequency" noise band can be further reduced by increasing the number of samples per code from 32 to a larger number. The results in Figs. 3 and 4 were calculated by using the first 14 polynomial basis functions. The INL estimation using sinusoidal basis functions also gave similar performance. This supports the observation that the proposed method does not rely strongly on the class of basis functions used in the model.

For the purpose of comparison, INL_k of the ADC was also estimated by using the traditional histogram method as in (26) with one of the two nonlinear signals. The result is plotted in Fig. 5. This estimation of INL_k is significantly affected by the input nonlinearity as discussed in (27), which introduced an error of more than 300 LSBs. The results also indirectly indicate that the input signals are just nearly 8-bit linear. They are fairly linear for the real world, but for our 16-bit precision ADC, the amount of nonlinearity in the input is excessive. The inputs used in these tests were synthetically generated to be representative of real-world quasi-linear analog ramp generators such as can be generated with simple integrators.

The test time penalty of this algorithm was found to be insignificant. The actual test time for this 16-bit ADC is 52 s, and the postprocessing of the algorithm takes 1.2 s in Matlab to calculate all of the INL_k values from the collected bin counts. Once coded in the tester workstation, the algorithm is expected to complete well within 100 ms. If a fast nonlinear source were used, the testing time performance would actually improve.

VII. Conclusion

The SEIR method for accurate linearity testing of ADCs using nonlinear input signals has been introduced. Beyond a readily satisfied restriction that the nonlinearities of the excitation have no high spatial frequency components, no prior knowledge about the offset or nonlinearities in the input signals is required with this method. Using actual production test hardware, the method was shown to be able to test a high-performance 16-bit ADC to well within ± 2 LSB INL specifications using only 7-bit linear inputs. The computation time required to implement this method is small and should not cause a significant degradation in test time compared to that required with existing approaches and may offer substantial reductions in test time in some applications. With the introduction of this method and corresponding extensions, the test hardware development paradigm could shift from one of highly linear source development to one of low drift and high-speed source development. The nonlinear low-drift input waveform and its shifted replica used in the proposed method can be readily generated on a DIB to reduce tester requirements and costs or on the chip to support DFT or BIST features.

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