Testing of Precision DACs Using Low-Resolution ADCs with Dithering

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Abstract

The bottleneck of DAC testing is the fast and accurate measurement devices. Production testing of high-resolution DACs with Giga Hertz clock rates is a challenging problem, and there is no widely adopted approach for on-chip testing of precision DACs in an SoC system. This work presents a new approach for testing high-resolution DACs. High speed data acquisition is achieved with flash ADCs; sufficient resolution is provided by dithering; and high test accuracy is guaranteed by the proposed data processing algorithm. This method provides a potential solution to both the production and on-chip DAC testing problems. Simulation results show that the static linearity of 14 bit DACs can be tested to better than 1 LSB accuracy, and dynamic performance of more than 85 dB SFDR can be tested with 1 dB accuracy, using 6-bit ADCs and dithering. Experimental results included in the paper also affirm the performance of the algorithm in testing high-resolution DACs using 6-bit ADCs.

1. Introduction

There has been explosive growth in the consumer electronics market during the past decades. PDA's, portable multimedia players, digital cameras and video recorders are prevalent in our daily life. Their functions can even be combined in a very small cell phone. As the IC industry shifts from PC-centric to consumer electronics-centric, digital technologies are no longer solving all the problems. Electronic devices integrating more functions, such as mixed-signal and RF, have become new challenges to the IC industry. System-on-a-chip (SoC) design and built-in self-test of mixed-signal circuits are two enabling technologies behind the integration of these functions and are of great interest to the industry and the academia.

When digital testing has been studied for long time, testing of analog and mixed-signal circuits is still in its development stage. Many methods proposed in 1980's or even earlier are still being used by engineers and researchers. Existing solutions for testing analog and mixed-signal (AMS) circuits have two major problems. First, the test cost is high. This has become a strategic problem to many large circuit manufacturers and led to serious discussions. Second, it is more and more challenging to improve the test capability of existing methods to keep up with the performance of the fast-evolving mixed-signal products demanded on the market. Furthermore, there is lack of effective methods for on-chip test of mixed-signal integrated systems. The *International Technology Roadmap for Semiconductors* (*ITRS*) identified mixed-signal testing as one of the most daunting SoC challenges [1].

The digital-to-analog converter (DAC) serves as the interface between the digital processing functions and analog signals. As the SoC design style getting more and more popular and requirements for high-quality AMS circuitries continuously going up, the demand for high-performance DACs is growing rapidly. The *ITRS* indicates that "… digital-to-analog conversion performance becomes increasingly important as it opens the door to new high-volume but low-cost applications." World's leading AMS integrated circuits companies, such as Analog Devices, Texas Instruments and National Semiconductors, are all manufacturing high-speed high-resolution DACs for applications such as wireless communications and digital signal processing. The best commercial parts, such as AD9779 from ADI and DAC5687 from TI, have 16-bit resolutions and more than 500 MSPS update rates. The next generation products with better performance are currently under design and will come to the market very soon [10].

Along with the advancement in DAC performance, there are consequently new needs in DAC design and testing. It is well known that DAC testing is more challenging than ADC testing, as DACs usually have higher resolutions and speeds than ADCs. Measurement devices used in conventional DAC testing methods should have better performance and run faster than the device under test (DUT) to provide accurate characterization results. It is a nontrivial task to manufacture sufficiently fast and accurate instruments for testing the current and future highest-performance DACs. For example, to get the linearity of a 16-bit DAC at a 500 MSPS rate, the tester should have better than 18-bit accuracy, about 110 dB in dynamic range, over a frequency range of at least 1 GHz. State-of-the-art data acquisition techniques have difficulties to achieve such performance.

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Our work is targeting at providing cost-effective solutions to the high-performance DAC testing problem. It is supported by the Semiconductor Research Corporation (SRC) at the member companies' request. We have come up with and investigated a novel method of using low-accuracy instruments to test high-performance DACs. Our study shows that high-resolution DACs can be accurately tested by using low-resolution ADCs with appropriate voltage dithering. We discussed our ideas and researches with engineers from the industry at the SRC annual review, where leading mixed-signal IC companies were well represented, and received very positive evaluations [8]. Some of our results were also summarized in a paper presented at TECHCON 2005. The paper shows that 14-bit DACs can be tested to 1-LSB accuracy by using 6-bit ADCs [11] and it received an award judged by a panel of industry experts in the area of analog and mixed-signal test. Because of the availability of very high-speed low-resolution ADCs, this approach provides a potential solution to the testing problem for high-speed high-resolution DACs.

2. Existing Methods for DAC Testing

Bench test plays important roles in design development, parameter tuning, debugging, and product validation stages of a DAC, while production test measures the specifications, sifts good, bad and marginal parts, and enables calibration for improving the performance of a DAC. An efficient testing method with high accuracy, short test time and low cost is very necessary for both of the two cases.

There are many well developed and widely adopted methods existing for bench and production test of different types of DACs. Quasi-static linearity and low-frequency dynamic performance of medium and low-speed DACs can be measured by using sigma-delta or dual-slope ADCs [9]. These types of ADCs can have very high accuracy, for instance, more than 20 bit linearity or 120 dB SFDR, but their sampling speed is inherently not high as limited by their respective architectures. High-frequency spectral test of communications DACs is usually done by using spectrum analyzers. Spectrum analyzers' dynamic range is affected by their nonlinearity and distortion and is usually limited to less than 90 dB or lower for some specific measurements. Notch filters are sometimes used to kill the dominant fundamental component to reduce the nonlinearity and distortion. Also spectrum analyzers will need long time to generate a complete spectrum over a wide frequency range with a small resolution bandwidth, and they do not provide any time domain information of the measured signal.

Some other DAC testing approaches have been studied and reported. An on chip pass-or-fail testing approach for DACs using accurate reference voltages and a precision gain amplifier was presented by Arabi, Kaminska, and Sawan [2]. An approach of using a DAC's static nonlinearity to characterize its intermodulation errors was introduced by Vargha, Schoukens, and Rolain [3]. This approach is useful if the intermodulation errors are mainly from static nonlinearities, which is true at low frequencies. Rafeeque and Vasudevan proposed an improved built-in self-test (BIST) scheme for DACs using an accurate sample-and-subtract circuit, a linear VCO, and a stable clock counter [4]. An overall review of existing built-in self-test approaches for DACs can be found in their paper.

In spite of these efforts, testing of high-speed precision DACs remains as a problem. It puts stringent requirements on the testing instruments. Linearity and stability of measurement devices should be better than the resolution of a DAC under test. It is also desirable to have a test structure that runs as fast as the DAC under test to conduct real-time testing and reduce the total test time. Production testing of DACs with higher than 1 GSPS update rate and better than 90 dB SFDR is a coming challenge in the very near future. Furthermore, the problem of on-chip testing for high-performance DACs is of interest and still open. Calibration techniques have proven to be effective in significantly improving a DAC's performances [5]. For effective calibration, an accurate characterization of the DAC is always necessary and often times carried out by using precision instruments such as off-chip high-resolution ADCs [6, 7]. If a highly accurate and stable DAC testing circuitry can be built on-chip, it will enable integrated self-calibration for DACs in an SoC design.

3. Linearity Specifications of DACs

The widely used terminologies for characterizing a DAC's static linearity are the same as those used for ADCs, the integral nonlinearity (*INL*) and the differential nonlinearity (*DNL*). Various definitions for *INL* and *DNL* exist, one slightly different from another. We will use the definition based on a fit line connecting the smallest and largest DAC output voltages. The *INL* is defined as the largest difference between the true transfer curve and the fit line of a DAC, and the *DNL* as the maximum error of the true increments between two consecutive outputs with respect to their averaged value. By using this definition, an *n*-bit DAC's *INL* at code *k* can be written as

$$INL_k = (N-1)\frac{v_k - v_0}{v_{N-1} - v_0} - k\ (LSB), k = 0,1...N-1, \quad (1)$$

where $N = 2^n$ and v_k is the output voltage associated with k. The unit LSB, standing for the least significant bit, is the averaged voltage increment,

$$1\ LSB = \frac{v_{N-1} - v_0}{N-1}. \quad (2)$$

INL_0 and INL_{N-1} are equal to 0 under this definition, which is a straightforward result of the fit line definition. The expression of *INL* is

$$INL = \max_k \{ | INL_k | \}. \quad (3)$$

Definitions of code-wise and overall *DNL* are

$$DNL_k = (N-1)\frac{v_k - v_{k-1}}{v_{N-1} - v_0} - 1 \ (LSB), k = 1...N-1, \quad (4)$$

and $$DNL = \max_k \{ | DNL_k | \}. \quad (5)$$

One of the widely used dynamic performance specifications for DACs is the spurious free dynamic range (SFDR), when a digital sine wave at a specific frequency is used as the input. The SFDR is defined as the difference between the amplitude of the fundamental component and that of the maximum spurious component in the spectrum of the DAC output.

INL and *DNL* of a DAC are usually tested by measuring the output voltages v_k and calculated as in (1) to (5). The SFDR of a DAC can be measured by sampling the output waveform with a high-accuracy digitizer and applying FFT to the sampled output sequence. It is obvious that to get both of these specifications we need accurate measurement of the DUT output.

4. Test Precision DACs Using Low-Resolution ADCs with Dithering

This work proposes a DAC testing approach with two goals, short test time and high accuracy. Flash ADCs have the fastest conversion rate among the data acquisition devices, so it is used in our approach to quantize the output voltage of high-speed DACs. Flash ADCs' resolutions are usually less than 8 bit because of the architecture limitation. The concern of using a low-resolution ADC in high-performance DAC testing is that it will introduce large quantization errors and its transition levels are not accurate. A dithering technique will be used to increase the resolution of the test, while final accuracy of the test result will be guaranteed by an effective data processing algorithm applied to the DAC output quantized by the low-resolution ADC with dithering.

4.1 Test Setup and Data Capture

The proposed strategy uses a low-resolution measurement ADC (m-ADC) and a dithering DAC (d-DAC) to test a high-performance DAC, usually called the device under test (DUT), see the block diagram in Figure 1. The d-DAC can be specifically designed for the testing purpose, or simply another device from the same product family of the DUT. The output of the d-DAC will be scaled by a small factor α and added to the output of the DUT as a dithering component. The dithered output of the DUT will be quantized by the m-ADC.

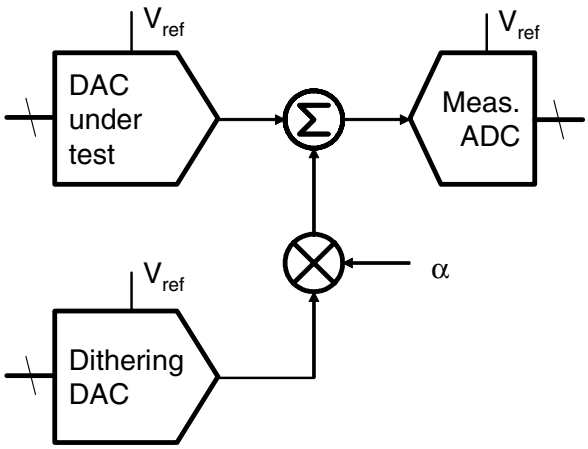


Figure 1 Block diagram of the proposed method.

In the test, the DUT will repeatedly generate a waveform of interest. During each period of the waveform, the d-DAC will provide a distinct but constant dithering voltage to be added to the DUT output. The m-ADC will quantize a certain number of periods of the waveform with different dithering levels. Because of the different dithering levels, the m-ADC's output codes associated with one output voltage of the DUT will be slightly different from one run to the next. Specifically, the output code associated with a voltage right smaller than an ADC transition level will increase when the dithering level increases. See Figure 2, where the DUT output waveform is triangular in this example.

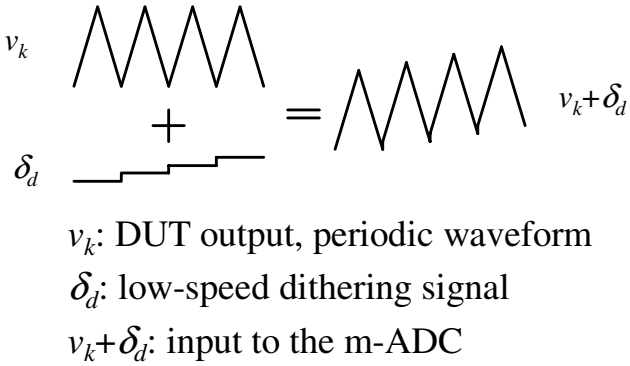


Figure 2 DUT's output with dithering.

The output codes of the m-ADC can be put into a two-dimensional structure as shown in Table 1, where N_d and N_D are the numbers of output levels of the d-DAC and the DUT, respectively. Assuming a 6-bit ADC is used, the output code will range from 0 to 63. Each column in Table I is associated with one d-DAC input, or alternatively speaking a dithering level, and collected from one period of the waveform generated by the DUT, a ramp in this example. On the other hand, each row in the table comes from one DUT output voltage v_k with different dithering levels. The scaling factor α is chosen for the d-DAC so that the dithered voltages associated with any one specific DUT output will cover at least one complete code bin of the m-

ADC. A dithering range of 3 *LSB* of the m-ADC is enough to guarantee this feature for a low resolution ADC, for which the *DNL* is usually much less than 0.5 LSB. Given this property, the output codes of the m-ADC associated with any input code to the DUT, a row in Table I, will always consist of at least 3 distinct codes. These output codes will be used to calibrate the m-ADC and test the DUT.

Table I. Output of the m-ADC vs. Input to the d-DAC

d-DAC input / DUT output	1	2	3		d	…				N_d
v_1	2	2	2	3	3	3	3	4	4	4
v_2	2	2	3	3	3	3	3	4	4	4
v_3	2	2	3	3	3	3	4	4	4	4
…										
v_k	40	41	41	41	41	42	42	42	42	43
…										
v_{ND-1}	60	60	60	61	61	61	61	61	62	62
v_{ND}	60	60	61	61	61	61	61	62	62	62

4.2. Proposed DAC Test Method

Without dithering, a DUT output voltage v_k. will be quantized by the m-ADC as a code j if $T_j < v_k <= T_{j+1}$, see Figure 3 (a). T_j is the transition level of the m-ADC between code j–1 and j. Based on this output, we can only have a rough estimation of the DUT output as

$$\hat{v}_k = T_j = v_k + q_k , \qquad (6)$$

where q_k is the quantization error introduced by the m-ADC. q_k can be as large as hundreds of LSBs for the DUT, since the m-ADC's resolution is much lower than that of the DUT. This is why low-resolution ADCs are not used to test precision DACs. In our approach, dithering is used to improve the resolution and minimize the quantization error.

As in Figure 2, the m-ADC will quantize many dithered copies of the DUT output voltage, $v_k+\delta_d$, where δ_d is the d-th dithering level, and the associated output codes form a row in Table I. The quantized output may change as the dithering voltage increases. At a specific dithering level, δ_{dkj}, the output code of the m-ADC changes from j–1 to j, as the dithered voltage changes from less than T_j to larger than T_j, see Figure 3 (b). Then we have a new estimate of the DUT output as

$$\hat{v}_k = T_j - \delta_{dkj} , \qquad (7)$$

where $\delta_{dkj} = d_{kj}/N_d - 1/2$ is the dithering level and d_{kj} is defined in Figure 3. For linearity test, the unit of the dithering voltage does not affect the final accuracy, so we use their linearly code-dependent part and normalize it with N_d, and 1/2 is taken off for representing differential voltage dithering. It is assumed in the discussion that the dithered voltages associated with v_k are uniformly spaced over the whole dithering range, a small interval around v_k. This is reasonable for a small scaling factor α, because any nonideality in the d-DAC is dramatically scaled down and becomes negligible as compared to the errors of the DUT. Further discussions on this assumption will be provided later in the performance analysis section. e_k in Figure 3 (b) is the error between the estimate of v_k in (7) and its true value. In this case, e_k is limited by the step size of the dithering voltages and can be made very small by a sufficient number of steps in a fixed range.

We have shown that we can effectively increase the resolution of testing by dithering, but test accuracy is not guaranteed because we do not know the exact value of T_j in (7). If we appropriately set the dithering range, there will be more than one transition in the m-ADC's output codes associated with v_k. In Figure 3 (b), the output code changes from j to j+1 at the dithering level $\delta_{dk(j+1)}$. This gives us another estimate as

$$\hat{v}_k = T_{j+1} - \delta_{dk(j+1)} , \qquad (8)$$

where $\delta_{dk(j+1)} = d_{k(j+1)}/N_d$. For each v_k, we can have at least two equations like (7) and (8). There are totally $2*N_D$ such equations in N_D v_k variables and N_{ADC}–1 T_j variables, for k = 1, 2… N_D. Since the m-ADC's resolution is lower than that of the DUT, N_{ADC}–1 is smaller than N_D. Therefore, the DUT's output voltages and m-ADC transition levels can be simultaneously solved from the $2N_D$ linear equations, under the Least Squares sense when necessary.

The DUT's linearity specifications can be calculated from the estimated v_k's using the equations or methods discussed in Section 3. The estimation errors in (7) and (8), e_k and e_k', are bounded by the dithering step size and can be reduced by applying a small dithering increment between two consecutive dithering levels. If we make this increment much smaller than 1 LSB of the DUT, the final test result based on the estimated values will have very high accuracy.

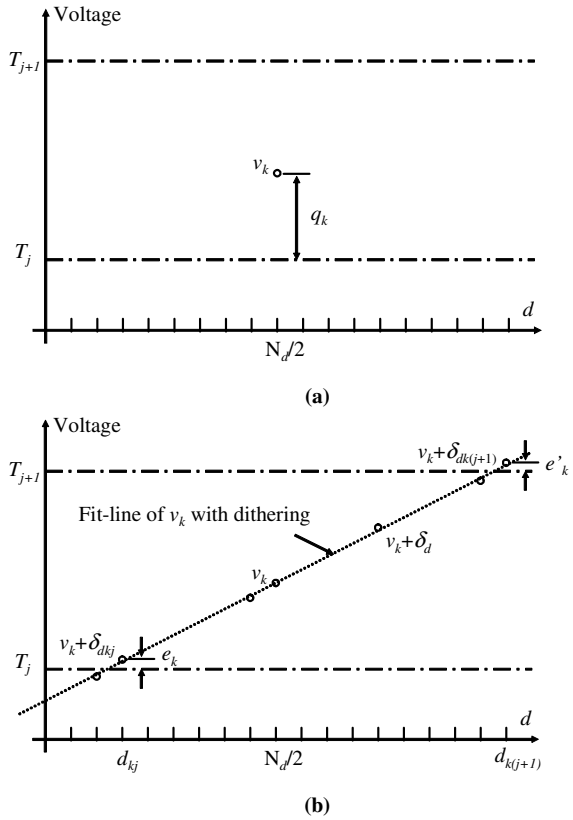


Figure 3 DAC testing with dithering.

4.3. Implementation of the Proposed Algorithm

It is inefficient to solve $2N_D$ equations simultaneously, especially when N_D is large. From investigating the equations' structure, we find that v_k's and T_j's can be calculated from the equations by applying a series of simple algorithmic operations.

We can first calculate one value of the m-ADC's j-th code bin width, $W_j = T_{j+1} - T_j$, from (7) and (8) as

$$\hat{W}_j^{(k)} = \delta_{dk(j+1)} - \delta_{dkj} . \tag{9}$$

For some different v_k's, we may have other values for W_j. The final estimate is the average over of these values,

$$\hat{W}_j = \underset{k}{mean}\{\hat{W}_j^{(k)}\} . \tag{10}$$

Transition levels of the m-ADC can then be calculated by taking cumulative summations of these code bin widths as

$$\hat{T}_j = \sum_{i=0}^{j-1} \hat{W}_i . \tag{11}$$

Without affecting the linearity of the m-ADC, T_0 is chosen to be 0 in (11). The DUT output voltage can be calculated from (7) and (8) as

$$\hat{v}_k = \underset{j}{mean}\{\hat{T}_j - \delta_{dkj}\} , \tag{12}$$

where the average is taken over all the T_j's covered by the dithered voltages of v_k.

The proposed DAC testing strategy with low-resolution ADCs can be summarized as following steps.

1. DAC under test generates periodic waveform with different dithering levels;
2. ADC quantizes the dithered waveform;
3. Estimate ADC transition points using (9)-(11);
4. Calculate DAC output voltages using (12);
5. Characterize DAC performance based on the measured waveform as discussed in Section 3.

5. Performance Analysis and Other Issues

This section provides some performance analysis and implementation considerations of the proposed high-performance DAC testing strategy.

5.1. Performance Analysis

An intuitive observation of the proposed algorithm is that the test result will be more accurate, if the m-ADC has higher resolution or the d-DAC can provide more distinct dithering levels with high resolution and linearity. Further analysis is in agreement with this observation and the test accuracy of the proposed method can be summarized by the following equation as

$$A_{test} = n_{ADC} + ENOB_{dith} - \log_2 \alpha , \tag{13}$$

where A_{test} is the desired test accuracy in bit, n_{ADC} is the m-ADC's resolution, $ENOB_{dith}$ represents the effective number of bits of the d-DAC in linearity, and α is the scaling factor in m-ADC's LSB. In (13), we assume the d-DAC has a sufficient resolution so that the error introduced by dithering is dominantly dependent on d-DAC's linearity and the effect of quantization noise is neglected. This assumption is reasonable as the resolution is comparatively easy to get, but the linearity of a DAC is limited by the design and fabrication technologies. In (7) and (8), we assume the d-DAC is linear while it is actually not, so nonlinearity of the d-DAC will affect the final test accuracy. Therefore, the d-DAC can only provide accuracy improvement equal to it linearity in (13). However, if the d-DAC can be accurately characterized or calibrated, the d-DAC can improve the test accuracy even more and the *ENOB* term in (13) can be replaced by the d-DAC's resolution $n_{d\text{-}DAC}$.

Using the above equation, we can determine the requirement on the test devices for specific test accuracy. For example, if we have a 6-bit ADC and the dithering range is 4 LSB at the 6-bit level, we need following d-DAC linearity to achieve 14-bit accuracy

$$\begin{aligned} ENOB_{dith} &= A_{test} - n_{ADC} + \log_2 \alpha = 14 - 6 + 2 \\ &= 10(bit). \end{aligned} \tag{14}$$

Eq. (14) means a 6-bit ADC can provide 14-bit test accuracy if 10-bit linear dithering is available.

5.2. Circuit Implementation

Assuming the DUT and the d-DAC are fully-differential current-steering DACs, a practical realization of the proposed test scheme is shown in Figure 4. This circuit can also be used with single-ended circuits after some simple modifications. The scaling of d-DAC's output and the dithering summation can be physically implemented with the two π networks of resistor $R_{+/-}$, $R_{s+/-}$ and $R_{d+/-}$. If the d-DAC and the DUT are the same product, $R_{+/-}$ and $R_{d+/-}$ are also the same. To correctly match DACs' output impedance and set the scaling factor, the resistance values need to be appropriately chosen such that

$$\begin{aligned} &R_{+/-} \parallel (R_{s+/-} + R_{d+/-}) = R_0; \\ &R_{+/-} /(R_{s+/-} + R_{+/-}) = \alpha, \end{aligned} \tag{15}$$

where R_0 is the specified load resistance of the DACs. The above conditions can uniquely determine the nominal values of $R_{+/-}$, $R_{s+/-}$ and $R_{d+/-}$. Since resistive networks are usually very linear, it will not introduce extra nonlinear errors in dithering, which is necessary to guarantee the m-ADC characterization.

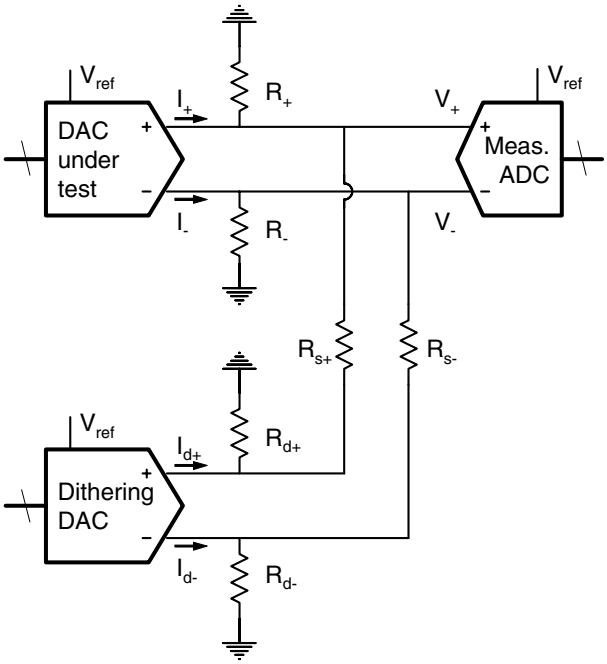


Figure 4 Circuit implementation of the proposed test scheme.

5.3. Data Storage and Transition Identification

If the number of required dithering levels is large for high test accuracy from (13), the size of Table I can be very large correspondingly. For instance, if the DUT has 16384 output voltages to be tested and the d-DAC needs to generate 1024 dithering levels, there will be approximately 16 M output codes to be stored. This storage requirement is nontrivial but still doable for production testing, but it is usually too much for an on-chip testing application. To reduce the storage requirement, the output codes from the m-ADC can be saved in a histogram style. This operation does not hurt the testing performance as we will see shortly, since the dithering information we need are all contained in the histogram data.

Table II. Histogram storage for m-ADC's output codes

DUT output	m	H_m	H_{m+1}	H_{m+2}	H_{m+3}
v_1	2	3	4	3	0
v_2	2	2	5	3	0
v_3	2	2	4	4	0
…					
v_k	40	1	4	4	1
…					
v_{ND-1}	60	3	5	2	0
v_{ND}	60	2	5	3	0

Table II shows the histogram storage of the test results. For a row in Table I associated with a DUT output voltage, the corresponding row in Table II saves the minimum m-ADC output code m, and the number of hits for m, m+1, …, up to the maximum output code, generated by the dithered voltages. The local histogram data can be used to estimate m-ADC transition levels as (9) to (11). The code bin width represented by the histogram counts is

$$\hat{W}_j^{(k)} = H_j^{(k)} / N_d \,, \tag{16}$$

when the j-th code bin is completely covered by the dithered voltage of v_k. And the $\delta_{dk,j}$'s in (12) can be calculated from the histogram as

$$\delta_{dkj} = \sum_{m<j} H_m^{(k)} / N_d \,. \tag{17}$$

So the testing algorithm carries out as before. However, the number of memory cells is dramatically reduced. Usually each row in Table II will contain one minimum code and five histogram counts at most. Only 100 K memory cells are needed for testing 16384 points as in the previous example. It is reduction of more than 150 times as compared to Table I.

Furthermore, the time for capturing the data as presented in Table II can be dramatically reduced by using binary search instead of linearly incremental search. Binary search will identify all the dithering levels at which transitions of the output of the m-ADC happen, associated with a specific DUT output voltage, which gives the $d_{k,j}$ information. These data can be summarized as in Table III. It's straightforward to determine the information required for m-ADC and DUT identification from Table III. If a 10-bit d-DAC is used in test, the number of samples required for one v_k is less than 40 when using binary search to determine at most 4 transitions. After the m-ADC is identified in one DAC test, this average number of

dithering samples for one v_k can be even reduced to less than 15 for following tests. It is a reduction of more than 50 times in testing time as compared to 1024-level linear dithering. Of course, binary search is only applicable to quasi-static test.

Table III. Output transitions of measurement ADC's output codes

DUT output	m	$d_{k,m}$	$d_{k,m+1}$	$d_{k,m+2}$
v_1	2	3	7	
v_2	2	2	7	
v_3	2	2	6	
…				
v_k	40	1	5	9
…				
v_{ND-1}	60	3	8	
v_{ND}	60	2	7	

Since both the number of the samples, equivalently testing time, and the amount of memory cells required for each DUT output is very small, this approach is cost-effective and can be practically implemented in either production or on-chip testing applications.

5.4. Other Test with the Proposed Algorithm

The DUT can generate other waveforms than a ramp or triangular signal, while the proposed method is still applicable. We just need to change the first column of the Table I, II or III correspondingly to the new waveform, for example, a sine wave. After we recover the waveform in the time domain by using the proposed method, following-up processing, such as FFT, can be taken to determine the DUT performance. The d-DAC's output also does not need to change in a ramp style. Sine wave style dithering can also be used. We just need to modify (9) to an appropriate form. The idea is similar to using sine waves in the histogram test of ADCs.

6. Simulation Results

14-bit DACs were tested in simulations. The proposed algorithm is not dependent on the architecture of the DUT. We chose the thermometer coded current-steering DAC as the DUT, since it has the largest number of independent errors from each of the current sources. Both static and spectral testing situations are simulated.

6.1. Quasi-Static Testing

A 6-bit flash ADC was used in measurement. The *INL* of the m-ADC is about 0.3 LSB at the 6-bit level. Its true INL_k is plotted in black in Figure 5. Transition levels of the ADC were first measured as discussed in Section 4.3. The estimated INL_k curve is plotted in red in Figure 5 as well. The two curves are nearly identical so that we can only see one curve on the plot. The estimation errors are about 0.002 LSB at the 6-bit level, which is sufficient for 14-bit DAC testing. The DUT has an *INL* of 14 LSB, and its true INL_k is plotted in black in Figure 6 (a). The DUT has about 10 bit linearity, which is realistic according to [2]. Another 12-bit DAC of the same structure is used to provide 4096 dithering levels. This d-DAC has about 10-bit linearity as well, with an *INL* of 3 LSB at the 12-bit level.

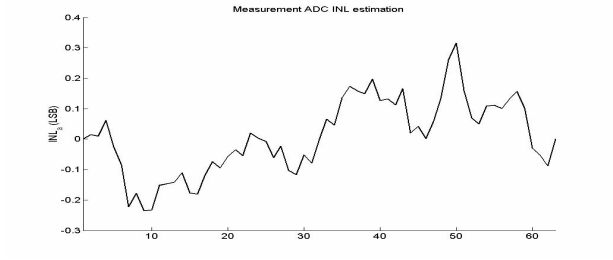
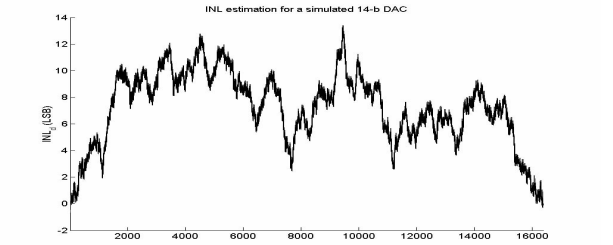
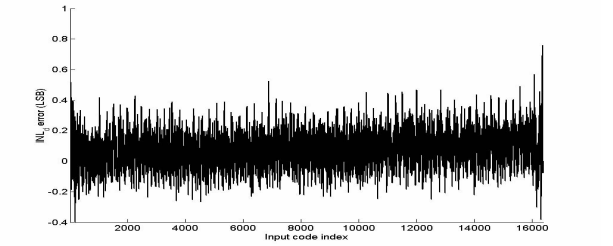


Figure 5 True and estimated INLk of the m-ADC.



(a)



(b)

Figure 6 INL_k estimation of a 14-bit DAC. The true and estimated INL_k are plotted in black and red in (a), respectively. Estimation errors are in (b).

In simulation, the dithering range was chosen to be 3.6 LSB of the m-ADC, and a noise is added to the input of the m-ADC with a standard deviation equal to 0.25 LSB at the 14-bit level. Based on calculation in Section 5.1, a 6-bit ADC, 10-bit linear dithering and the above dithering range can provide 14-bit test accuracy. The estimated INL_k of the DUT is plotted in red in Figure 6 (a). The estimated curve matches the true INL_k curve very well. The estimation errors for all codes are plotted in Figure 6 (b). The INL_k of the DUT was tested to better than 1 LSB accuracy at the 14-bit level. It is in agreement as what we expected.

6.2. Spectral Performance Testing

A single tone test was done on a 14-bit DAC for testing its SFDR. The m-ADC was still a 6-bit flash ADC. 512 dithering levels were used. A waveform length of 8196 samples, containing 111 periods of a sinusoidal signal, was

used in simulation. A Gaussian noise with a standard deviation of 1 LSB at the 14-bit level was added to the sine wave output of the DUT. The typical SFDR of simulated DACs was set at 85 dB.

The spectrum of the true output sine wave of a DUT is plotted on the top of Figure 7, for which the SFDR was read as 86.85 dB. By using the proposed testing algorithm, the spectrum was estimated and plotted on the bottom of Figure 7, where the SFDR was estimated as 87.19 dB. The two spectrums match very well at the significant frequency components and the true and tested SFDR readings are within an 1-dB accuracy window, when a 6-bit ADC was used in measurement.

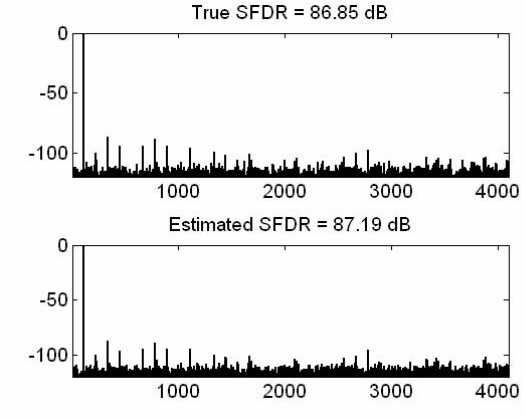


Figure 7 SFDR test of 14-bit DAC with 6-bit ADC and dithering.

To further validate the performance of the proposed testing strategy, same simulation was repeated on 64 different 14-bit DUTs. The SFDR estimation errors are plotted in Figure 8, with the true SFDR as the horizontal axis. Most of the SFDR testing errors are less than 1 dB and all of the errors are within 1.5 dB for SFDR ranging from less than 75 dB to more than 90 dB.

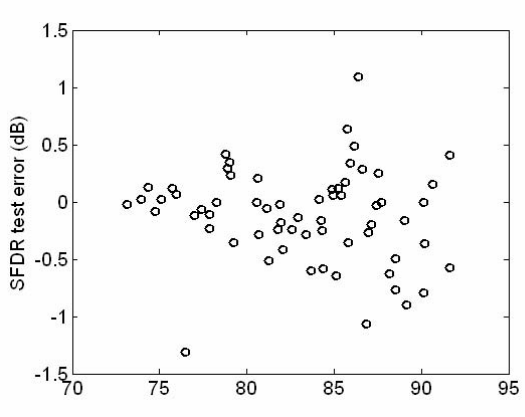


Figure 8 SFDR test error with 6-bit ADC.

7. Experimental Results

Some experiments were done to validate the performance of the proposed DAC testing algorithm with low-resolution ADCs. We used a Conejo baseboard by Innovative Integration in our experiments. This board has four 16-bit DACs, four 14-bit ADCs, and a TI DSP on chip. As the total number of samples for the dithered measurement is limited by the data storage capability of the board, testing of very high-resolution DACs were not carried out, but we can show that the concept of the proposed method is working by the following results.

7.1. Spectral Test

A sine wave signal with a synthesized –60 dB second harmonic component was tested. 2048 samples were taken on a waveform containing 11 periods. The signal was first measured by using a 14-bit ADC. The FFT spectrum is plotted in Figure 9. The measured SFDR was 59.91 dB. It will be used as a reference to evaluate the performance of the proposed method.

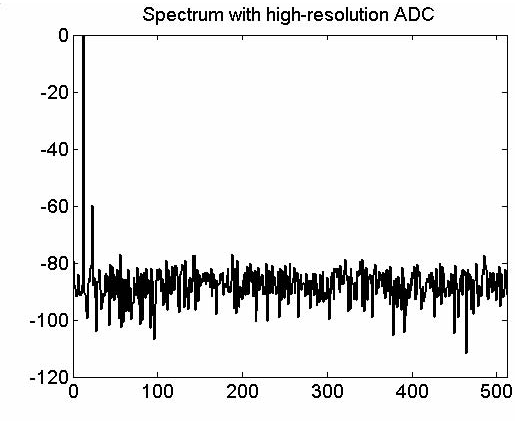


Figure 9 Estimated spectrum using a 14-bit ADC.

The signal was then tested by using a low-resolution ADC with dithering. Since there was no 6-bit ADC in our test setup, we used the high-resolution ADC on the Conejo baseboard and truncated the least significant bits of the output to get 6-bit digitizing results. Although the original ADC had a very high performance, its quantization effects after truncation could easily mask the true spectral errors in the signal as shown in Figure 10. There are many spurious components have larger than -60 dB magnitudes.

The sine wave was then repeated 256 times and dithered by a sine wave generated by the d-DAC, using the single-ended version of the resistor summing circuitry in Figure 4. The range of the dithering signal was 5% of the output of the DUT. The dithering signal contained 257 periods during the total of 2048*256 samples on the DUT output, so that each DUT output experienced a complete period of sine wave dithering. The dithered output was quantized by the pseudo 6-bit ADC. The proposed algorithm was used to draw the FFT spectrum, which is plotted in Figure 11. The estimated SFDR was 59.23 dB. This number is very close to the true value. The -60 dB second harmonic was identified. Other spurious terms were at least 20 dB smaller

in the test result, which is natural considering that the original resolution of the DAC is 16-bit.

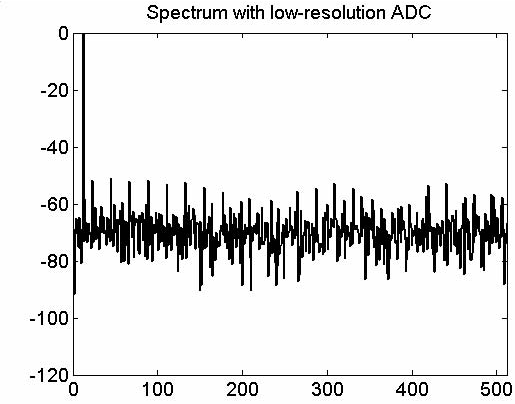


Figure 10 Estimated spectrum using 6-bit ADC w/o dithering.

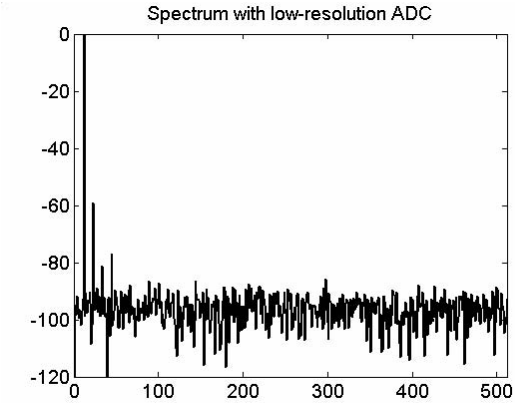


Figure 11 Estimated spectrum using 6-bit ADC w. dithering.

It is obvious that the noise level in the test results with the 6-bit ADC is about 10 dB lower than that with the high-resolution ADC. This benefit comes from the averaging effect of the large number of dithering.

7.2. Quasi-Static Test

A pseudo 10-bit DAC was generated by using the 16-bit DAC on the Conejo baseboard for INL_k testing. An extra sinusoidal shape INL_k was purposely introduced. INL_k of the 10-bit DUT was measured using a 14-bit ADC many times. The mean value of INL_k from different measurements, when the noise effect is averaged out, would be used as a reference for evaluating the performance of the proposed method. It is plotted in Figure 12. The 10-bit DAC was then tested by using the proposed algorithm with a 6-bit ADC, from truncation, and 512 level dithering. The dithering range is set to be about 5% of the m-ADC input range. The measured INL_k is plotted in Figure 13.

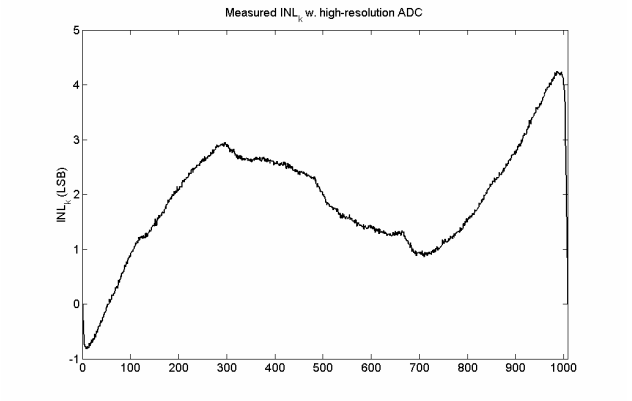


Figure 12 INL_k measurement with a high-resolution ADC.

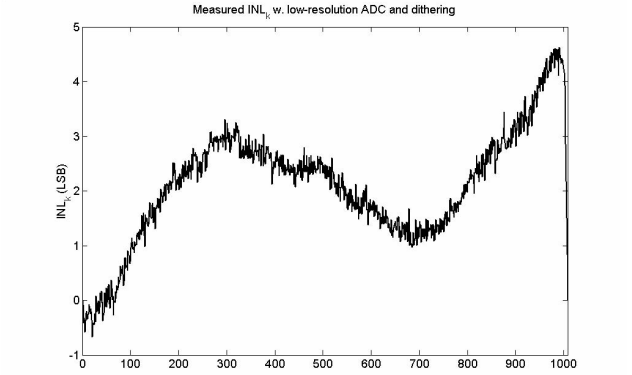


Figure 13 INL_k measurement with 6-bit ADC and 9-bit dithering.

It can be calculated from (13) that a 6-bit ADC plus 9-bit dithering and the dithering range we used can provide about 13-bit test accuracy. From Figure 12 and 13, we can observe that INL_k measured by the 14-bit ADC and the proposed method are very close to each other. Therefore the algorithm works and achieves the performance we predicted.

8. Conclusions

An effective DAC testing approach is presented in this paper. This approach uses high-speed flash ADCs and dithering to test high-resolution DACs. Simulation results show that INL_k of 14-bit DACs can be tested to 1-LSB accuracy by using a 6-bit ADC and 12-bit dithering, and spectrums of signals with more than 85-dB SFDR can be measured to 1 dB accuracy. Experimental results also supported the effectiveness of the algorithm in DAC testing using low-resolution ADCs. Because the proposed algorithm doesn't require high-precision test instruments, it provides a potential practical solution to the problem of production and on-chip testing of high-speed high-resolution DACs.

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