Aggressive Area Scaling in Passive Transresistance Networks

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***Abstract*—the issue of very aggressive area scaling to practically achieve large transresistance in a small amount of area is addressed. Closed form analytical expressions for the area scaling efficiency for an R-2R transresistance network and a ladder-based transresistance network are presented. Closed form analytical expressions and numerical comparisons for the standard deviation of the transresistance of these networks that are useful for determining ratio matching yield are also included.**

I. INTRODUCTION

Resistors are widely used in circuits implemented at the printed circuit board level but the practical implementation of resistors in standard high-volume CMOS processes is limited because of the area required for the physical implementation of the resistor. In such processes, polysilicon (with silicide blocking) is the only feature that is consistently available that can produce resistors with attractive voltage coefficients, reasonable matching properties, and reasonable process variability. Since the sheet resistance of polysilicon in such processes is rather low (typically between 10 Ω/□ and 50 Ω/□), the area required for resistors beyond a few KΩ is very large [1] and the power required to drive small resistors at reasonable signal levels is high and it is these two factors that dominantly limit the practical implementation of resistors in such processes. Although this limitation is of concern in essentially all circuits where resistors would offer attractive circuit potential, it is of particular concern when building active filters that operate from the audio frequency range up to the MHz range and beyond since the long time constants inherently require either large valued resistors or large capacitors.

Although the availability of a standard two-terminal resistor would be of particular interest, resistors are often used to realize a linear transresistance function. An example of using resistors to realize a transresistance function is shown in the simple feedback amplifier of Fig. 1a where the voltage gain is ideally given by the expression:

$$A_V = -\frac{R_2}{R_1}. \tag{1}$$

Correspondingly, the voltage gain of the circuit of Fig. 1b which uses two transresistance elements is given by the expression:

$$A_V = -\frac{R_{T2}}{R_{T1}}. \tag{2}$$

In (2), R_{T1} and R_{T2} are the transresistance gains of the input and feedback blocks respectively. An area efficient linear implementation of the transresistance block with reasonable process variability and matching will thus provide the same gain function as the resistor-based feedback amplifier.

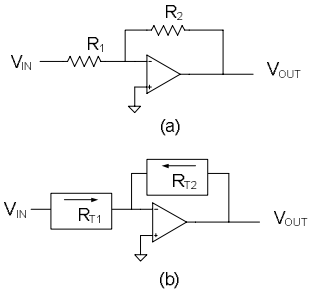

Figure 1. Voltage Amplifiers a) Resistor-based b) Transresistor-based.

Several authors [2]-[5] have discussed the use of various passive ladder-type resistor networks comprised of relative low-valued resistors for the implementation of the transresistance elements. These structures, which are inherently very linear, offer significant reductions in the area compared to what is required for a direct resistor implementation. In this work, a comparison of the area required for several of these implementations will be made along with a discussion of the sensitivity of the resultant structures to process variations and matching.

II. AREA EFFICIENCY OF THE TRANSRESISTOR NETWORKS

Two transresistor networks are shown in Fig. 2. The first is a generalization of what some authors term a T-feedback network [2]. If the network is reduced to a single stage, the transistor is comprised simply of a resistor R_S so when applied in the amplifier circuit of Fig. 1b, it is equivalent to the feedback structure of Fig. 1a. When a

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two-stage structure is used it becomes the popular T network. Generally R_P is considerably less than R_S when using the T-network to increase the transresistance. The circuit of Fig. 2b is recognized as an n-stage R-2R network. It was used recently by Ismail [3] and Rijins [5] for obtaining an area-efficient programmable transresistance for a filter and VGA applications and is shown in the highest transresistance configuration in Fig. 2b. The left-most 2R resistor does not contribute to the largest transresistance but was included in [3] to provide for the binary programmability of the transresistance. In this work we will not concentrate on the digital programming structures but the variability discussion in the next section will identify what programmability is needed to compensate for process variations and random mismatch in the passive elements.

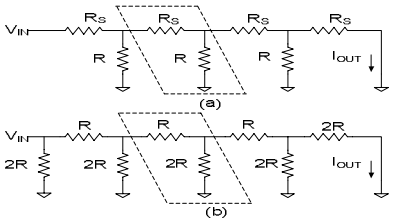

Figure 2. Ladder-based transresistors a) 4-stage T-network b) 4-stage R-2R network.

In both cases the basic element that is repeated to increase the number of stages is shown in the dashed box. The distinction between the T-network and the R-2R network is only in how the component values are selected.

It will be assumed that the width of all resistors is fixed and that a reference resistor with this width is identified. This reference resistor can be thought of as a unit resistor. It will also be assumed that all resistors are realized with a series connection of the appropriate number of unit resistors. This reference will be of minimum width if the goal is to minimize the total resistor area. In the networks of Fig. 2, it is assumed that the reference resistor is the resistor designated as "R" and that the nominal area of this reference resistor is A_{RN}. It thus follows that the area for a resistor R_X is given by

$$A_{RXN} = A_{RN}\frac{R_{XN}}{R_N},$$

where R_{XN} is the nominal value for the resistor R_X and R_N is the nominal value for the reference resistor R.

For notational convenience we will define a reference resistor scaling factor θ of a transresistance network to be the ratio of the nominal equivalent transresistance, $R_{EQN,}$ to the nominal resistance of the reference resistor. Formally, we thus have

$$\theta = \frac{R_{EQN}}{R_N}. \qquad (2)$$

It can be shown that the transresistance of the R-2R network is given by the expression:

$$R_{R-2R}(n) = 2^n R. \qquad (3)$$

where n is the number of stages in the network. It follows from (3) that significant increases in the transresistance can be achieved with an R-2R network if a large number of stages are used. It also follows from (2a) and (3) that the reference resistor scaling factor for the R-2R transresistor is

$$\theta_{R2R} = 2^n. \qquad (3a)$$

The transresistance of the T-network is given by

$$R_T = \begin{cases} aR & n=1 \\ (2+a)aR & n=2 \\ (2+a)^2 aR & n=3 \\ \left[(2+a)^3 - 2(2+a)\right]aR & n=4 \\ [(a+2)^4 - 3(a+2)^2 + 1]aR & n=5 \\ [(a+2)^5 - 4(a+2)^3 + 3(a+2)]aR & n=6 \\ [(a+2)^6 - 5(a+2)^4 + 6(a+2)^2 - 1]aR & n=7 \\ [(a+2)^7 - 6(a+2)^5 + 10(a+2)^3 - & \\ \quad 4(a+2)]aR & n=8 \end{cases}, \qquad (4)$$

where $a = R_s / R$. For large n, R_T is proportional to $(2+a)^{n-1}$ which becomes large if a and n are even modestly large. A parametric closed-form expression for the reference resistor scaling factor for the T-network appears to be somewhat complicated but θ_T for any fixed n can be obtained directly from (4) by simply dividing the terms on the right hand side by R.. Table I shows a comparison of the transresistance of the R-2R network and the T-network for a =4, 10, and 25. With a=10 and only 3 stages, the transresistance of the T-network increases by over 3 orders of magnitude and with a=25 and n=8, the transresistance of the T-network increases by over 11 orders of magnitude. Although the increase in the transresistance of the R-2R network is geometric, it is much smaller than that obtainable for the T-network when the value of a is even modestly large.

The issue of what area savings is possible with the transresistance networks is of more concern. We will define the resistance area efficiency, η, to be the ratio of the transresistance, R_{EQ}, to the total resistance of the network. Formally,

$$\eta = \frac{R_{EQ}}{R_{TOT}}. \qquad (4a)$$

Thus, η is an area savings factor for using a transresistance network rather than a single resistor for implementing a given transresistance. For the R-2R network the total resistance is R_{TOT}=(3n+4)R so the area efficiency is given by the expression

$$\eta_{R-2R}(n) = \frac{2^n}{3n+4}. \qquad (5)$$

For implementing the T-network, the total resistance is R_{TOT} = (na+ n-1)R. By dividing the total transresistance in

(4) by this factor, the area efficiency of the T network can be readily obtained as shown in (5a).

$$\eta_T = \begin{cases} \dfrac{a}{na+n-1} & n=1 \\ \dfrac{(2+a)a}{na+n-1} & n=2 \\ \dfrac{(2+a)^2 a}{na+n-1} & n=3 \\ \dfrac{\left[(2+a)^3-2(2+a)\right]a}{na+n-1} & n=4 \\ \dfrac{\left[(a+2)^4-3(a+2)^2+1\right]a}{na+n-1} & n=5 \\ \dfrac{\left[(a+2)^5-4(a+2)^3+3(a+2)\right]a}{na+n-1} & n=6 \\ \dfrac{\left[(a+2)^6-5(a+2)^4+6(a+2)^2-1\right]a}{na+n-1} & n=7 \\ \dfrac{\left[(a+2)^7-6(a+2)^5+10(a+2)^3-4(a+2)\right]a}{na+n-1} & n=8. \end{cases} \quad (5a)$$

Numerical comparisons of the area efficiency appear in Table I. It can be seen that it takes 5 stages for the R-2R network to obtain a factor 10 improvement in area efficiency. On the contrary, the T-network offers substantial improvements in area efficiency even for relatively small values of n and offers over 9 decades improvement in efficiency for an 8-stage implementation when a=25.

III Process Sensitivity of Transresistor Networks

It has been shown in the previous sections that substantial reductions in area and substantial scaling in transresistance can be obtained with the transresistance networks. A major factor that limits the practicality of these networks is their sensitivity to process variations. In this section the sensitivity of these networks to process variations will be considered. Two issues are of particular interested. The first one is the concern of how the nominal transresistance varies with process. The second issue is how the transresistance varies with die-level variations.

In regard to the variation with process parameters, it should be noted that the transresistance of all of the ladder-based structures can be expressed as a product of a geometric factor and the resistance of a reference resistor. It thus follows that the process sensitivity of the transresistors is the same as that of a standard resistor in the same process.

The issue of die-level variations will now be addressed. The components of die-level variations that associated with uncorrelated deviations of widely spread devices can be considered as part of random process variations. In what follows we will assume that layout techniques are used in the transresistors to compensate for gradient effects and that the local random variations will be the dominant factor affecting the variability of resistors. It will also be assumed, for convenience, which the edge roughness effects on the resistor boundary are negligible compared to the random variations of the sheet resistance in the resistor body.

Under these assumptions, it is well known that the variance of a rectangular resistor of length L and width W and value R_X due to local random variations in the sheet resistance can be expressed as

$$\sigma^2_{\frac{R_X}{R_{XN}}} = \frac{\sigma^2_\rho}{A_{R_X}}, \quad (6)$$

where A_ρ is a process-dependent constant, R_{XN} is the nominal value of the resistor, and $A_{RX}=WL$ is the area of the resistor. Our goal will thus be to see how the variance of a transresistor compares to that of a basic rectangular resistor. It can be shown that the variance of the transresistance can be expressed in terms of the variance of the reference resistor R by the expression

$$\sigma^2_{\frac{R_{EQ}}{R_{EqN}}} = h\sigma^2_{\frac{R}{R_N}}, \quad (7)$$

where the term h is dependent upon the architecture of the transresistor but not upon the process. It thus follows from (6) and (7) that

$$\sigma^2_{\frac{R_{EQ}}{R_{EQN}}} = h\frac{\sigma^2_\rho}{A_R}. \quad (8)$$

It also can be shown that

$$A_R = \frac{\eta}{\theta}A_{TOT}, \quad (9)$$

where A_{TOT} is the total area of the transresistance network. Substituting from (9) into (8) we obtain

$$\sigma^2_{\frac{R_{EQ}}{R_{EQN}}} = \left[\frac{h\theta}{\eta}\right]\frac{\sigma^2_\rho}{A_{TOT}}. \quad (10)$$

The term in brackets in (10) is a variance scaling factor and is dependent only on architecture of the transresistor and the dependence on process and area has the same functional relationship as for a single resistor as evidenced by comparing (10) with (6). We will now consider the variance scaling factor.

From quite straightforward derivations for $1 \le n \le 3$, the values of h are given in (11) and (12) for R-2R network and T-structure, respectively, and hand analysis becomes quite tedious for n>3.

$$h_{R-2R} = \begin{cases} 0.5 & n=1 \\ 0.5625 & n=2 \\ 0.707 & n=3 \end{cases} \quad (11)$$

$$h_T = \begin{cases} \dfrac{1}{a} & n=1 \\ \dfrac{a^3+2(a+1)^2}{a(a+2)^2} & n=2 \\ \dfrac{2a^3+3a^2+4a+2}{a(a+2)^2} & n=3 \end{cases} \quad (12)$$

TABLE I. EQUIVALENT RESISTANCE AND AREA EFFICIENCY OF TRANSRESISTOR NETWORKS

	$R_{EQ,}\theta$				Area Efficiency, η			
n	R2R	T (a=)			R2R	T (a=)		
		4	10	25		4	10	25
1	2	4	10	25	.29	1	1	1
2	4	24	120	675	.4	2.67	5.71	13.2
3	8	144	1440	1.82E4	.62	10.3	45	236.7
4	16	816	1.7E4	4.91E5	1	42.9	396	4764
5	32	4760	2.03E5	1.32E7	1.68	198	3760	1.03E+05
6	64	2.77E4	2.42E6	3.57E8	2.91	956	3.72E4	2.30E+06
7	128	1.62E5	2.88E7	9.63E9	5.12	4750	3.79E5	5.31E+07
8	256	9.42E5	3.44E8	2.59E11	9.14	2.41E4	3.95E6	1.25E+09

Substituting the parameters h, θ, and η required in variance scaling factor we obtain (13) and (14).

$$\left[\frac{h\theta}{\eta}\right]_{R2R} = \begin{cases} 3.45 & n=1 \\ 5.625 & n=2 \\ 9.123 & n=3 \end{cases}, \tag{13}$$

$$\left[\frac{h\theta}{\eta}\right]_{T} = \begin{cases} 1 & n=1 \\ \dfrac{2a^4+5a^3+6a^2+8a+2}{a^3+4a^2+4a} & n=2 \\ \dfrac{6a^4+13a^3+18a^2+14a+4}{a^3+4a^2+4a} & n=3 \end{cases}. \tag{14}$$

The variance scaling factor is tabulated in Table II for both the R-2R network and T-structure. The variance scaling factor increases with *n* and, in the T-structure, also increases with a. In both cases it becomes considerably larger than 1 for large n. This information should be useful for determining the area that must be allocated to the transresistance networks for achieving a predetermined acceptable standard deviation.

Although we will not go into details, it can be shown from (7), (11) and (12) that the variance of R_{EQ} is comparable to that of the reference resistor by observing the values of h are in the vicinity of 1 for both transresistance networks. This suggests the transresistance networks configured discussed in this paper will not provide good matching performance unless a larger area is allocated to the reference resistor and increasing the area allocated to the reference resistor defeats the purpose of the area scaling efficiency. Thus, if digital programming is not used, aggressive area efficiency scaling will be useful only if there are rather lax tolerances on matching. If digital programming, which is inherent in the ladder transresistance structure, is used, the substantial area benefits of the transresistance networks can be derived

Issues such as bandwidth requirement of the op amp when transresistance are used in amplifiers and filters and the effects on noise performance when aggressive resistor scaling is used are of interest, but those material are not be addressed further in this paper.

TABLE II. VARIANCE SCALING FACTOR

Variance Scaling Factor				
n	R2R	T (a=)		
		4	10	25
1	3.45	1	1	1
2	5.625	6.7	17.8	47
3	9.123	18.8	52	140

IV CONCLUSION

Closed-form analytical expressions useful for designers have been derived for two transresistance networks that offer aggressive area scaling over what is required for realizing the same transresistance function with single resistors. It was shown that much more aggressive area scaling for a given number of stages is attainable with the transresistance T-network than the transresistance R-2R structure. The sensitivity to process variations for the transresistance networks is the same as that for single resistors. Analytical design expressions for the standard deviation of the transresistance in the transresistance networks were also presented. These results are useful when designers need to determine the level of binary programming that is required to achieve a desired level of matching accuracy at a given yield level.

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