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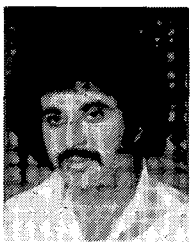

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Switched-Resistor Filters—A Continuous Time Approach to Monolithic MOS Filter Design

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Abstract—**A method of designing continuous-time active *RC* filters which employ only capacitors and FET transistors is presented. The effective *RC* time constants of these filters are determined by capacitor ratios. The filters employ switched resistors. These filters can use any existing active *RC* or passive *RC* topology as the basis for the design and inherit the sensitivity properties of the circuit from which they are derived. These switched-resistor (SR) filters operate over a wide frequency range and are manufacturable in monolithic form using a basic MOS process which requires no component trimming.**

I. INTRODUCTION

THE INABILITY to accurately determine *RC* products in existing semiconductor processes has impeded the development of monolithic active *RC* filters. This problem has been recently circumvented by using switched-capacitor (SC) techniques in which the effective *RC* products are determined by capacitor ratios which can be accurately determined (to 0.1 percent or better [1]) in existing popular NMOS processes. The SC filters, however are discrete-time in nature and thus introduce aliasing and hence require additional input and output continuous-time filters. SC filters are also subject to frequency warping, require cumbersome analysis and modeling, and are often limited to low-frequency applications due to the limitations of the switches and active devices imposed by the high clock rates generally required.

The switched-resistor (SR) technique presented here employs FET's biased in the ohmic region as resistors. All FET resistors are periodically switched out of the filter and into a pretune circuit which maintains the resistance of the FET at the prescribed value by establishing the gate to source voltage on a holding capacitor. The continuous-time nature of the filter, however, is maintained by alternately switching other properly pretuned FET resistors into the filter during the pretune states. Since the resistors are memoryless elements, additional requirements such as the rapid transfer of charge at switching times generally required in SC circuits are not made on the active devices.

The use of FET's as voltage-controlled resistors in the design of compensated filters has been discussed in the literature. Rao and Srinivasan [2] used JFET's to compensate for power supply effects on the GB of the OP AMP's. Master and slave filters are employed in [3] and [4] where the master is phase-locked to a reference signal source to generate a dc voltage which simultaneously controls both the master and slave filters. Unfortunately the "Master–Slave" approach requires matched FET characteristics in [3] and matched programmable operational amplifiers and FET characteristics in [4] since the "Master" filter rather than the desired "Slave" filter is compensated. The matching of the FET resistances for a common gate to source voltage are strongly dependent upon the matching of threshold voltages which can not be controlled as accurately as capacitor ratios [5]. Furthermore, only a single characteristic of the master filter, ω_0, is controlled by the phase-lock technique which is in general not sufficient to guarantee proper operation of the slave filters.

Another "Master–Slave" approach using voltage-controlled integrators instead of the FET's directly was presented recently [6] but it too requires matching of FET's

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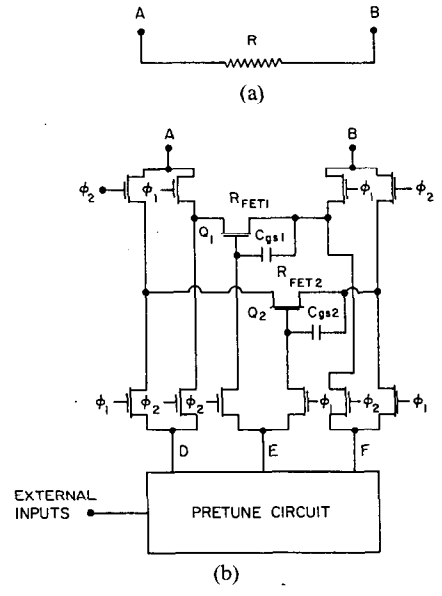


Fig. 1. Basic SR process. (a) Fixed resistor. (b) Switched resistor.

employed in the integrators for proper operation.

The SR approach presented in this paper pretunes each resistor in the *actual* filter so that the component values of the actual filter are compensated. The effective RC products of the filter are proportional to a ratio of capacitors (which may realistically be monolithic as in the SC approach) which can be typically controlled to about 0.1 percent in existing MOS processes. It is actually preferable to accurately determine RC products rather than absolute resistor or capacitor values since present manufacturing tolerances on absolute resistor and capacitor values are still quite large. The pretune circuit compensates for changes of temperature and for FET mismatch, thus eliminating the need of matching the less controllable FET characteristics.

A comparison of SR designs with the popular SC approach is justifiable since both are manufacturable with the same basic MOS process. Although the filter characteristics for both approaches are determined by capacitor ratios, the SR designs are capable of higher frequency operation and less subject to frequency warping and aliasing due to the inherently continuous-time nature of the filter response.

II. SR Structure

The basic SR structure is shown in Fig. 1 where the resistor R of Fig. 1(a) is ideally equivalent to the SR structure of Fig. 1(b). The FET's Q_1 and Q_2 are biased to operate in the ohmic region by appropriately restricting the magnitude of the drain to source voltage. The voltage on the gate–source capacitors is established by the pretune circuit so that ideally $R_{FET1} = R$ during clock phase ϕ_1 and $R_{FET2} = R$ during clock phase ϕ_2. The clocks ϕ_1 and ϕ_2 are assumed complementary and nonoverlapping. The clock frequency, f_c, determines the refresh rate but does not affect circuit performance provided $1/f_c$ is much smaller than the RC time-constant of the gate–source capacitance and the FET input impedance which can be practically established in the 0.1-s to 10-s range and higher.

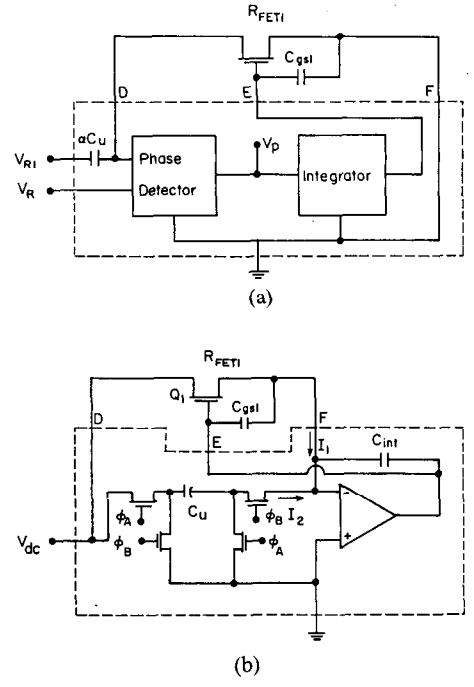


Fig. 2. Typical Pretune circuits during clock phase ϕ_1. (a) Phase locked. (b) Switched capacitor.

Many options exist for the design of the pretune circuit, the choice of which strongly affects the characteristics of circuits employing the SR's. Emphasis here will be placed upon precharge designs which will accurately determine the effective RC time-constants of passive or active RC filters employing the SR's. With this goal, two precharge schemes will be discussed.

Assume a passive or active RC filter is to be transformed to a SR structure by replacing all resistors by SR equivalents. Assume C_u is the unit capacitance for all capacitors in the original filter design and that α is a positive real number. One precharge circuit using a basic phase-lock approach is shown in Fig. 2(a) along with Q_1 (which is in the precharge state during clock phase ϕ_1). V_R is an external reference signal of frequency ω_R and 0° reference phase. The reference voltage V_{R1} is of the same frequency as V_R but shifted in phase by θ_R. The phase detector has a *time average* output voltage V_P, that relates monotonically in a sufficiently large interval about the zero crossing, θ_{D0}, to the phase at node D such as shown in Fig. 3. The phase detector drives an integrator which in turn determines the gate–source voltage stored on the gate–source capacitor C_{gs1}. This pretune circuit will force the first-order R_{FET1}-αC_u circuit to have a phase shift of θ_{D0} beteen nodes R_1 and D. It thus follows that during lock the value of $R_{FET1}C_u$ is given by

$$R_{FET1}C_u = \frac{\tan(90° - \theta_{D0} + \theta_R)}{\alpha\omega_R}. \tag{1}$$

Since the product of R_{FET1} and the unit capacitance is dependent only upon accurately controllable parameters (θ_{D0}, θ_R, and ω_R) and the capacitor ratio α it follows that the effective product of R_{FET1} and any capacitor in the filter is likewise dependent only upon θ_{D0}, θ_R, ω_R, and a

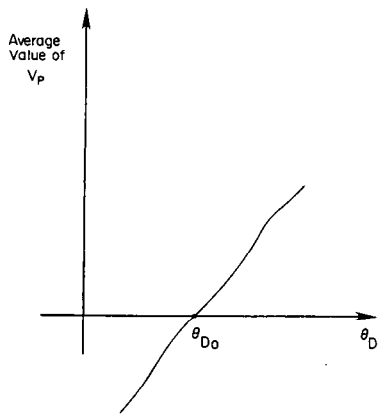


Fig. 3. Typical transfer characteristics of phase detector.

ratio of capacitors as desired. Although specific details about phase comparator designs will not be presented, one such scheme can be obtained by placing high-speed comparators at both inputs of the phase detector and using the outputs of these phase comparators to drive an "exclusive or" gate between two appropriately determined voltage levels while making $V_{R1} = V_R$ (i.e., $\theta_R = 0$). The choice of α, ω_R, and θ_{D0} remains to be made. If the original filter has equal R's and operates around ω_0, a practical choice of these parameters might be $\omega_R = \omega_0$, and $\theta_{D0} = 45°$. Note that this scheme actually requires only the reference V_R since V_{R1} has been chosen to equal to V_R. Another similar phase comparator scheme with $\theta_{D0} = 90°$ appears in the following example.

A second pretune circuit using a SC is shown in Fig. 2(b). In this figure, it is again assumed that operation is during clock phase ϕ_1 so that Q_1 is connected to the pretune circuit as indicated. For this circuit, note that the integrator output will be forced to a constant average value due to the feedback to the gate of Q_1. Assuming V_{dc} to be a constant dc voltage, this average value will be constant if and only if the average value of I_1 and I_2 are equal. If it is assumed that the clocks ϕ_A & ϕ_B are nonoverlapping and complementary with frequency f_c, the circuit shown will be locked provided that

$$C_u R_{\text{FET}} = 1/f_c.$$

Note that this pretune scheme is insensitive to stray capacitances associated with C_u, independent of temperature, and independent of the integrator capacitor C_{int}.

In filters involving a large number of SR's, the area devoted to the pretune circuits must be considered. A single pretune circuit, however, can be used to pretune several resistors since the time required to pretune a single MOS resistor will typically be much less than the period of the switching clock ϕ_1.

The frequency range over which these SR filters can operate is quite large since the filter itself behaves as a continuous-time circuit except at the switching times of the pretune circuit. The switching time can be negligible compared to practical clock frequencies which fall in the 0.1–10-Hz range. If a passive circuit is realized, operation should extend into the megahertz range and if active devices are employed they will generally determine the high-frequency limitations.

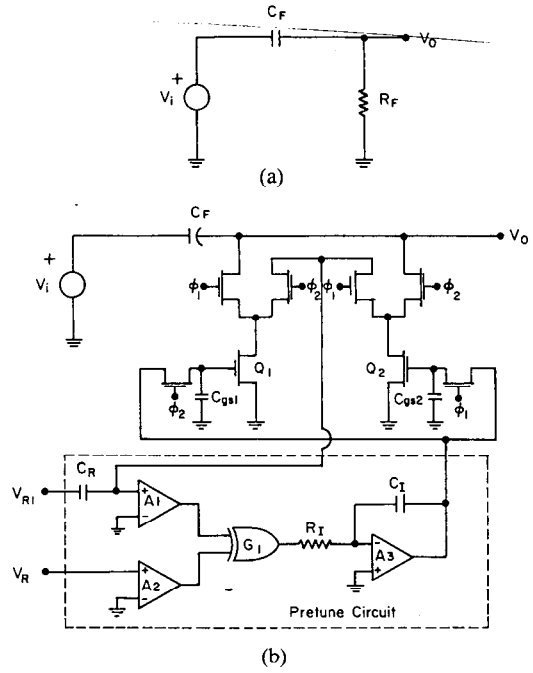


Fig. 4. Example of SR high-pass filter. (a) Parent passive structure. (b) Switched resistor.

The filter topology selection/synthesis problem will parallel that of the well-researched active RC approach. Many of the active RC filters should be directly applicable to SR techniques. It may prove desirable to consider minimum resistor and/or equal resistor and/or grounded resistor active RC filters.

III. Examples

A simple first-order highpass SR filter is shown in Fig. 4(b) along with the parent continuous-time circuit of Fig. 4(a). The pretune circuit is shown in the dashed box. For this circuit, assume

V_R	$= V_m \sin \omega_R t$
V_{R1}	$= V_{m1} \sin(\omega_R t + \theta_R)$
$R_I C_I$	$\gg 1/\omega_R$
A_1 and A_2	are high speed comparators
A_3	is an OP AMP
G_1	is an exclusive-or digital gate with symmetric output voltage levels.

If the additional assumptions that all active devices are ideal and that the time-constants of the gate capacitor-FET input impedances are much larger than the period ϕ_2 it follows from (1) that the circuit of Fig. 4(b) behaves like the circuits of Fig. 4(a) with an equivalent resistance of

$$R_{FEQ} = \frac{\tan(90° - 90° + \theta_R)}{C_R \omega_R} = \frac{\tan \theta_R}{C_R \omega_R}. \tag{2}$$

Stated alternately, the 3-dB cutoff frequency of the circuit of Fig. 4(b) is given by

$$\omega_{3\,\text{dB}} = \frac{C_R \omega_R}{C_F \tan \theta_R}. \tag{3}$$

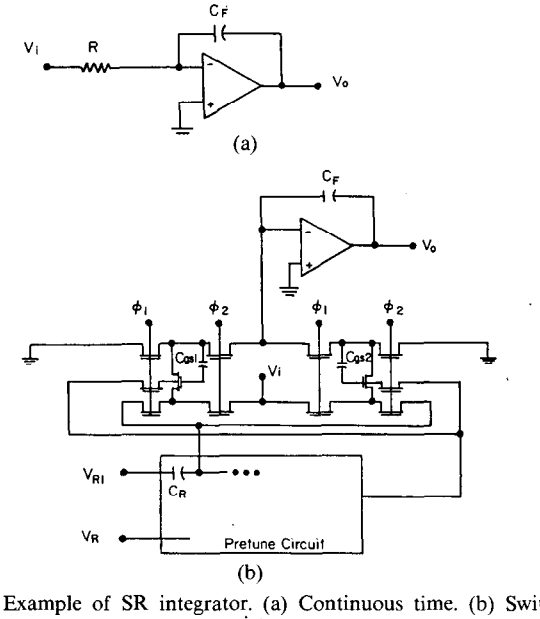


Fig. 5. Example of SR integrator. (a) Continuous time. (b) Switched resistor.

Note that the filter performance is essentially independent of $R_I, C_I, C_{gs1}, C_{gs2}$, period of clocks, V_m, and V_{m1}. If the ratio of C_R to C_F is accurately controlled, as can be currently accomplished in standard monolithic processes, it follows that the characteristics of the filter are accurately controllable.

An integrator is shown in Fig. 5(a) along with a SR version in Fig. 5(b). The pretune circuit is identical to that of Fig. 4(b). Assuming ideal operational amplifiers and ideal operation of the SR network, the unity gain frequency of the circuit of Fig. 5(b) is given by

$$\omega_0 = \frac{C_R \omega_R}{C_F \tan \theta_R}. \tag{4}$$

IV. Theoretical Analysis

In this section the effects of the switched resistors, will be investigated on a theoretical basis. This analysis will be restricted to the circuit of Fig. 4(b) and is used to quantitatively justify the simplified derivation of (2) and (3).

First, assume the FET's are identical MOS devices operating in the ohmic region with drain–source characteristics given by [7]

$$\frac{V_{DS}}{I_0} = R_{\text{FET}} \simeq \left(\frac{L}{u_n W C_{0x'}}\right)\left(\frac{1}{V_{GS} - V_T}\right) = \frac{R_{F1}}{V_{GS} - V_T} \tag{5}$$

where the definition of the process and geometric parameters is standard and the constant R_{F1} has units ohm·volts. The gate–source port of the FET will be assumed to be modeled by a resistor, R_G, in shunt with a capacitor of value, C_G. If $C_{gs1} = C_{gs2} = C_{gs}$, the time-constant of the first-order gate circuit is defined by

$$T_G = R_G(C_G + C_{gs}). \tag{6}$$

Assume ϕ_1 and ϕ_2 are complementary (nonoverlapping) clocks that have period $2T$ and that time is referenced to start the clocks at $t = 0$. It thus follows that the FET resistance, which is periodic with period T, is defined during the fundamental period while it is in the filter circuit by

$$R_{\text{FET}}(t) = \frac{R_{FEQ}}{e^{-t/T_G} + \theta(e^{-t/T_G} - 1)} \tag{7}$$

where

$$\theta = \frac{V_T R_{FEQ}}{R_{F1}} \tag{8}$$

and R_{FEQ} is the desired FET impedance which will be defined by (2). The filter circuit of Fig. 4(b) satisfies the differential equation

$$\frac{dV_0(t)}{dt} = A(t)V_0(t) + f(t) \tag{9}$$

where

$$f(t) = \frac{dV_i(t)}{dt} \tag{10}$$

and

$$A(t) = -\frac{1}{C_F R_{\text{FET}}(t)}. \tag{11}$$

Since $A(t)$ is periodic with period T, (9) is recognized as a first-order linear differential equation with periodic coefficients. Closed-form expressions for the solution of this equation are readily available [8], [9] but are, in general, quite unwieldly to solve parametrically. We are interested here, rather, in the steady-state response due to a sinusoidal excitation and in the spectral content of this response.

Assume the excitation is given by

$$V_i = V_S \sin \omega_s t. \tag{12}$$

With this excitation, it follows [8] that the steady-state response is given by

$$V_0(t) = \beta_0 \sin(\omega_s t + \nu_0) + \sum_{k=1}^{\infty} \beta_{kf} \sin(\omega_s t + k\omega t + \nu_{kf}) + \sum_{k=1}^{\infty} \beta_{kb} \sin(\omega_s t - k\omega t + \nu_{kb}) \tag{13}$$

where

$$\omega = \frac{2\pi}{T} \tag{14}$$

and where all β's and ν's are real. Unfortunately, the expressions for the β and ν parameters are not readily obtainable in explicit form. Approximate explicit expressions, however, will be given for ν_0 and the β parameters.

Since $A(t)$ is periodic, it may be expressed as a Fourier series by

$$A(t) = \sum_{k=-\infty}^{\infty} \tilde{C}_k e^{jk\omega t}. \tag{15}$$

From (6) and (10) it follows that

$$\tilde{C}_0 = \frac{\left(T_G(1+\theta)(e^{-T/T_G} - 1) + \theta T\right)}{TT_F} \tag{16}$$

and

$$\tilde{C}_k = \frac{T_G(1+\theta)(e^{-T/T_G}-1)}{TT_F\left(1+\frac{KT_G 2\pi}{T}j\right)} \tag{17}$$

where

$$T_F = C_F R_{FEQ}. \tag{18}$$

It can now be shown that for small T, the desired parameters in (13) can be approximated by

$$\beta_0 \simeq \frac{\omega_s V_s}{\sqrt{|\tilde{C}_0|^2+\omega_s^2}}$$

$$\nu_0 \simeq \tan^{-1}\left(\frac{\tilde{C}_0}{\omega_s}\right) \tag{19}$$

and

$$|\beta_{kf}| = |\beta_{kb}| \simeq \frac{|\tilde{C}_k|\omega_s V_s}{\sqrt{k\omega|\tilde{C}_0|^2+\omega_s^2}}. \tag{20}$$

It thus follows that the ratio of the sidelobe magnitudes to that of the fundamental is given by

$$\gamma_k = \frac{|\tilde{C}_k|T}{2\pi k} = \frac{T_G(1+\theta)(1-e^{-T/T_G})}{T_F 2\pi k\sqrt{1+\left(\frac{T_G}{T}\right)^2 k^2 4\pi^2}}. \tag{21}$$

Since typically $T_G > T$, this can be approximated by

$$\gamma_k \simeq \frac{T(1-e^{-T/T_G})(1+\theta)}{T_F 4\pi^2 k^2}. \tag{22}$$

It can be seen that this quantity is a decreasing function of k and T_G and an increasing function of T.

A bound for the steady-state response in the time domain can also be obtained. It can be shown that if $V_{OI}(t)$ is the sinusoidal steady-state response of the filter in the ideal case that $R_{\text{FET}}(t) = R_{FEQ}$, then for all t the actual steady-state response satisfies the expression

$$|V_0(t) - V_{OI}(t)| \leq \frac{(1+\theta)(1-e^{-T/T_G})}{e^{-T/T_G}(1+\theta)-\theta}|V_{OI}|_{\max} \tag{23}$$

where $|V_{OI}|_{\max}$ is the peak value of the sinusoidal waveform $V_{OI}(t)$. This bound is actually quite loose but will suffice for what follows.

A quantitative measure of γ_k and the error bound in the time domain for typical applications is useful for dictating the importance of including the sidelobes, and indeed the time dependence of $R_{\text{FET}}(t)$, in the analysis. For SR circuits designed to operate from a few hundred hertz to a few megahertz, it is reasonable to design the filter with typical component values so that

$$\frac{T}{T_G} < 10^{-3}$$

$$\frac{T_G}{T_F} > 10^6. \tag{24}$$

For these design constraints, it follows from (22) and (23) that for $V_{GS} = 3V_T$ (i.e., $\theta = 0.5$)

$$\gamma_k < \frac{3.8\times 10^{-2}}{k^2} \tag{25}$$

and

$$|V_0(t) - V_{OI}(t)| \leq 0.0015|V_{OI}|_{\max} \tag{26}$$

indicating that the first sidelobes are over 28 dB down from the fundamental and subsequent lobes are considerably lower. From (26) it can be concluded that the time-domain waveform differs very little from that obtained in the ideal case. It can be concluded that in many applications the sidelobes for this circuit can be neglected and the analysis can be carried out by assuming a time independent FET resistance

$$R_{\text{FET}}(t) \simeq R_{FEQ}. \tag{27}$$

The exact theoretical analysis of the SR integrator of Fig. 5(b) is similar to that for the high-pass filter. The exact theoretical analysis of higher order SR filters appears very tedious and a closed-form parametric solution is unlikely. Although the theoretical analysis presented applies only to this example it is reasonable to expect that one can neglect the time dependence of $R_{\text{FET}}(t)$ when analyzing more general structures provided T and T_G are chosen so that the changes of $R_{\text{FET}}(t)$ are small during intervals of length T. The changes in $R_{\text{FET}}(t)$ can be made arbitrarily small by increasing C_{gs} for any filter structure.

V. Experimental Results

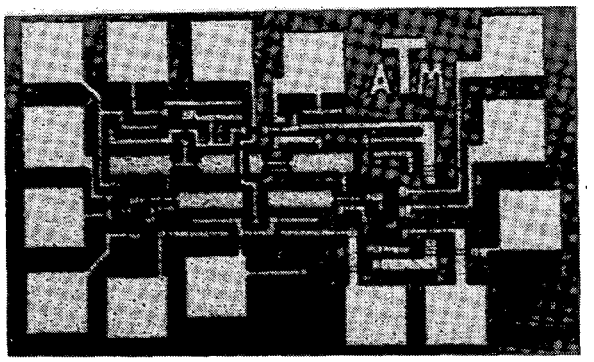
The circuit of Fig. 4(b) was evaluated in the laboratory using discrete active and passive components. The measured values for the components are listed in Table I for three different test frequencies at which the filter was evaluated. Relatively large valued capacitors were used in this evaluation so that instrumentation and switch parasitics would be negligible. Comparators A_1 and A_2 were of type LM361. The "exclusive-or" gate was constructed from a T^2L 7486 followed by a 7404 and two analog switches to drive R_I (which was duplicated) by the well-defined voltages of either +5 V or −5 V. The amplifier A_3 was a LF356. The FET's were ECG465 devices that were intentionally mismatched.

The steady-state cutoff frequencies during the states ϕ_1 and ϕ_2 (f_{0,ϕ_1} and f_{0,ϕ_2}, respectively) are also compared in Table I with the theoretical (f_0) obtained assuming $R_{\text{FET}}(t) = R_{FEQ}$. As can be seen the percent error between the theoretical cutoff frequency and that obtained during either ϕ_1 or ϕ_2 is less than 4 percent at all test frequencies. The observed change in the frequency response during either phase ϕ_1 or ϕ_2 was quite negligible as expected since T_g (>1000 s) was quite large compared to T. Considerably better accuracy can be expected in monolithic form.

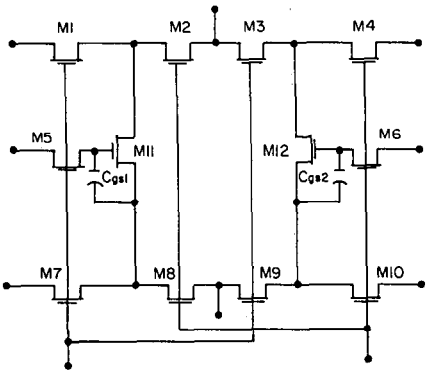
An integrated version of a SR pair was designed and fabricated in a double-poly NMOS process. A microphotograph of the die of this building block is shown in Fig. 6(a) along with the electrical equivalent of Fig. 6(b). The design

TABLE I
TEST CONDITIONS AND EXPERIMENTAL PERFORMANCE FOR CIRCUIT OF FIG. 4(B)

	Test 1	Test 2	Test 3
C_F	100. nf	9.999 nf	10.107 nf
R_{FEQ}	1.59 KΩ	1.59 KΩ	1.44 KΩ
T	10 sec.	10 sec.	10 sec.
ω_r	(2π)1.0 K rad/sec.	(2π)0.996K rad/sec.	(2π)99.93 K rad/sec.
ϕ_r	45°	45°	45°
C_R	100. nf	9.999 nf	1.106 nf
C_{g1}, C_{g2}	10 nf	10 nf	10 nf
f_o	1.999 KHz	10.00 KHz	99.93 KHz
f_o, ϕ_1	1.003 KHz	10.38 KHz	102.4 KHz
f_o, ϕ_2	1.003 KHz	10.16 KHz	99.63 KHz



(a)



(b)

Fig. 6. Integrated SR building block. (a) Microphotograph. (b) Equivalent circuit.

W/L for M1−M10 was 1 mil/0.3 mil and for M11 and M12 was 0.3 mil/1 mil. The design value for the gate capacitors C_{gs1} and C_{gs2} was 1.24 pF. This building block was used to investigate the effects of the gate holding capacitor and switch mismatch. No attempt to measure effective RC time constants was made at this point since the pretune circuit was external in this evaluation.

The integrated building block was evaluated experimentally in the circuit of Fig. 4(b) at room temperature. The pretune signal, V_{R1}, and C_F were determined and fixed so the filter cutoff frequency was approximately 800 Hz. A clock frequency of 0.5 Hz was used. Fig. 7 shows a plot of frequency response of the filter for phases ϕ_1 and ϕ_2 at the start, middle, and end of each phase. The time-domain effects of the gate voltage droop and the comparisons between phases ϕ_1 and ϕ_2 are shown in Fig. 8 where the input frequency is maintained at 1 kHz (clocking is superimposed at the top of the photograph). From these results, the effects of switch mismatch appear negligible. From Figs. 7 and 8 it can be seen that the gate-holding capacitor

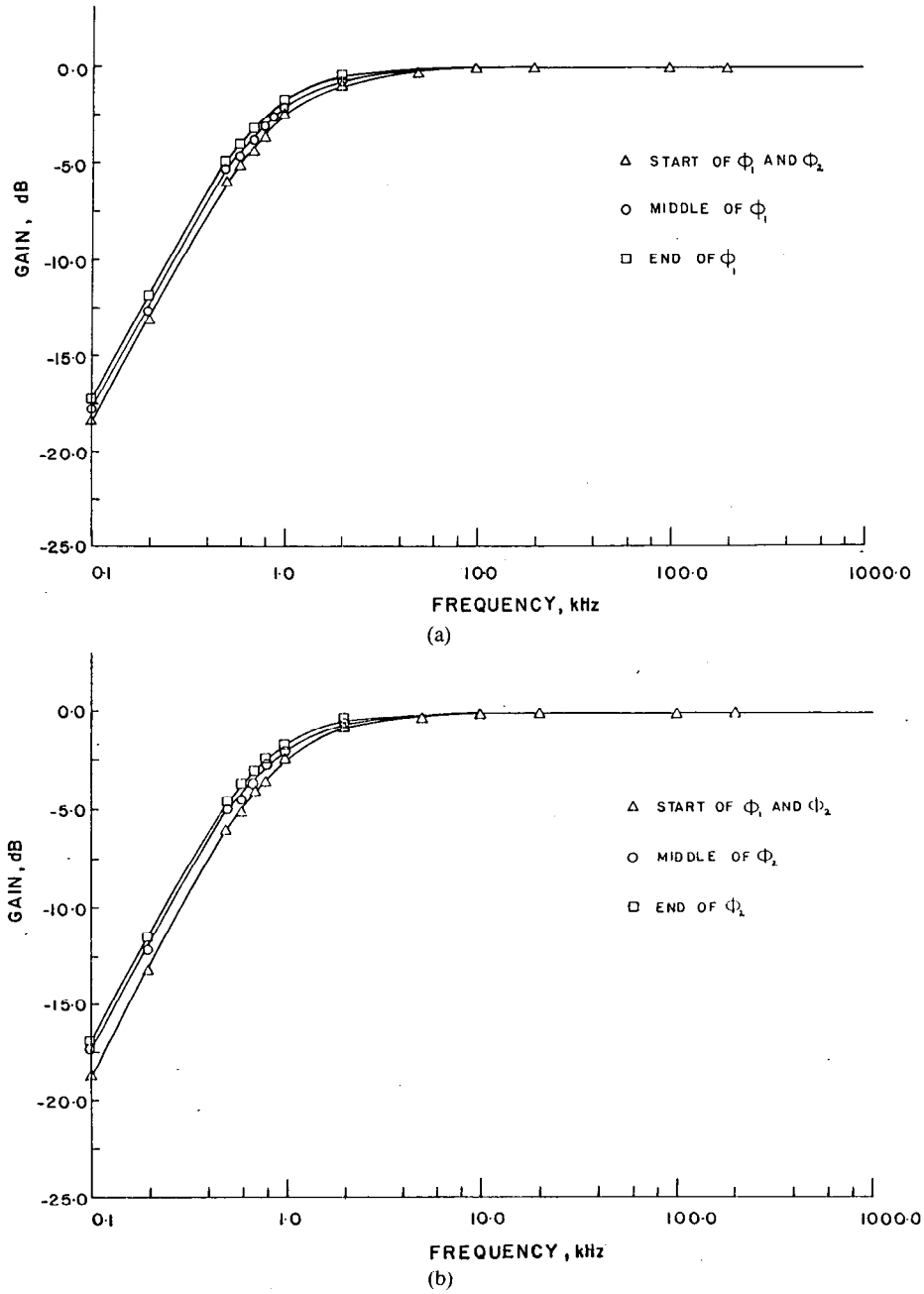


Fig. 7. Experimental response of first-order filter with integrated SR block. (a) Phase ϕ_1. (b) Phase ϕ_2.

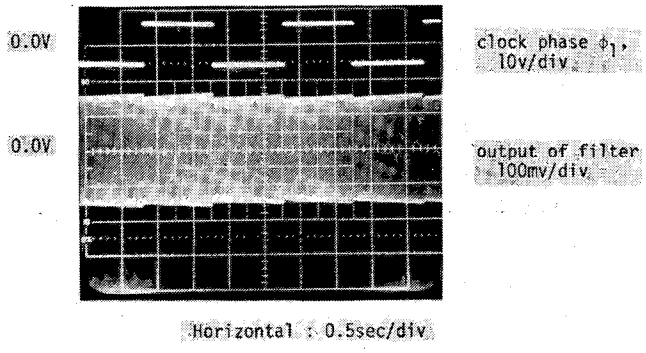


Fig. 8. Filter output during clock phases ϕ_1 and ϕ_2. *Top*: waveform of clock phase ϕ_1, frequency $f_c = 0.5$ Hz (ϕ_1 and ϕ_2 are nonoverlapping complementary clocks). *Bottom*: waveform of the filter output, input frequency $f = 1$ kHz.

does discharge somewhat with a 0.5-Hz clock causing a modest shift in cutoff frequency. These effects can be reduced by either increasing the clock frequency or increasing the size of the gate-holding capacitor.

The integrator of Fig. 5(b) was also evaluated in the laboratory. An external pretune circuit identical to that used for the high-pass filter was employed. The balance of the filter was integrated in a double-polysilicon NMOS process. Two separate SR's with mismatched W/L ratios were attached to the summing node of the operational amplifier to investigate the mismatch effects. A microphotograph of the die of this integrator is shown in Fig. 9 and the equivalent circuit is shown in Fig. 10. The operational amplifier is identical to that discussed in [10]. The design

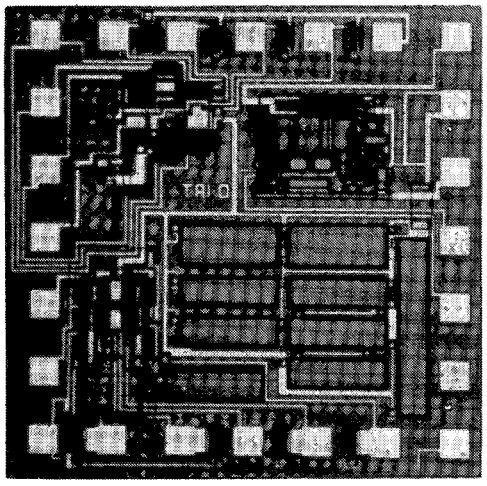


Fig. 9. Microphotograph of SR integrator.

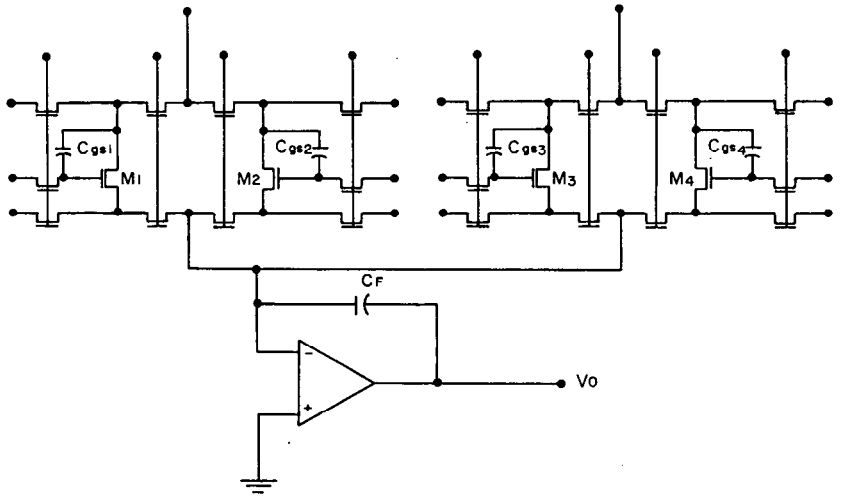


Fig. 10. Equivalent circuit of SR integrator.

W/L ratios of the MOSFET's and capacitor values, exclusive of those in the operational amplifier, can be obtained from Table II. A large external feedback resistor, $R_{Fb} = 3.52$ MΩ, was placed in shunt with C_F to compensate for offset voltage and bias current of the operational amplifier. The phase-locked pretune circuit maintained lock over more than one octave change in the reference frequency for both the M1–M2 and M3–M4 SR pairs. This corresponds to a comparable change in the unity gain frequency of the integrator.

As in the previous example, no attempt will be made to determine the absolute accuracy of the unity gain frequency as related to C_F, C_R, ω_R, and θ_R since the pretune circuit is external. To investigate the effects of mismatch of the $M1-M2$ and $M3-M4$ SR pairs and the accuracy of the pretune circuit for various pretune frequencies, the nominal value of C_F was experimentally obtained from the theoretical expression relating the unity gain frequency of the integrator to ω_R, θ_R, C_R and the external feedback resistor. Using the $M3-M4$ SR pair and a pretune frequency of 560 Hz a unity gain frequency of 1.93 kHz was measured. The switching rate was maintained at 50 Hz. From the measured values of θ_R and C_R, a nominal value of $C_F = 100.2$ pF was calculated. This compares to a design value of $C_F = 108.14$ pF. Using this nominal value for C_F, the theoretical unity gain frequency was calculated

TABLE II
DESIGN PARAMETERS FOR SWITCHED-RESISTOR INTEGRATOR OF FIG. 10

Capacitor	Design Capacitance	
C_{gs1}-C_{gs4}	9.74 pf ± .2 pf	
C_F	108.14 pf	
Transistor	**W**	**L**
M1, M2	.3 mil	10 mil
M3, M4	.3 mil	5 mil
All other MOSFETs shown in Fig. 10	2.7 mil	.3 mil

TABLE III
EFFECTS OF DEVICE MISMATCH ON SWITCHED-RESISTOR INTEGRATOR

		Unity Gain Frequency		
Devices	$f_R=\omega_R/2\pi$	Theoretical	Experimental	% error
M1-M2	400	.870KHz	.869KHz	-.1
M1-M2	550	1.44KHz	1.43KHz	-.7
M3-M4	760	3.32KHz	3.36KHz	+1.2
M3-M4	1000	4.58KHz	4.58KHz	-

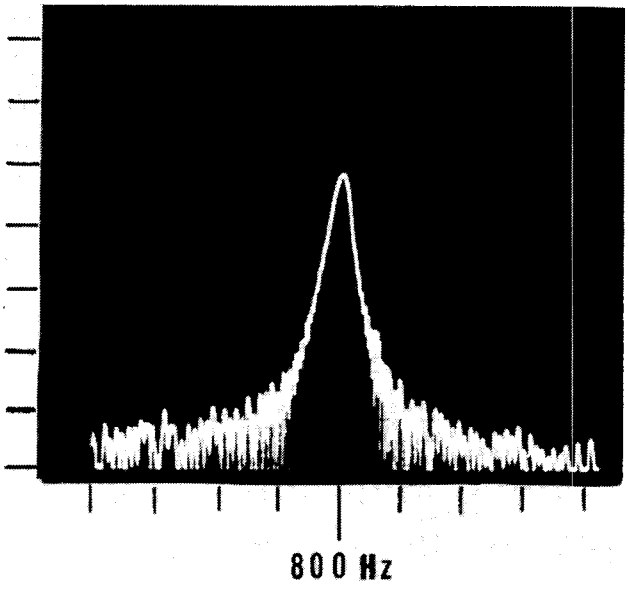


Fig. 11. Spectral response of integrator of Fig. 5(b) with a clock rate of 5 Hz. 50 Hz/div. horizontal, 10 dB/div. vertical.

for several different pretune frequencies from the measured values of θ_R and C_R and compared with the experimental. These results are summarized in Table III. From this table, it appears that the effects of device mismatch and changes in phase of the pretune circuit are quite modest.

It must be emphasized that no conclusions about absolute accuracy are to be drawn from this table since the theoretical unity gain frequency was calculated from the nominal value of C_F. The effects of signal distortion on this integrator were experimentally investigated. The pretune frequency was adjusted for a unity gain frequency of 800 Hz. With an 800-Hz excitation the spectral response shown in Fig. 11 was obtained for a clock frequency of 5 Hz. The presence of the sidelobes at $f=800\pm 5n$ can be seen as anticipated from the previous analysis but their affects will not be significant in many applications.

Design Considerations for SR Networks

In this section we will attempt to outline some of the practical considerations and limitations of the SR approach:

1) The L/W ratios of the MOS switches should be selected so that the switch "on" impedance is small compared to the SR impedances in the circuit.

2) The dynamic range is limited by the linearity of the MOSFET in the ohmic region. This can be increased with depletion devices and/or large gate to source voltages.

3) C_{gs} should be large enough so that parasitic switch and poly-capacitances to the gates do not cause a significant change in the gate to source voltage when the MOSFET is switched from the pretune circuit to the filter circuit. It should be pointed out, however, that cancellation of clock feedthrough effects to the gate-holding capacitor occur if identical switches are used to connect R_{FET} to the pretune circuit.

4) The parasitic capacitance associated with the SR's should be considered when designing the filter if the pretuned resistance is large.

5) The clock controlling the gate-holding capacitor should be nonoverlapping.

6) In a circuit employing a large number of SR's, one must consider the tradeoffs between using a single pretune circuit with relatively complicated clocking schemes compared to multiple pretune circuits and very simple clocking.

VI. CONCLUSIONS

A new method of designing MOS compatible active filters has been presented which employs SR techniques. The characteristics of these filters were shown to be dependent upon ratios of capacitors as in SC designs and hence the filter characteristics are largely independent of process parameters.

One of the major advantages of using SR structures instead of SC designs is the capability of designing monolithic high-frequency filters since the filter is essentially continuous-time in nature rather than sampled data.

A comparison of theoretical and experimental results for two simple SR configurations were presented which correlated quite closely. The experimental results were based upon both a discrete version and an integrated design.

SR techniques may well offer a superior alternative to SC configurations in the design of monolithic filters in some applications. A combination of SR and SC designs on a single chip also seems practical and should provide a significant increase in flexibility for the circuit designer.

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