Modeling of MOS Transistors with Nonrectangular-Gate Geometries

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Abstract—**The dc electrical characteristics of MOS transistors with nonrectangular-gate geometries are investigated. Closed-form analytical expressions relating the terminal characteristics to the geometric parameters are presented for several gate geometries including the trapezoid, "V," "L," and annulus.**

Experimental results based upon a specially fabricated NMOS test bar containing these nonrectangular devices are presented. A comparison of the theoretical and experimental results is made which shows close agreement.

I. INTRODUCTION

THE SHAPE and dimensions of the gate of MOSFET transistors are generally the only device parameters controllable by the integrated-circuit design engineer once the process parameters have been specified. Typically the designer utilizes the rectangular-shaped gate whenever possible. This approach is commonplace since the rectangular geometry is convenient for layout, component density can be high, and good models for this device have been developed.

Nonrectangular devices are (e.g., trapezoidal, "L"-shaped, "V"-shaped, etc.) occasionally used, however. Those devices are particularly useful when it is of paramount importance to fit a given amount of circuitry into a predetermined region on the die or when extreme device lengths or widths are required. Unfortunately, utilization of these nonrectangular MOSFET's is limited by the unavailability of suitable device models. Even in the seemingly simple case of an "L"-shaped transistor there are differing opinions as to what the actual "equivalent length" and "equivalent width" are, or if, indeed, such an equivalence exists.

One industrial group with which the authors had become familiar recently had need of a nonrectangular device with specific characteristics. They addressed the problem of modeling their devices by fabricating on a separate test bar a family of devices of the required shape, but with varying dimensions, and experimentally extracting the information necessary for characterization. The inherent time delay and fabrication costs often make such an approach impractical.

Aside from, but directly associated with the problem of modeling nonrectangular-gate MOSFET's, is the question of what effects, if any, does the designer controllable shape have on performance and can this parameter be advantageously utilized to optimize circuit performance.

Richman [1] considered the problem, in 1967, by posing the question and fabricating special test devices, however, no quantitative results were presented. He was particularly

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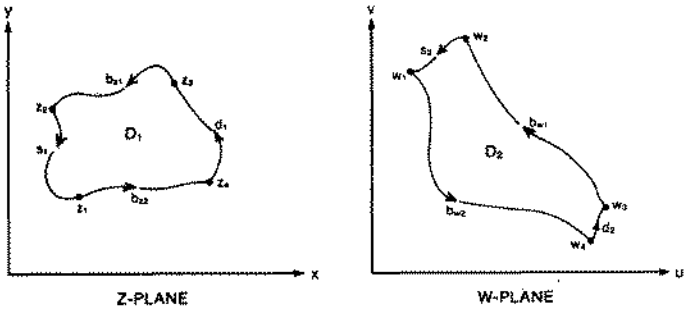

Fig. 1. MOS transistors with arbitrarily shaped gate geometries.

interested in the effects of device geometry on parasitic capacitances and transconductance gain.

Rao and Carr considered trapezoidal MOSFET's in two papers in the early 1970's [2], [3] and presented simple, closed-form parametric expressions for the dc relationships between I_D, V_{DS}, and V_{GS}. Unfortunately, their expressions are invalid as pointed out by Hemmert [4]. In the same paper, Hemmert presented his own solution to the trapezoidal problem by following the basic approach Wick [5] used to investigate the Hall effect in gyrators. It will be shown here that although his approach is correct, Hemmert's solution to the trapezoidal problem is also invalid. Closed-form explicit parametric expressions will be presented for the dc terminal characteristics of several common nonrectangular-gate MOS transistors.

II. Analysis of Nonrectangular Transistors

Several theorems relating to modeling arbitrarily shaped nonrectangular MOSFET's, in the ohmic region, are presented in this section. These results will be utilized subsequently. For notational convenience, the development will be for n-channel devices.

Consider the two-dimensional "top view" of an arbitrary MOSFET shown in Fig. 1(a) where the curves s_1, b_{z1}, d_1, and b_{z2} form a simple closed curve which is the boundary of the gate. The gate is assumed to be perfectly conducting. The curve segments d_1 and s_1 serve as the drain and source contacts, respectively, and are nonintersecting. The location and orientation of the origin in the x-y plane is arbitrarily located, as shown in Fig. 1.

The physical model of the device will be the same as that used by Sah [6] to obtain the simple dc electrical model for rectangular devices of channel length L and width W operating in the ohmic region typically used for design purposes

$$I_D = \frac{uC_{ox}W}{2L}\left(2(V_{GS} - V_T) - V_{DS}\right)V_{DS}, \quad \text{for } V_{DS} < V_{GS} - V_T \tag{1}$$

where V_T is the threshold voltage, u is the channel mobility, and C_{ox} is the oxide capacitance per unit area. I_D, V_{GS}, and V_{DS} denote the drain current, gate-to-source voltage, and drain-to-source voltage, respectively.

In what follows, it will be assumed, without loss of generality, that $V_s = 0$ (i.e., the source serves as the voltage reference). The channel will be assumed to be of a constant thickness, z_0.

The z-component (the z-axis is perpendicular to the x-y plane of Fig. 1) of the electrical field in the channel is assumed negligible compared to the component in the x-y plane, allowing one to express the channel voltage at the point (x, y, z) as $V(x, y)$ which will be represented as V for notational convenience. The threshold voltage is assumed to be independent of position. Assuming z_0 is arbitrarily small, the mobile-sheet charge density at the point (x, y) in the channel is given by

$$\rho_{ms} = C_{ox}\left[V_{GS} - V_T - V\right]. \tag{2}$$

The sheet conductivity of this layer is given by

$$\sigma_{ms} = u\rho_{ms} \tag{3}$$

where u is the surface mobility of the electrons in the channel. Let $\boldsymbol{J}$ and $\boldsymbol{E}$ represent the sheet current density and electric-field vectors, respectively, in the channel. It thus follows from Ohm's law and the continuity equation that

$$\boldsymbol{J} = \sigma_{ms}\boldsymbol{E} \tag{4}$$

$$\nabla \cdot \boldsymbol{J} = 0 \tag{5}$$

where the electric field is given by

$$\boldsymbol{E} = -\nabla V. \tag{6}$$

Substituting (2), (3), (4), and (6) into (5) we obtain the differential equation

$$(V_{GS} - V_T - V)\nabla^2 V - \nabla V \cdot \nabla V = 0 \tag{7}$$

which along with the boundary conditions

$$V(x, y) = 0, \quad \text{along } s_1$$

$$V(x, y) = V_{DS}, \quad \text{along } d_1$$

$$\boldsymbol{n}(x, y) \cdot \boldsymbol{E} = 0, \quad \text{along } b_{z1} \text{ and } b_{z2}$$

(where $\boldsymbol{n}(x, y)$ is a unit vector normal to the boundary at the point (x, y) on the boundary) totally governs the operation of the device. It remains to express the drain current, I_D, in terms of V_{GS} and V_{DS}. If we let γ represent any simple curve extending from b_{z1} to b_{z2}, the current I_D can be obtained from the line integral along γ from the equation

$$I_D = \int_\gamma \boldsymbol{J} \cdot \boldsymbol{n}\, dl \tag{8}$$

where $\boldsymbol{n}$ is the unit vector normal to γ (oriented toward the source). If we now assume γ is any equal potential surface obtained by solving (7) (which must extend from b_{z1} to b_{z2}), it follows that $\boldsymbol{J}$ is everywhere perpendicular to γ so that (8) becomes

$$I_D = \int_\gamma |\boldsymbol{J}|\, dl = u\, C_{ox}\left[V_{GS} - V_T - V\right]\int_\gamma |\nabla V|\, dl. \tag{9}$$

The solution of (7) and the subsequent solution of (9) required to obtain the device model are, in general, unwieldly. These equations are, however, readily solvable in the case where the gate geometry is rectangular. The Riemann mapping theorem [7] will now be used to transform a nontractable gate geometry into a rectangular geometry. Two

theorems will then be presented that allow one to obtain the solution of the arbitrarily shaped gate directly from the solution in the rectangular case.

Riemann Mapping Theorem

Let D_1 and D_2 be simply connected domains in the Z-plane and W-plane, respectively. There then exists a univalent function T such that $W = T(z)$ maps D_1 onto D_2.

The mapping can be chosen so that the boundary points z_1, z_2, z_3, and z_4 map to the points w_1, w_2, w_3, and w_4 as shown on Fig. 1. Note that this maps the source and drain contacts s_1 and d_1 to s_2 and d_2, which will be taken as the source and drain contacts of the transformed device in the W-plane. The following two theorems are readily proven [8].

Theorem 1: Assume $V_1(x, y)$ is a real valued function defined on a domain D_1 in the Z-plane and T is a univalent transformation of D_1 onto the domain D_2 in the W-plane. Define the real valued function $V_2(u, v)$ on the domain D_2 by

$$V_2(u, v) = V_1(T^{-1}(u, v)). \tag{10}$$

Then if V_1 satisfies the differential equation

$$(a - V_1)\nabla^2 V_1 - (\nabla V_1 \cdot \nabla V_1) = 0 \tag{11}$$

with boundary conditions

$$V_1(x, y) = 0, \quad \text{on } s_1$$
$$V_1(x, y) = V_{DS}, \quad \text{on } d_1$$
$$\boldsymbol{n} \cdot \boldsymbol{E}_1 = 0, \quad \text{on } b_{z1} \text{ and } b_{z2}$$

where a and V_{DS} are real constants and $\boldsymbol{E}_1 = -\nabla V_1$, then $V_2(u, v)$ satisfies the differential equation

$$(a - V_2)\nabla^2 V_2 - (\nabla V_2 \cdot \nabla V_2) = 0 \tag{12}$$

with boundary conditions

$$V_2(x, y) = 0, \quad \text{on } s_2$$
$$V_2(x, y) = V_{DS}, \quad \text{on } d_2$$
$$\boldsymbol{n} \cdot \boldsymbol{E}_2 = 0, \quad \text{on } b_{w1} \text{ and } b_{w2}.$$

Theorem 2: Let T, D_1, D_2, V_1, and V_2 be as defined in theorem 1 and let γ_1 be the "equal potential" curve in D_1 defined by $V_1(x, y) = k$ where k is a real constant that satisfies

$$0 \leqslant k \leqslant V_{DS}$$

and γ_2 is the image under T of γ_1. Then, the drain currents of the two devices, I_{DZ} and I_{DW}, which are expressible by

$$I_{DZ} = h \int_{\gamma_1} [a - V_1] |\nabla V_1| \, dl_1 \tag{13}$$

$$I_{DW} = h \int_{\gamma_2} [a - V_2] |\nabla V_2| \, dl_2 \tag{14}$$

where h is a real constant, satisfy the equation $I_{DZ} = I_{DW}$.

If we define a and h by

$$a = V_{GS} - V_T$$
$$h = uC_{ox} \tag{15}$$

then, from (7), (9), and theorems 1 and 2 we can obtain the expression for the drain current of the device in the Z-plane in terms of V_{GS} and V_{DS} by solving for V_2 in (12), solving for I_{DW} in (14), and then equating I_{DZ} and I_{DW}. Alternately, we can solve for the current I_{DZ} and equate I_{DZ} and I_{DW} to obtain I_{DW}. As stated earlier, the direct solution of the pairs of equations which characterizes an arbitrarily shaped transistor is generally unwieldly. We will intentionally choose the mapping T so that the solution of (12) and (14) or the solution of (11) and (13) is tractable or already known.

A solution of (11) and (13) for the case that the device is a rectangle (with vertexes in the Z-plane defined by $z_1 = (0, 0)$, $z_2 = (0, W)$, $z_3 = (L, W)$, and $z_4 = (L, 0)$) with length L and width W is given by

$$V_1 = a - \sqrt{a^2 + \frac{2x}{L}\left(\frac{V_{DS}^2}{2} - aV_{DS}\right)}, \quad \text{for } (x, y) \in D_1 \tag{16}$$

and

$$I_{DZ} = \frac{hW}{L}\left[aV_{DS} - \frac{V_{DS}^2}{2}\right]. \tag{17}$$

Although the details of the solution are not presented, the solutions are readily derivable from (11) and (13). It can be observed from (16) that $V_1(x, y)$ is not dependent upon the y variable, an *assumption* that is often made when analyzing rectangular-gate MOS transistors. Substituting into (17) the constants a and h given in (15) yields Sah's equation (1).

Two interesting observations can be made at this point.

Observation 1: The functional form of the relationship between V_{DS}, V_T, and V_{GS} is not affected by gate geometry. For an arbitrarily shaped device an equivalent rectangular-gate transistor exists and the device geometry only affects the "equivalent" W/L ratio. As a consequence, all devices are electrically symmetric with respect to the drain and source, even though they may not be geometrically symmetric.

Observation 2: If the boundaries b_{z1} and b_{z2}, in Fig. 1, serve as the source and drain (or drain and source) contacts, respectively, then the equivalent W/L for this device is the reciprocal of the equivalent W/L for the device initially considered.

Since Riemann's mapping theorem guarantees the existence of a univalent mapping of any device with a gate bonded by a simple closed curve to a rectangular device, Observation 1 follows from (17) and the fact that the rectangular-gate transistors are electrically symmetric with respect to drain and source. If we select a rectangular-gate device in the W-plane of Fig. 1, observation 2 follows from the facts that the mapping T which maps s_1 to s_2 also maps b_{z1} and b_{z2} to b_{w1} and b_{w2}, and that the reciprocal relationship for interchanging contact sides is valid for rectangular devices.

It should be emphasized that the preceeding analysis and

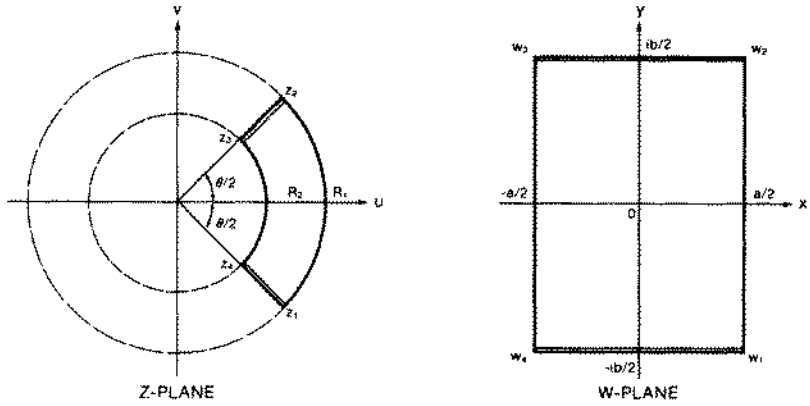

Fig. 2. Mapping of a rectangle onto a ring.

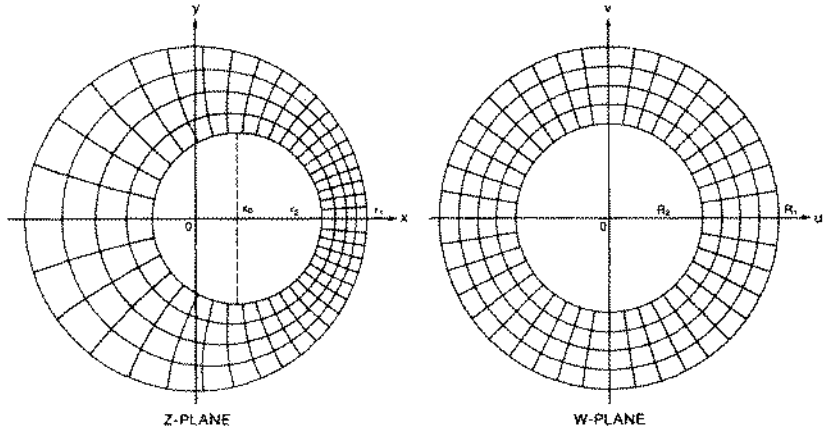

Fig. 3. Mapping of eccentric-ring onto concentric annulus.

conclusions are valid only for the dc physical model presented. Device geometry does affect parasitic capacitances, channel modulation, electrical symmetry in the saturated region, and short-channel device performance.

III. Applications

Several devices with nonrectangular gates are analyzed in this section. These analyses all utilize the univalent transformation approach of theorem 1.

A. Ring-Gate Devices

Consider the ring-gate transistor shown in Fig. 2. A univalent mapping of this rectangle in the W-plane to the ring-gate device in the Z-plane is given by

$$z = e^{w} \tag{18}$$

where the segments $[w_1, w_2]$, $[w_2, w_3]$, $[w_3, w_4]$, and $[w_4, w_1]$ get mapped to $[z_1, z_2]$, $[z_2, z_3]$, $[z_3, z_4]$, and $[z_4, z_1]$, respectively. It thus follows that the device characterization parameters a and b for the rectangular-gate device are related to the characterization parameters θ, R_1, and R_2 for the ring-gate device by

$$\left.\begin{aligned} a &= \ln (R_1/R_2) \\ \text{and} \\ b &= \Theta \end{aligned}\right\} \tag{19}$$

where θ is in radians and satisfies the equation

$$0 \leqslant \theta \leqslant 2\pi.$$

It also follows that if the source is connected to $[z_3, z_4]$, and the drain to $[z_1, z_2]$, then from (19)

$$\left(\frac{W}{L}\right)_{eq} = \frac{\Theta}{\ln (R_1/R_2)} \tag{20}$$

and from observation 2 of the previous section, that if the source and drain are connected to $[z_2, z_3]$ and $[z_1, z_4]$ that

$$\left(\frac{W}{L}\right)_{eq} = \frac{\ln (R_1/R_2)}{\Theta}. \tag{21}$$

The model for an annular-gate device follows immediately from (20) with $\theta = 2\pi$.

B. Eccentric Ring-Gate MOSFET

Consider now the eccentric ring-gate device in Fig. 3 along with the annular-gate device that has been previously analyzed. Kober [9] shows that the linear fractional transformation,

$$w = \frac{z - s}{z - t} \tag{22}$$

where s and t satisfy the equations

$$t = \frac{x_0^2 + r_1^2 - r_2^2 + \sqrt{(x_0^2 + r_1^2 - r_2^2)^2 - 4x_0^2 r_1^2}}{2x_0} \tag{23}$$

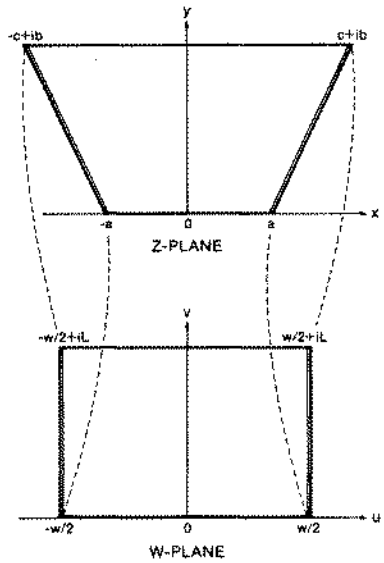

Fig. 4. Mapping of a trapezoid to a rectangle.

$$s = \frac{r_1^2}{t} \tag{24}$$

conformally maps the eccentric ring-gate device onto the concentric-circle device where the device characterization parameters are as indicated on Fig. 3. Routine manipulations now yield the equivalent W/L for the eccentric device

$$\left(\frac{W}{L}\right)_{eq} = \frac{2\pi}{\ln\left[\dfrac{r_1(t - x_0)}{r_2 t}\right]}. \tag{25}$$

Several equal-potential lines are also shown in Fig. 3.

C. Trapezoidal Devices

A trapezoidal-gate MOSFET is shown in Fig. 4 along with its rectangular image under a univalent transformation. For convenience, the source and drain are associated with the opposite parallel sides of the trapezoidal device and are mapped to the horizontal sides of the rectangle which have length W. Although the Riemann mapping theorem guarantees the existance of this transformation, unfortunately it does not give a closed form expression for the mapping. In this case, we have not been able to find a simple, explicit mapping in terms of elementary functions or rational fractions. The Schwartz-Christoffel transformation [7] can, however, be used in a two-step manner to obtain the required mapping.

Consider now the W_1-, W_2- and Z-plane shown in Fig. 5. The Schwartz-Christoffel transformation will be first used to map the upper-half of the Z-plane onto the rectangle in the W_1 plane by the mapping $W_1 = \phi_1(z)$. The Schwartz-Christoffel transformation will again be used to map the upper-half of the Z-plane onto the trapezoid in the W_2-plane by the mapping $W_2 = \phi_2(z)$. The images of the sides and vertices of the two mappings are as depicted in Fig. 5. The parameter k is not a free parameter but can be obtained once a, b, c, and α have been specified where α is the angle indicated in degrees. Likewise, k is a function of the parameters W and L. The parameter k will be used later to obtain the relationship between the parameters that characterize the trapezoids and those that characterize the rectangle.

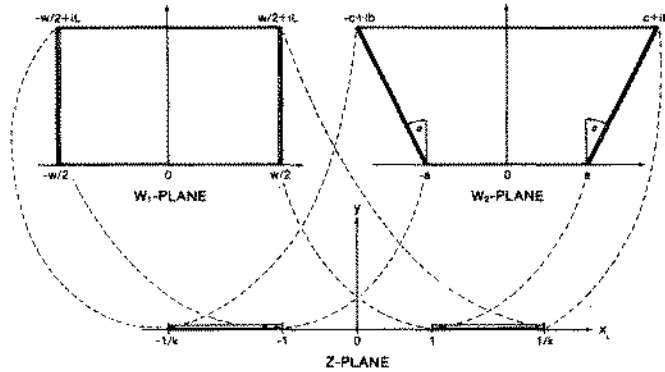

Fig. 5. Mapping of a rectangle to a trapezoid with the Schwartz-Christoffel transformation.

The mapping of the trapezoid to the rectangle is given by

$$w_1 = \phi_1(\phi_2^{-1}(w_2)). \tag{26}$$

If we assume that $\phi_1(0) = 0$ and define the normalized angle α_n by $\alpha_n = \alpha/360°$, one mapping $\phi_1(z)$ that maps the upper half-plane to the trapezoid, as depicted in Fig. 5 is given by

$$w_2 = \phi_2(z) = \int_0^z (1 - \xi^2)^{\alpha_n - 0.5}(1 - k^2\xi^2)^{-\alpha_n - 0.5}\, d\xi \tag{27}$$

where the integral is actually a line integral and the path of integration is any contour in the closed upper half plane. By letting $\alpha_n = 0$ in (27), a mapping to the rectangle as depicted on Fig. 5 is given by

$$w_1 = \phi_1(z) = \int_0^z (1 - \xi^2)^{-0.5}(1 - k^2\xi^2)^{-0.5}\, d\xi. \tag{28}$$

The relationship between a, b, α_n, W, and L remains to be determined. From Fig. 5 we observe that

$$\phi_2(1) = a \tag{29}$$

$$\phi_2(1/k) = c + jb. \tag{30}$$

It follows from (27), (29), and (30) after some routine manipulations that

$$\frac{2a}{b} = \frac{2}{\cos(\pi\alpha_n)} \frac{\displaystyle\int_0^1 (1 - x^2)^{\alpha_n - 0.5}(1 - k^2x^2)^{-\alpha_n - 0.5}\, dx}{\displaystyle\int_1^{1/k} (x^2 - 1)^{\alpha_n - 0.5}(1 - k^2x^2)^{-\alpha_n - 0.5}\, dx}. \tag{31}$$

By replacing α_n by 0 in (31), the equivalent W/L for the rectangular device, in terms of the parameter k, becomes

$$\frac{W}{L} = 2 \frac{\displaystyle\int_0^1 \frac{1}{\sqrt{(1 - x^2)(1 - k^2x^2)}}\, dx}{\displaystyle\int_1^{1/k} \frac{1}{\sqrt{(x^2 - 1)(1 - k^2x^2)}}\, dx}. \tag{32}$$

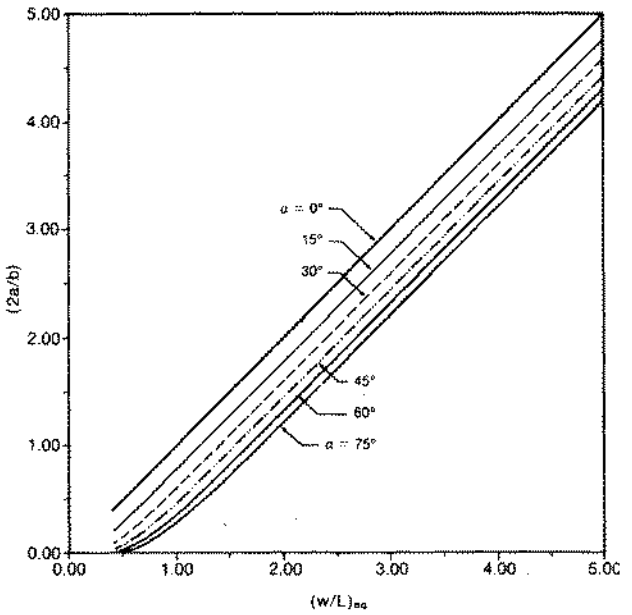

Fig. 6. Relationship between α, $2a/b$, and $(W/L)_{eq}$ for trapezoidal devices.

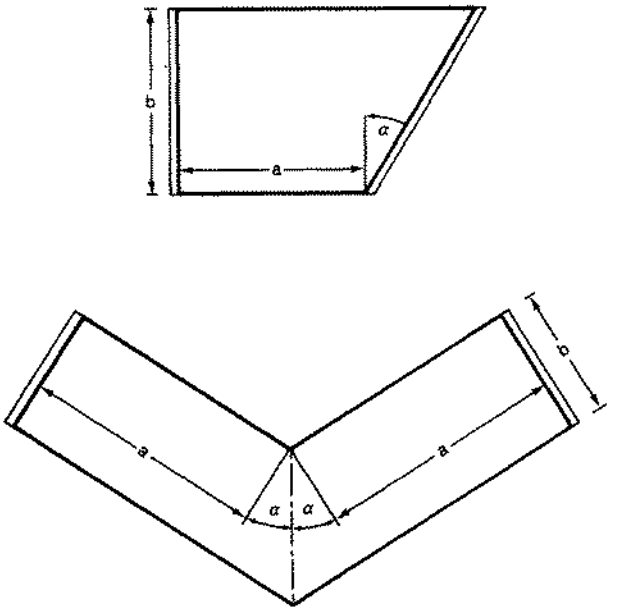

Fig. 7. Composition of basic devices. (a) "Halved" trapezoid. (b) "V"-shaped gate. Source and drain indicated by double lines.

(31) and (32) can now be solved simultaneously by eliminating k to obtain the desired relationship (since $\alpha = \alpha_n \cdot 360°$)

$$(W/L)_{eq} = f\left(\alpha, \frac{2a}{b}\right). \tag{33}$$

To the authors knowledge, no closed-form analytic expression for the elliptic integrals in (31) and (32) exists. The parameter k will now be eliminated numerically. Even numerically the elliptic integrals are ill-conditioned due the singularities at $x = 1$ and $x = 1/k$. Standard integration techniques such as using Simpson's rule are impractical. A Gauss-Jacobi algorithm [10] based upon 50 points proved sufficient for obtaining these integrals. The relationship indicated in (33) is shown on Fig. 6 for 15-degree increments in α. It can be seen that these curves are very linear provided $2a/b > 0.25$. An analytical approximation of the relationship indicated in (33)

$$(W/L)_{eq} = \frac{2a}{b} - 7 \times 10^{-5}\,\alpha^2 + 1.57 \times 10^{-2}\,\alpha - 2 \times 10^{-3} \tag{34}$$

where α is in degrees and which is accurate to within 1 percent provided $2a/b > 1.4$ was obtained from a second-order least-mean-square curve fit based upon the calculated data.

It should be noted that the results presented on Fig. 6 are not consistent with those of Hemmert [4]. Although Hemmert was using the same basic approach as employed in the previous section of this paper, his mapping T from the Z-plane to the W-plane did not satisfy the conformality requirement. Although the $\alpha = 90°$ curve was not included on Fig. 6 due to convergence problems in the numerical integration, the curve for $\alpha = 89.9°$, which is thought to be a very good approximation for the $\alpha = 90°$ case, was computed and satisfied (34) to within 2 percent. These results differ from the conjecture of Rao and Carr [3] that the equivalent W/L tends to infinity as α approaches 90°.

From observation 2 of the previous section, it follows that $(W/L)_{eq}$, for the trapezoidal device of Fig. 4 in the case that the drain and source are located on the nonparallel sides, is the reciprocal of that just derived.

D. Composition of Elementary Devices

The model of numerous additional devices can be obtained directly from that of the trapezoid and other devices analyzed by using symmetrical properties to disect and reconnect the known devices, provided that the disection is along curves where $\boldsymbol{n} \cdot \boldsymbol{J} = 0$ for the disection and the reconnection is along boundaries of equal length which have identical potentials at each point on the boundary. Analysis of two such devices obtained from the trapezoidal structure follow. (For models of several additional devices see Fig. 8.)

Denote $(W/L)_{eq}$ for the parallel drain-source trapezoidal device of Fig. 4 as $(W/L)_{REF}$ which is approximated in (34). By disecting this trapezoid along the vertical line $x = 0$, it follows that the current is halved, so that by observation 2 of the previous section, the equivalent W/L for the device shown in Fig. 7(a) is given by

$$(W/L)_{eq} = \frac{2}{(W/L)_{REF}}. \tag{35}$$

If two of these devices are now reconnected along the original drain connection to obtain the symmetric V-shaped device as indicated in Fig. 7(b), it follows that

$$(W/L)_{eq} = \frac{1}{(W/L)_{REF}}. \tag{36}$$

When $\alpha = 45°$, it follows from (34) and (36) that the device of Fig. 7(b) becomes the symmetric L-shaped transistor which has

$$(W/L)_{eq} = \frac{b}{2a + 0.559b}. \tag{37}$$

This can be compared to a "rule of the thumb" commonly used in industry to model this device of

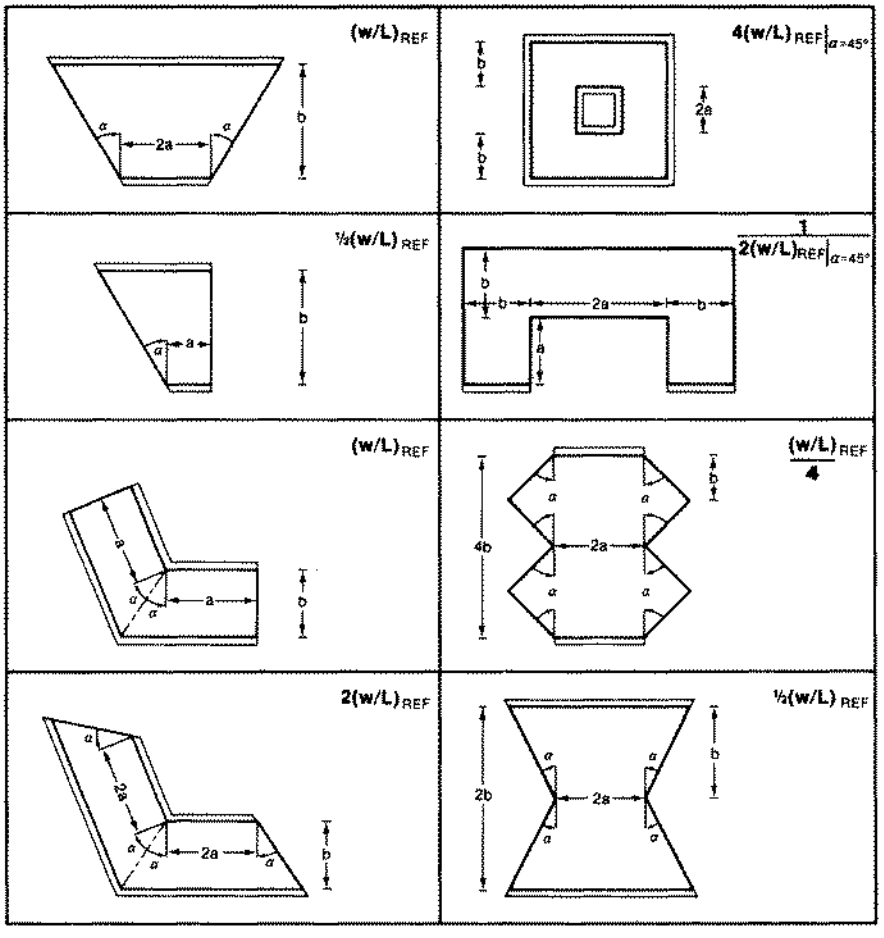

Fig. 8. $(W/L)_{eq}$ for composition transistors. Source and drain indicated by double lines.

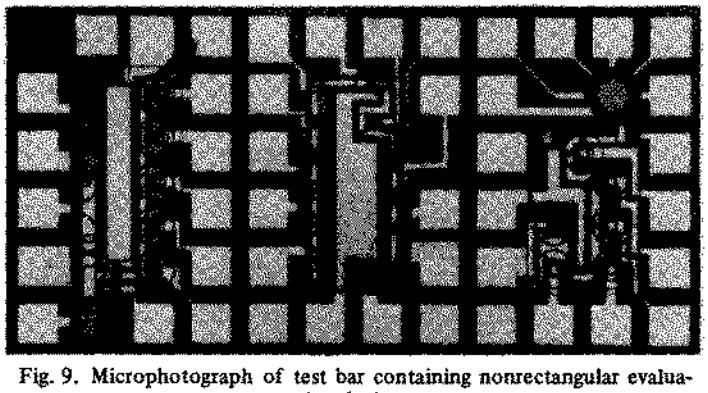

Fig. 9. Microphotograph of test bar containing nonrectangular evaluation devices.

$$(W/L)_{eq} = \frac{b}{2a + 0.5b}. \tag{38}$$

Results for these and additional devices are summarized in Fig. 8 where the source and drain contacts are indicated by a double line.

IV. Experimental Results

Several of the devices previously modeled were fabricated using a double polysilicon NMOS process with 0.05-mil design rule resolution. These included 13 trapezoidal-gate, 6 concentric-ring-gate, and 4 eccentric-ring-gate enhancement devices. One of the trapezoidal devices was rectangular and serves as a reference. A microphotograph of the test bar is shown in Fig. 9. The measured $(W/L)_{eq}$ is compared with the theoretical in Table I for all these devices. Characterization parameters listed are the same as those used in the text. Dimensions are in mils. Comparisons are all made with respect to the measured value of W/L of the rectangular device to minimize the effects of the process-dependent term uC_{ox}. The values of $(W/L)_{eq}$ were determined by a least-squares fit based upon measurements of I_D in the saturation region for values of V_{GS} = 1.5, 2, 3, 4, 5, 6, and 7 V, V_{BS} = 0, and V_{DS} = 7 V including compensation for the channel-length modulation parameter λ. This compensation was made under

TABLE I
EXPERIMENTAL PERFORMANCE EVALUATION OF NONRECTANGULAR-GATE MOSFET's

MOSFET	Design Parameters				$(W/L)_{exp}$	$(W/L)_{th}$	% Error
	Trapezoidal - Gate						
	2a	b	2c	α			
T1	3.20	2.00	3.20	0.0°	1.600	1.600	---
T2	2.80	2.00	3.20	5.7°	1.486	1.494	0.5
T3	2.40	2.00	3.20	11.3°	1.375	1.378	0.2
T4	2.00	2.00	3.20	16.7°	1.236	1.251	1.2
T5	1.60	2.00	3.20	21.8°	1.114	1.112	0.2
T6	1.20	2.00	3.20	26.6°	0.963	0.961	0.2
T7	0.80	2.00	3.20	31.0°	0.796	0.795	0.1
T8	0.40	2.00	3.20	35.0°	0.601	0.599	0.3
T9	1.20	1.60	2.80	26.6°	1.108	1.116	0.7
T10	1.20	1.20	2.40	26.6°	1.358	1.370	1.2
T11	1.20	0.80	2.00	26.6°	1.818	1.872	2.9
T12	1.20	0.40	1.60	26.6°	3.448	3.373	2.0
T13	0.80	1.00	1.60	21.8°	1.101	1.112	1.0
	Concentric - Ring Gate						
	R1	R2					
T14	2.00	0.60			5.248	5.219	.5
T15	2.00	0.80			6.934	6.857	1.1
T16	2.00	1.00			9.152	9.065	1.0
T17	2.00	1.20			12.244	12.300	0.5
T18	2.00	1.40			17.263	17.616	2.0
T19	2.00	1.80			27.371	28.158	2.8
	Eccentric - Ring Gate						
	x_0	r_1	r_2				
T20	0.20	2.00	0.80		6.844	6.948	1.5
T21	0.40	2.00	0.80		7.319	7.247	1.0
T22	0.60	2.00	0.80		7.929	7.853	1.0
T23	0.80	2.00	0.80		9.074	9.065	0.1

the assumption that the λ effects of rectangular-gate and nonrectangular gate MOSFET's are identical. This last assumption introduces a small error in the experimental results. For the process, the threshold voltage was approximately 0.5 V and uC_{ox} approximately $21.5 \cdot 10^{16}$ A · V^{-2}. As can be seen from Table I, the models derived are quite good. In addition to instrumentation, the errors can be attributed to the 0.05-mil digitization resolution and the λ parameter mentioned previously.

From the experimental evaluations it appears that the shape of the gate can be used to reduce λ effects. From a theoretical point of view, the shape of the gate affects the value of the parasitic capacitances and may be useful for reducing these effects in some applications.

V. Conclusions

The electrical characteristics of several nonrectangular-gate MOSFET's have been analytically determined. In this derivation it was shown that based upon the same physical model used to derive Sah's equation for the dc operation of rectangular-gate MOSFET's, any device with an arbitrarily shaped gate is electrically equivalent to a rectangular transistor. Experimental results based upon a large number of specially fabricated devices confirmed these conclusions.

The effects of the gate geometry on the channel-length modulation parameter λ and parasitic capacitances warrant further investigations. The effects of gate geometry on the electrical characteristics of short-channel devices may also be of interest.

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