

For a scaled 2-D filter (29) and (30) can be rewritten as

$$\sum_{i=1}^{n_1} W_{ii}^h = \text{tr}(W^h) \geq \frac{1}{n_1} \left(\sum_{i=1}^{n_1} 6_i^h \right)^2 \quad (31)$$

$$\sum_{i=1}^{n_2} W_{ii}^v = \text{tr}(W^v) \geq \frac{1}{n_2} \left(\sum_{i=1}^{n_2} 6_i^v \right)^2 \quad (32)$$

since the bound (24) for a scaled filter is given as

$$\|S_A\|_1 \leq (n_1 + n_2)(\text{tr}(W^h) + \text{tr}(W^v)). \quad (33)$$

The right-hand side of (33) is minimum iff each of the trace terms is minimum, which is true whenever equalities hold in (31) and (32). According to [11], these equalities hold for optimal realization for equal wordlength. Q.E.D.

It is easy to show that this minimum upper bound is

$$\|S_A\|_1 \leq (1+L) \left[\left(\sum_{i=1}^{n_1} 6_i^h \right)^2 + \frac{1}{L} \left(\sum_{i=1}^{n_2} 6_i^v \right)^2 \right] \quad (34)$$

with

$$L = \frac{n_2}{n_1}.$$

IV. CONCLUSION

An upper bound on coefficient sensitivity of 2-D optimal filters is established. This bound is useful in the design of digital filters since it can be computed directly from Grammian matrices. Further more, we have shown that the bound for an optimal realization having equal wordlength registers is minimum. Hence, it appears that optimal realization provides both low roundoff noise and low coefficient sensitivity.

REFERENCES

- [1] B. Liu, "Effects of finite wordlength on the accuracy of digital filters—A review," *IEEE Trans. Circuit Theory*, vol. CT-18, pp. 670–677, 1971.
- [2] M. D. Ni and J. K. Aggarwal, "Two dimensional digital filtering and its error analysis," *IEEE Trans. Computer*, vol. C-23, Sept. 1974.
- [3] S. Y. Hwang, "Round off noise in state space digital filtering: A general analysis," *IEEE Trans. Acoust., Speech, Signal Processing*, vol. ASSP-24, pp. 256–262, June 1976.
- [4] L. B. Jackson, "Round off noise bounds derived from coefficient sensitivities for digital filters" *IEEE Trans. Circuits Syst.*, vol. CAS-23, pp. 481–485 Aug. 1976.
- [5] L. B. Jackson, A. G. Lindgren, and Y. Kim, "Optimal synthesis of second-order state space structures for digital filters," *IEEE Trans. Circuits Syst.*, vol. CAS-26, pp. 149–153, Mar. 1979.
- [6] V. Tavsanoglu and L. Thiele, "Optimal design of state space digital filters by Simulations minimization of sensitivity and round off noise," *IEEE Trans. Circuits Syst.*, vol. CAS-31, pp. 884–888, Oct. 1984.
- [7] R. E. Crochiere and A. V. Oppenheim, "Analysis of linear digital network," *Proc. IEEE*, vol. 63, Apr. 1975.
- [8] S. Y. Kung, B. C. Levy, M. Morf, and T. Kailath, "New results in 2-D systems theory, Part II: 2-D state space models," *Proc. IEEE*, vol. 65, pp. 945–961, June 1977.
- [9] R. P. Roesser, "A discrete state-space model for linear image processing," *IEEE Trans. Automat. Contr.*, vol. 20, pp. 1–10, Feb. 1975.
- [10] B. C. Mertzios, "On the round off noise in 2-D state-space digital filtering," *IEEE Trans. Circuits Syst.*, vol. CAS-32, pp. 201–204, Feb. 1985.
- [11] A. Zilouchian and R. L. Carroll, "On the optimal synthesis of 2-D state-space digital filters," *IEEE Trans. Circuits Syst.*, Nov. 1985.
- [12] R. L. Carroll and A. Zilouchian, "On the round off noise of separable in denominator 2-D filters," *IEEE Trans. Circuits Syst.*, vol. CAS-33, p. 448, Apr. 1986.
- [13] A. Zilouchian and R. L. Carroll, "On the coefficient sensitivity bound of optimal realization," in preparation.
- [14] M. Vidyasagar, *Nonlinear System Analysis* Englewood Cliffs, NJ: Prentice-Hall, 1978.

Area/Bandwidth Tradeoffs for CMOS Current Mirrors

KIRK D. PETERSON AND RANDALL L. GEIGER

Abstract—Conventional CMOS current mirrors with large current ratios require very large active areas and have limited bandwidths. It is shown that replacing the inefficient large ratio current mirrors with a cascade of smaller current mirrors can give significant increases in bandwidth and reductions in active area. A simple design strategy is presented which can be used to obtain near optimal tradeoffs between active area and bandwidth.

INTRODUCTION

One of the basic building blocks for CMOS circuit design is the current mirror. Depending on the application a designer may choose the "simple" current mirror, Wilson mirror, cascade mirror, or others. Comparisons of some of the features (output resistance, bandwidth, and current gain) of the common mirrors are readily available [1]. For a given mirror and a specified nominal current gain, the designer is free to size the mirror (or cascade of mirrors) to maximize the overall bandwidth and minimize the total active area (sum of mirror $W \cdot L$ products). This is analogous to the sizing of a string of inverters for driving large capacitive loads (e.g., pad drivers) in digital circuit design.

ANALYSIS

Consider initially the simple current mirror of Fig. 1 and the cascade of simple current mirrors of Fig. 2. Whenever a large current gain ($k \gg 1$) or a large current reduction ($k \ll 1$) is attained with the current mirror of Fig. 1, a very wide device is required. Because of the associated large device capacitance, the bandwidth of such structures is limited. Alternatively, using several cascaded current mirrors as shown in Fig. 2 to attain the same nominal gain can result in a significant reduction in total active area and a significantly higher 3dB bandwidth for the mirror gain.

Fig. 3 shows the simulated 3-dB bandwidth and the total active area for a cascade of N equal gain mirrors with nominal overall current gains of 20 and 200 obtained from a SPICE2G.6 level 2 simulation using typical 5μ process parameters, including $K'_n = 11 \mu\text{A}/\text{V}^2$ and $K'_p = 3 \mu\text{A}/\text{V}^2$ where $K' = \mu C_{ox}/2$. Corresponding characteristics for reductions of 20 and 200 are depicted in Fig. 4. The input mirror is comprised of n-channel devices in all comparisons.

The bias current (I_{in} of Fig. 2) for current gain cascades was $1 \mu\text{A}$ and $200 \mu\text{A}$ for current reduction cascades. All devices are designed to operate in the saturation region and a minimum dimension of 10μ is used to provide good matching. When sizing the mirror's nominal current gain (A_i) for Figs. 3 and 4, channel length modulation (λ) effects were not included, so the gain for

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The authors are with the Engineering Research Center, Texas A&M University, College Station, TX 77843-3128.
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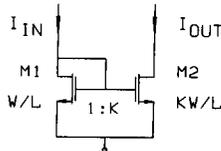


Fig. 1. "Simple" 1: *k* current mirror.

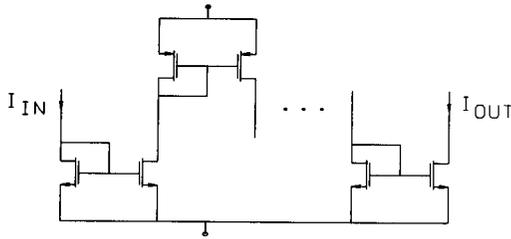


Fig. 2. Current mirror cascade.

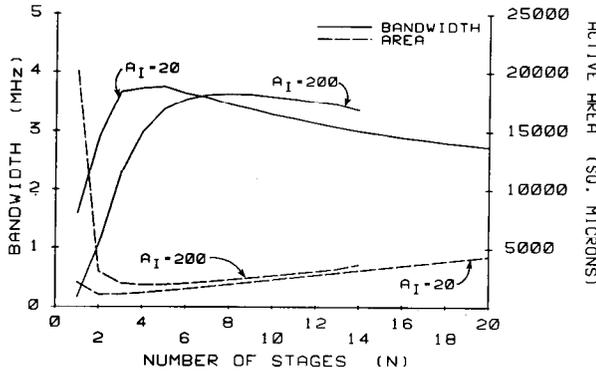


Fig. 3. Bandwidth and active area for cascaded current gain mirrors.

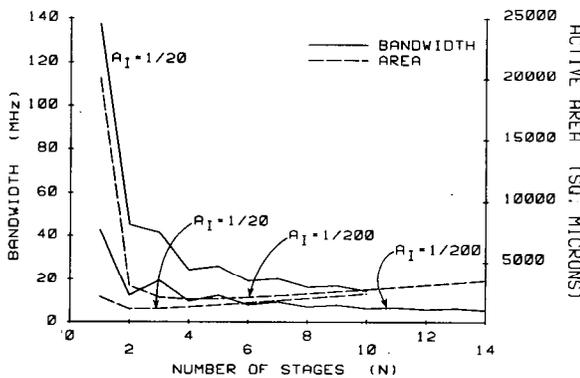


Fig. 4. Bandwidth and active area for cascaded current reduction mirrors.

each stage (k_i) was chosen as $N\sqrt{A_i}$ (for N stages). To keep the output mirrors saturated for several high N cascades of the $A_i = 200$ curve, the widths of the output mirror devices were doubled.

As expected, the design using a single mirror ($N=1$) has a very large active area and a very low bandwidth. As the number of stages increases, the total area tends to infinity and the bandwidth tends to zero. Between these extremes there is a fairly flat

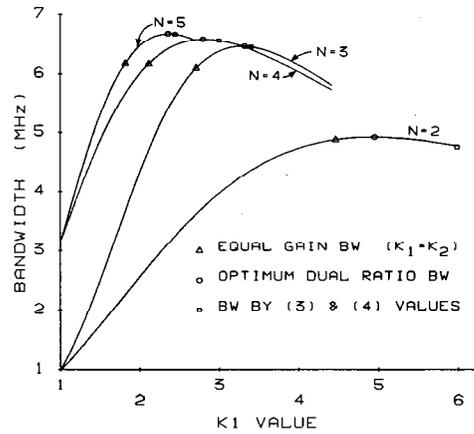


Fig. 5. Bandwidth of dual ratio current mirrors ($A_i = 20$).

minimum for the area curve and flat maximum for the bandwidth curve. Since the area curve does not include interconnect area, the actual design area rises with N more quickly than the plot indicates. Interconnect capacitance was neglected, indicating that the bandwidth of large N cascades is somewhat worse than shown.

The results will now be examined analytically. Assuming a simple 1-pole model for each mirror, the 3-dB bandwidth of the basic mirror of Fig. 1 can be approximated by:

$$f_{3\text{ dB}} \approx \frac{1}{2\pi} \frac{g_{m1}}{C_g} \approx \frac{3}{2\pi} \frac{\sqrt{K'I_{in}W/L}}{(1+k)C_{ox}WL} \quad (1)$$

where g_{m1} is the transconductance of M1, $C_g \approx 2/3 C_{ox}WL(1+k)$, and W, L, k are shown in Fig. 1. In the derivation of (1) it was assumed that $g_{m1} \gg g_{ds1}$ and that $2/3 C_{ox}WL \gg C_{dB} + C_{gs(\text{overlap})}$. Although the second assumption introduces a modest error, it is used to simplify the analysis. Since the 3-dB bandwidth is proportional to $\sqrt{I_{in}}$, the current reduction cascade will have a higher bandwidth than the current gain cascade for low N since there is no "dominant" pole due to a very low I_{in} stage (as with the input mirror for the current gain cascade).

The sawtooth effect in the current reduction bandwidth curves is due to the difference in mobility (and K') between the p-channel devices and the n-channel devices. The output mirror is alternately n channel/p channel for odd/even N . Since the output mirror has the lowest I_{in} it provides the "dominant" pole. Fluctuation of the "dominant" pole value with K' (for odd/even N) results in the sawtooth effect on the bandwidth curves.

BANDWIDTH OPTIMIZATION

For current gain cascades, one may attempt to maximize the overall mirror bandwidth and simultaneously achieve a fairly low total area because the area curve is quite flat near the bandwidth maximum. The gains of the n- and p-channel mirrors were all assumed equal in the comparisons shown in Figs. 3 and 4. The question about whether the assumption of equal mirror gains actually results in maximum bandwidth naturally arises. Due to mobility differences for n- and p-channel devices, it can be shown that further modest improvements in bandwidth can be attained by making the gain of the p-type mirrors different than that of the n-type structures.

The overall 3-dB bandwidth for $A_i = 20$ is shown in Fig. 5 as a

function of the n -channel mirror gain, k_1 , using the 1-pole model of (1). (The plotted bandwidths are slightly higher than shown in Fig. 3 because the simpler 1-pole model does not include all of the gate capacitances.) The curves show that the dual gain sizing scheme results in 3-dB bandwidths up to 8 percent above the best equal gain 3-dB bandwidths.

The task of determining the optimum value of k_1 is not trivial. A reasonably simple design method of determining k_1 that achieves close to the optimum bandwidths (for $N > 2$) is obtained by requiring equal factor separation of all mirror poles. Using the single-pole model for the mirror 3-dB frequency, it follows that the ratio of bandwidths of successive stages (for even n) are given by:

$$\frac{f_n}{f_{n-1}} = \sqrt{\frac{k_1}{r} \frac{1+k_1}{1+k_2}} \quad (2a)$$

$$\frac{f_{n+1}}{f_n} = \sqrt{rk_2 \frac{1+k_2}{1+k_1}} \quad (2b)$$

where k_1 is the n mirror gain, k_2 is the p mirror gain, and $r = K'_n/K'_p$. K_2 can be expressed in terms of the overall current gain A_i as

$$k_2 = \left(\frac{A_i}{k_1^{nn}} \right)^{1/np} \quad (3)$$

where nn is the number of n mirrors and np is the number of p mirrors. Upon equating the ratios of (2a) and (2b), it follows that for given nn and np , k_1 and k_2 are related by the expression:

$$\sqrt{k_1}(1+k_1)^2 = r\sqrt{k_2}(1+k_2)^2 \quad (4)$$

Equations (3) and (4) can be solved simultaneously to obtain k_1 and k_2 . The results of using the equal pole spacing are shown in Fig. 5. The bandwidth for a single stage mirror would be 1.89 MHz, so the significant improvement by using a cascade of mirrors is obvious. It is apparent that the approximation is quite good.

A practical design strategy would involve determining n (where $n = nn - np$) and hence nn and np from Fig. 2 or Fig. 3 to optimize bandwidth assuming equal mirror gains. Modest improvements in bandwidth can then be obtained by solving (3) and (4) for k_1 and k_2 .

CONCLUSION

It has been shown that significant bandwidth improvement and active area reduction can be simultaneously achieved by using cascades of current mirrors rather than single mirrors. A practical design strategy for obtaining near-optimal bandwidth was presented.

REFERENCES

[1] J. C. Davidson and K. W. Current, "MOS current sources—a comparison and evaluation," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 3, pp. 1215–1218, May 1984.

Comments on "Highly Selective Three-Dimensional Recursive Beam Filters Using Intersection Resonant Planes"¹

SOO-CHANG PEI AND SY-BEEN JAW

In the above paper,¹ Bruton and Bartley have proposed a novel method to realize highly selective 3-D recursive digital filters, these special filters have the property that their passbands surround a straight line along a particular direction of propagation. By cascading two 3-D recursive plane filters,¹ we can obtain the required 3-D beam filters in any direction using these two intersecting resonant planes. Bruton and Bartley have designed these two 3-D recursive plane filters by subjecting two 1-D analog low-pass filters to triple bilinear transformation:

$$S_i = \frac{Z_i - 1}{Z_i + 1}, \quad i = 1, 2, 3.$$

The orientation of the passband of 3-D recursive beam filter will be "bent" due to this triple bilinear transformation, this bending effect is rather difficult to illustrate and explain in 3-D case, we will show this below by "a 2-D example", assume a fifth-order analog Butterworth filter:

$$H_1(s) = \frac{1}{(1+s)(1+0.6180340s+s^2)(1+1.6180340s+s^2)}$$

then define the corresponding 2-D analog filter as follows:

$$H'_i(s_1, s_2) = H_1(s) \quad s = 1 \cdot s_1 + 2 \cdot s_2 = \alpha_1 s_1 + \alpha_2 s_2$$

where α_1, α_2 are related to the direction cosines of our selective propagation.

Apply double bilinear transform to get the 2-D recursive digital filter:

$$H'_i(Z_1, Z_2) = H'_i(s_1, s_2)|_{s_i = (Z_i - 1)/(Z_i + 1)}, \quad i = 1, 2.$$

The frequency response of this 2-D recursive digital filter is shown in Fig. 1, there is severe bending in the high frequency range.

Set

$$S|_{s=j\omega} = \alpha_1 \frac{Z_1 - 1}{Z_1 + 1} \Big|_{Z_1 = e^{j\omega_1}} + \alpha_2 \frac{Z_2 - 1}{Z_2 + 1} \Big|_{Z_2 = e^{j\omega_2}} = 0$$

we get

$$\omega_2 = 2 \tan^{-1} \left(\frac{-\alpha_2}{\alpha_1} \tan \frac{\omega_1}{2} \right) = 2 \tan^{-1} \left(c \tan \frac{\omega_1}{2} \right).$$

The curve for several values of c is plotted in Fig. 2, from this curve we can see bilinear transform causes severe distortion in the high frequency range except for the case $c=1$; the designed example chosen by Bruton and Bartley (see (11) in 1) is just happened to be $c=1$ without any distortion.

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