

In many applications the current sources are extended using multiple-output current mirrors (Fig. 9). For these circuits we recommend the same types of solutions to avoid latch-up. The required modifications of the conditions can easily be derived and will not be dealt with here.

#### IV. ALTERNATIVE LOW-VOLTAGE PTAT CURRENT SOURCES

Up to now discussion has been limited to current sources of the type in Fig. 1(a) and (b). This type of circuit shows a good PSRR for loads referred to the negative supply voltage. However, for loads referred to the positive supply voltage, for instance  $R_g$  and  $R_o$  in Fig. 9, no compensation for the Early effect of the output transistor occurs, which results in a bad PSRR. For these types of loads the circuit of Fig. 1(c) is preferable. In this case as well, latch-up can easily occur. The solutions for this problem are similar to the ones discussed before and are shown in Fig. 10. In this case it must hold that  $V_{CE1} < V_{CE2}$ , which results in conditions almost similar to those derived in the previous section.

#### V. CONCLUSIONS

Latch-up is a general design problem for bipolar circuits and especially for those circuits operated at low supply voltages. For low-voltage current sources we have shown that at subnominal levels of the supply voltage a sharp increase in the supply current can occur. This current peaking effect is caused by saturation of some of the transistors and is responsible for latch-up and other undesirable effects in electronic systems. Fortunately, the occurrence of current peaking and latch-up can easily be counteracted by enforcing the saturation of other well-chosen transistors.

Various methods to implement this idea and to realize latch-up-free current sources have been presented along with the conditions needed to be fulfilled by the circuit parameters.

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### A $\pm 5$ -V CMOS Analog Multiplier

SHI-CAI QIN AND RANDY L. GEIGER, SENIOR MEMBER, IEEE

**Abstract**—A four-quadrant CMOS analog multiplier is presented. The device is nominally biased with  $\pm 5$ -V supplies, has identical full-scale single-ended  $x$  and  $y$  inputs of  $\pm 4$  V, and exhibits less than 0.5 percent

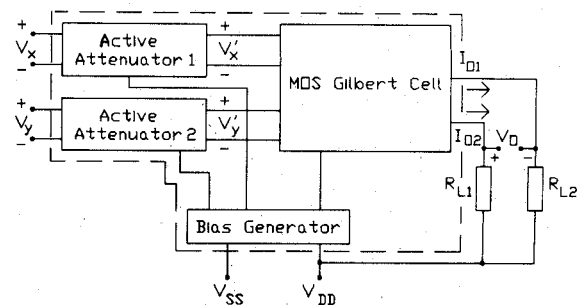


Fig. 1. Block diagram of CMOS multiplier cell.

nonlinear error at 75 percent of full-scale swing. Operation with supplies as low as  $\pm 2.5$  V is also possible. A comparison of theoretical and experimental results obtained from fabrication of the multiplier in a 3- $\mu$ m p-well CMOS process is made.

#### I. INTRODUCTION

Bipolar variable-transconductance analog multipliers based on Gilbert's cell [1] have been successfully used for many years. Unfortunately, it is not possible to realize an MOS analog multiplier simply by substituting the BJT's in a bipolar multiplier with MOS transistors as is often done in developing the MOS functional equivalent of established bipolar circuits. This is due to the fact that the output current of the MOS source-coupled differential pair depends nonlinearly on the bias current  $I_{ss}$  and input signal  $V_i$ . Consequently, the linear input range of the corresponding MOS multiplier is narrow and difficult to compensate. The MOS analog multiplier is, however, a very useful subcircuit in integrated VLSI systems.

In recent years, some MOS analog multipliers have been reported [2]–[4]. The specifications are not, however, as attractive as the bipolar counterparts. The multiplier of Soo and Meyer [3] had a  $\pm 1$ - $V_{p-p}$  full-scale output swing and nonsymmetric inputs of  $-0.4$  V  $< V_x < +0.4$  V and  $-0.7$  V  $< V_y < +0.7$  V and required  $\pm 10$ -V supplies. The output error was less than 0.3 percent of full-scale output at 75 percent of full-scale swing. The gain factor of the multiplier cell itself, differential output current divided by  $V_x V_y$ , was  $3.57$  mA/V<sup>2</sup>. The output noise was measured to be 77 dB below the full-scale output signal. The bandwidth was reported at 1.5 MHz. Babanezhad and Temes [4] describe an n-well CMOS multiplier that offers a much improved input-to-supply voltage ratio as well as a much improved output-to-supply voltage ratio. However, the improvement in output voltage swing was obtained by using a conventional operational amplifier and discrete resistors to amplify a signal that was obtained from a basic multiplier cell that had a gain factor (differential output current divided by  $V_x V_y$ ) of  $1.22$   $\mu$ A/V<sup>2</sup>, which is much less than that reported in [3]. The nonlinearity was reported in the range of 1.3- to 1.6-percent of full-scale output. The 3-dB bandwidth was measured at 75 kHz.

#### II. PRINCIPLE OF OPERATION OF PROPOSED MULTIPLIER

A block diagram of the proposed CMOS multiplier is shown inside the dashed box in Fig. 1. The multiplier is based upon an MOS version of the Gilbert cell that is similar to that used by Babanezhad and Temes [4]. Differential active attenuators are used at the input to the MOS Gilbert cell to increase signal swing capabilities. The output of the multiplier is a differential output current. A differential output voltage can be obtained between

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The authors are with the Department of Electrical Engineering, Texas A&M University, College Station, TX 77843-3128.  
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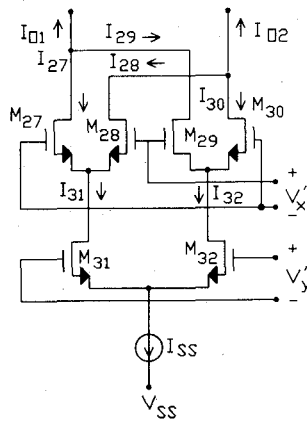


Fig. 2. MOS version of Gilbert cell.

two resistors referenced to  $V_{DD}$  as shown in the figure. A description of each of the basic blocks follows.

### A. MOS Gilbert Cell

An MOS version of the Gilbert multiplier cell [1] is shown in Fig. 2. Assume that all transistors in Fig. 2 are biased in the saturation region and obey the ideal square-law equation and that devices are sized and matched so that the transconductance parameters satisfy the equations  $K_{27} = K_{28} = K_{29} = K_{30} = K_a$  and  $K_{31} = K_{32} = K_b$ . Defining the output currents  $I_{01} = -(I_{27} + I_{29})$  and  $I_{02} = -(I_{28} + I_{30})$ , it can be readily shown that the differential output current  $I_{0d} = I_{02} - I_{01}$  is given by

$$I_{0d} = \sqrt{2K_a} V'_x \left[ \sqrt{I_{31}} \sqrt{1 - \frac{K_a V_x'^2}{2I_{31}}} - \sqrt{I_{32}} \sqrt{1 - \frac{K_a V_x'^2}{2I_{32}}} \right]. \quad (1)$$

If

$$\frac{K_a V_x'^2}{2I_{31}} \ll 1$$

and

$$\frac{K_a V_x'^2}{2I_{32}} \ll 1 \quad (2)$$

it follows that  $I_{0d}$  depends linearly on  $V'_x$  and is given by the expression

$$I_{0d} \approx \sqrt{2K_a} (\sqrt{I_{31}} - \sqrt{I_{32}}) V'_x. \quad (3)$$

It can also be readily shown that  $I_{31}$  and  $I_{32}$  are dependent upon the voltage  $V'_y$  as indicated by the expression

$$V'_y = \frac{1}{\sqrt{K_b}} (\sqrt{I_{31}} - \sqrt{I_{32}}). \quad (4)$$

Substituting (4) into (3), it follows that

$$I_{0d} = \sqrt{2K_a K_b} V'_x V'_y. \quad (5)$$

This is the characteristic of an ideal analog multiplier.

From the above analysis, it appears that the dependence of  $I_{0d}$  on  $V'_y$  is inherently totally linear. Unfortunately, since both  $I_{31}$  and  $I_{32}$  are  $I_{SS}$  and  $V'_y$  dependent, both  $V'_x$  and  $V'_y$  must be kept small to maintain good linearity. One strategy for minimizing these effects is to add attenuators to both the  $V'_x$  and  $V'_y$  inputs.

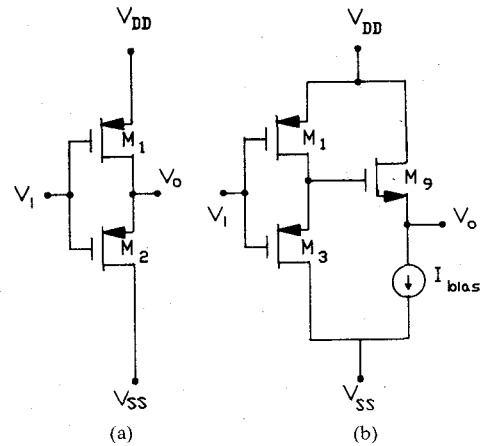


Fig. 3. Active attenuator: (a) attenuator of [5] and (b) attenuator with level shifter.

### B. Active Attenuator

A basic active attenuator [5] is shown in Fig. 3(a). Transistor  $M_1$  is assumed to be operating in the ohmic region and  $M_2$  is assumed to be operating in the saturation region. If bulk effects are neglected, the output voltage of the active attenuator is given by the expression

$$V_o = \left[ 1 - \sqrt{\frac{W_1 L_3}{W_1 L_3 + W_3 L_1}} \right] (V_i - V_{DD} - V_T) + V_{DD}. \quad (6)$$

Thus, the gain of the attenuator is given by

$$m = 1 - \sqrt{\frac{W_1 L_3}{W_1 L_3 + W_3 L_1}}. \quad (7)$$

For biasing purposes, a level shift is needed when coupling the attenuator into the Gilbert cell. A simple source follower can be used for this purpose as indicated in Fig. 3(b).

### C. Multiplier Cell

If  $m_1$  and  $m_2$  denote the gains of active attenuator 1 and active attenuator 2 of Fig. 1, respectively, it follows from (5) that the overall transfer characteristics of the CMOS multiplier can be approximated by

$$I_{0d} = I_{01} - I_{02} \approx [\sqrt{2K_a K_b}] V_x V_y m_1 m_2. \quad (8)$$

If a pair of resistors,  $R_{L1} = R_{L2} = R_L$ , are used to convert the differential output current to a differential output voltage as shown in Fig. 1, the output voltage is given by the expression

$$V_o = R_L I_{0d} \approx [\sqrt{2K_a K_b} R_L] V_x V_y m_1 m_2. \quad (9)$$

The overall multiplier cell is shown in Fig. 4. Device sizes used in a realization of this circuit are shown in Table I. The active attenuators were sized to give a 1:8.7 attenuation. This ratio offered a reasonable trade-off between signal swing, nonlinearity, error, and power consumption.

## III. EXPERIMENTAL RESULTS

The circuit of Fig. 4 was fabricated in a standard 3- $\mu$ m p-well CMOS process. Fig. 5 shows the microphotograph of the chip.

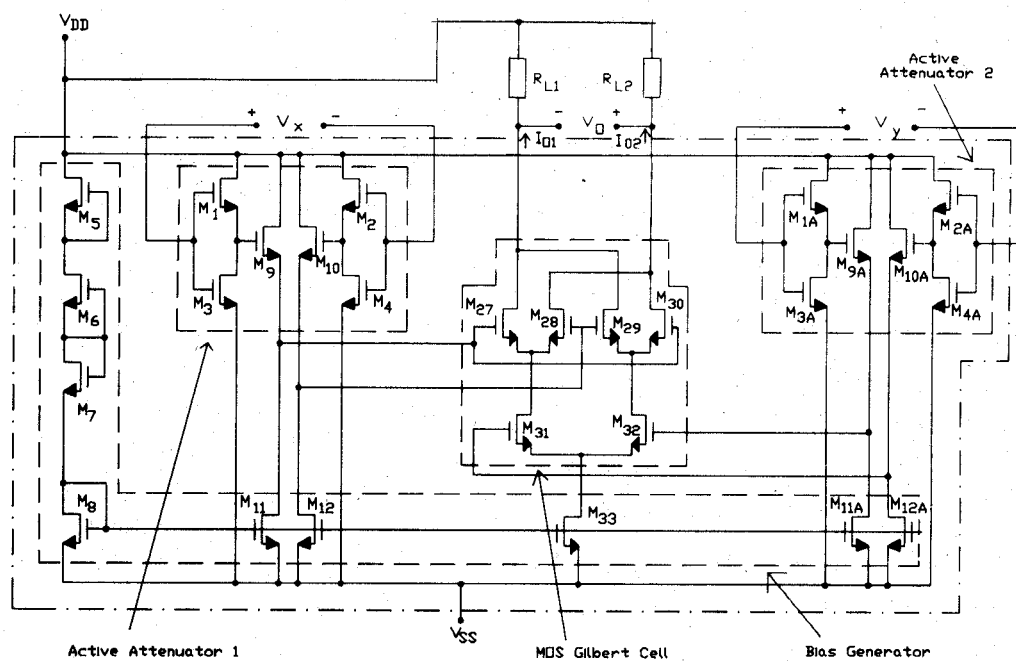


Fig. 4. CMOS multiplier.

TABLE I  
DEVICE SIZES FOR MULTIPLIER CELL  
Component size  $W/L$  ( $\mu\text{m}$ )

$M_1$	20/10	$M_{10}$	100/8	$M_{11A}$	16/8
$M_2$	20/10	$M_{11}$	16/8	$M_{12A}$	16/8
$M_3$	10/18	$M_{12}$	16/8	$M_{27}$	100/8
$M_4$	10/18	$M_{1A}$	20/10	$M_{28}$	100/8
$M_5$	8/36	$M_{2A}$	20/10	$M_{29}$	100/8
$M_6$	8/36	$M_{3A}$	10/18	$M_{30}$	100/8
$M_7$	8/36	$M_{4A}$	10/18	$M_{31}$	100/8
$M_8$	8/8	$M_{9A}$	8/120	$M_{32}$	100/8
$M_9$	100/8	$M_{10A}$	8/120	$M_{33}$	240/8

The chip area, including bonding pads, is  $932 \times 940 \mu\text{m}^2$ . The active area is  $13200 \mu\text{m}^2$ .

The dc transfer curves of the differential output current versus input voltage  $V_x$  of the chip for different  $V_y$  are shown in Fig. 6(a). In these plots and all experimental results that follow, one terminal to each input was grounded and the input was applied to the other input. This results in the effective presence of a common mode input that tends to degrade linearity specifications. This type of excitation was selected rather than a symmetric input with no common mode component since it represents typical excitations that will be encountered when applying these devices. The multiplier was terminated with matched 1K load resistors and biased with  $\pm 5$ -V supplies for these measurements. Correspondingly, plots of  $I_{od}$  versus  $V_y$  for different  $V_x$  are shown in Fig. 6(b). Based upon the linearity measure of [3], the nonlinear error for this circuit was measured and found to be less than 0.5 percent at 75 percent of full-scale swing.

All experimental results presented up to this point are based upon the differential output current. It is often the case that a differential of single-ended output voltage is required. As indicated by (9), a differential voltage output can be obtained directly from the proposed multiplier by adding the two external resistors as indicated in Fig. 1. The nonlinear errors, in percent relative to full scale, introduced by these load resistors, remain quite small for the circuit of Fig. 4 over a wide range of resistor values as indicated by the output error plot in Fig. 7.

The output noise characteristics were measured with  $V_y = 0$  V and  $V_x = 3$  V. The rms noise in the band 1 Hz to 1 MHz was

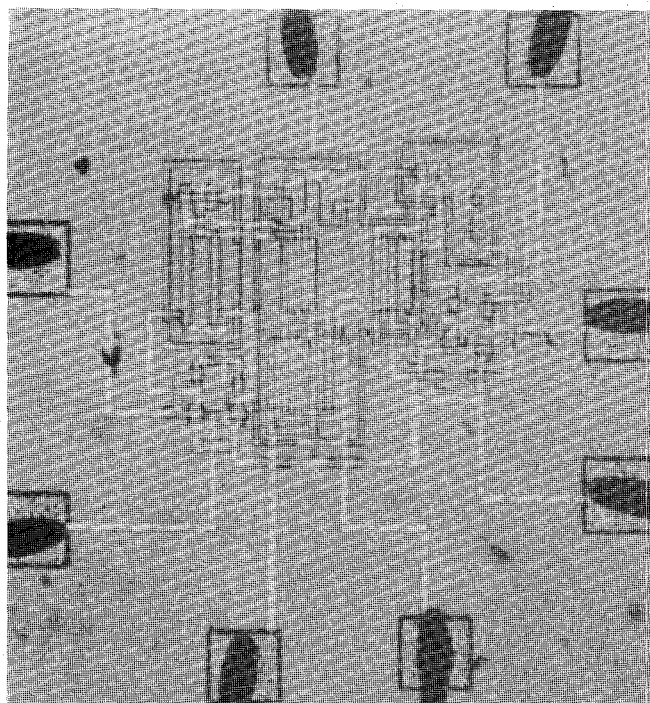


Fig. 5. Die photograph of CMOS multiplier.

measured single ended across a 100-k $\Omega$  load resistor to be 390  $\mu\text{V}$ , which corresponds to a single-ended output noise current of 3.9 nA. The dynamic range is 74.7 dB. The  $-3$ -dB bandwidths for the X and Y inputs were measured in excess of 500 kHz.

#### IV. CONCLUSION

A CMOS analog multiplier comprised of 27 MOS transistors, which was fabricated in a 3- $\mu\text{m}$  CMOS process, has been presented. The circuit can operate with power supply voltages ranging from  $\pm 5$  to  $\pm 2.5$  V with small distortion. Large single-ended input voltage swings of  $\pm 4$  V with  $\pm 5$ -V supplies are practical.

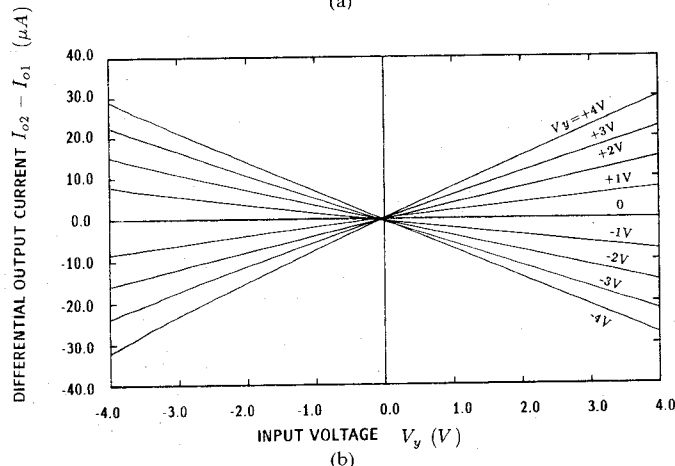
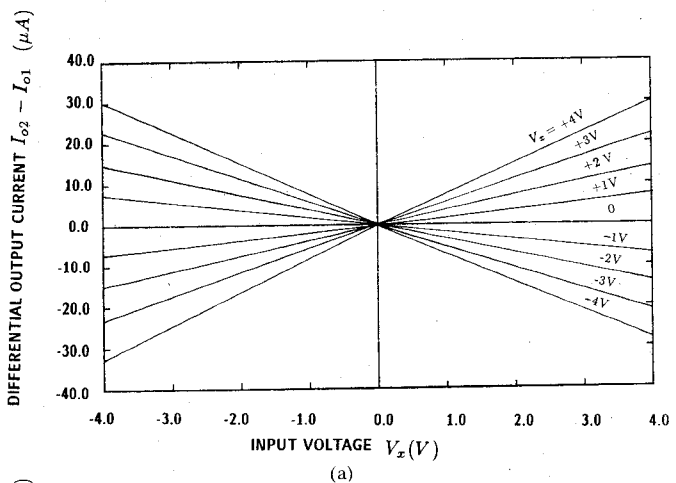


Fig. 6. Transfer characteristics of CMOS multiplier with  $\pm 5$ -V supplies: (a) for different  $V_x$ ; and (b) for different  $V_y$ .

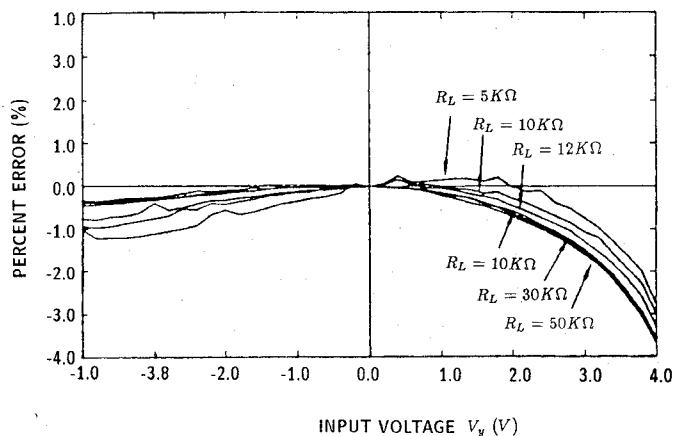


Fig. 7. Nonlinear output voltage errors for different  $R_L$  with  $V_x = 3$  V.

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