A ROBUST DIGITALLY PROGRAMMABLE AND RECONFIGURABLE MONOLITHIC FILTER STRUCTURE

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Abstract

A digitally reconfigurable and programmable filter structure is introduced. An implementation fabricated in a $3\mu m$ CMOS process capable of realizing any even–order transfer function of up to 6^{th}–order over the 3–decade frequency range from 1kHz to 1MHz with a resonant frequency resolution of less than $\pm\frac{1}{4}\%$ over the entire range is discussed.

Introduction

Many signal processing systems require a variety of widely different continuous–time filter functions. Both the wide variety of filter requirements and the problems associated with the unavailability of good practical resistors and large capacitors on silicon have slowed the development of viable high frequency monolithic continuous–time filter strategies [1–4]. MOS structures which maintain a good dynamic range over a wide adjustment range have proven even more problematic and fully reconfigurable continuous–time structures are essentially nonexistent.

In this paper, a digitally programmable monolithic filter structure is presented which is capable of realizing user–selectable high–order transfer functions. The structure is completely reconfigurable and programmable.

A specific implementation of this filter structure has been realized in a $3\mu m$ CMOS process. This filter block has digitally independent control of up to 3 pole pairs and up to 3 zero pairs and is thus capable of realizing any of the standard even-order filter functions of up to 6^{th}–order. The pole and zero adjustment range extends over three decades from 1kHz to 1MHz with an effective resolution in either pole or zero resonant frequency of $\pm\frac{1}{4}\%$ throughout this range and pole or zero Q resolution betweeen $\pm 0.05\%$ to $\pm 5\%$ and with a typical resolution of $\pm\frac{1}{2}\%$.

Filter Architecture

The basic filter architecture is shown in Fig. 1. In this structure, input and output signals from any biquad can be routed to either the analog input/output bus or the output from one biquad can be connected to the input of another biquad. The local digital controller is used to program and reconfigure each biquadratic block as well as control the analog bus connections. The structure which was fabricated and experimentally evaluated contained 3 biquadratic blocks, each with seven independent digitally controllable parameters. The structure of each of the biquadratic blocks is shown in Fig. 2. A transconductance–amplifier approach was used to achieve good linearity, good high–frequency performance, and a multiple–decade parameter adjustment range.

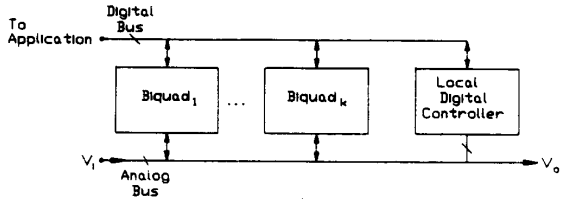

Fig. 1 Digitally Programmable Filter Architecture

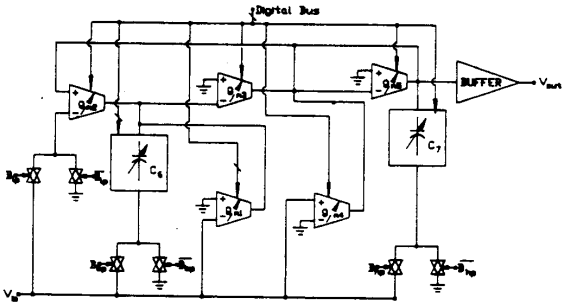

Fig. 2 Biquadratic Filter Section

Each of the five transconductance gains could select from 704 different states, and each of the two capacitor arrays could select from 20 different states. The transfer function of this block is given by

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$$\frac{V_{out}}{V_{in}} = \frac{(B_{hp})s^2 + \left(\frac{g_{m4} - g_{m3}B_{bp}}{C_7}\right)s + \left(\frac{g_{m1}g_{m3} + g_{m2}g_{m3}B_{lp}}{C_6C_7}\right)}{s^2 + \left(\frac{g_{m5}}{C_7}\right)s + \frac{g_{m2}g_{m3}}{C_6C_7}} \quad (1)$$

where the B variables can assume the value of either 0 or 1 depending upon the switch settings. It follows from Eq.(1) that the resonant frequency and bandwidth of the pole pair and zero pair are given respectively by

$$\omega_p = \sqrt{\frac{g_{m2}g_{m3}}{C_6C_7}} \quad (2)$$

$$BW_p = \frac{g_{m5}}{C_7} \quad (3)$$

$$\omega_z = \sqrt{\frac{g_{m1}g_{m3} + g_{m2}g_{m3}B_{lp}}{C_6C_7}} \quad (4)$$

$$BW_z = \frac{g_{m4} - g_{m3}B_{bp}}{C_7} \quad (5)$$

The f_o and bandwidth adjustment domain for the poles and zeros of the filter is shown in Fig. 3.

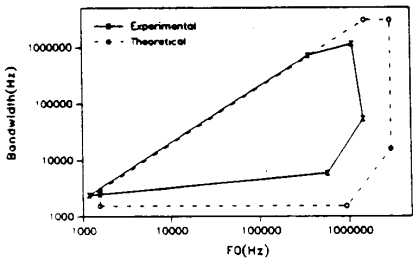

Fig. 3 f_0 and Bandwidth Adjustment Domain

OTA Architecture

The OTA architecture uses a differential transconductance input stage followed by the three-mirror gain/differential to single ended converter shown in Fig. 4. The transconductance amplifier was designed to provide for over two decades of g_m adjustment. To achieve good signal swing and good linearity, the linearized differential input pair of Nedungadi [5] was used for the input stage. To minimize the signal swing reduction inherent with bias current adjustment of MOS differential pairs, coarse g_m adjustment was achieved by digitally switching the current mirror gain for mirrors 1 and 3 of Fig. 4 rather than by adjustment of the bias current of the differential pair. Fine g_m adjustment was achieved through adjustment of the bias current of the differential input stage. The signal swing reduction associated with a single bias current adjustment would have proven particularly problematic here because of the requirement for a large g_m adjustment range.

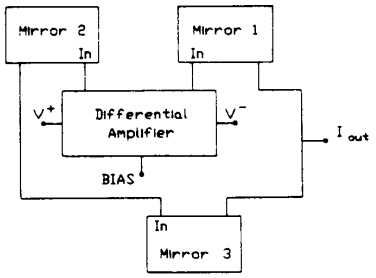

Fig. 4 Basic OTA Architecture

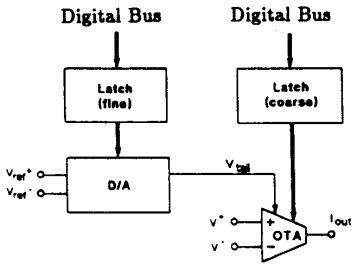

Fig. 5 Programmable OTA Structure

The programmable OTA structure is depicted in Fig. 5. Six bits were allocated to both the coarse and fine adjustments. In order to achieve a given uniform resolution of filter resonant frequency and Q which is independent of frequency over the entire adjustment range of the filter, successive g_m values must be uniformly spaced on a logarithmic axis. Whereas uniform spacing of a parameter on a linear axis is generally easily achievable, uniform spacing on a logarithmic axis appears more involved. The uniform spacing of g_m values throughout the fine adjustment range was achieved by using a logarithmic DAC to control the bias current. Uniform spacing over the coarse adjustment range can be achieved by trading off coarse control bits for adjustment range. In the specific implementation presented here, 11 uniformly spaced increments of 61.8% were achieved with 6 coarse adjustment bits. Combining coarse and fine adjustment resulted in 704 g_m values uniformly spaced on a logarithmic axis over approximately 2.36 decades with an effective g_m resolution of $\pm\frac{1}{2}\%$.

Capacitor Architecture

The programmable capacitor array is shown in Fig. 6 where switches $S_1 - S_n$ are used to add capacitors in shunt with C_0. As with the OTA, the capacitor values were chosen for uniform resolution on a logarithmic axis.

In the specific implementation, a resolution of 13% over a 10 to 1 adjustment range was achieved with 20 uniformly spaced capacitance values from the 6 control bits. The capacitance in Fig. 6 can be digitally adjusted from 2.4 pf to 24.4 pf.

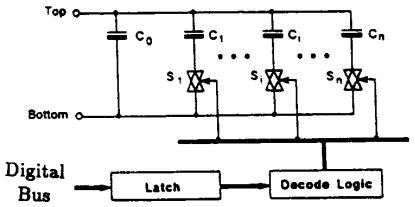

Fig. 6 Programmable Capacitor Arrays

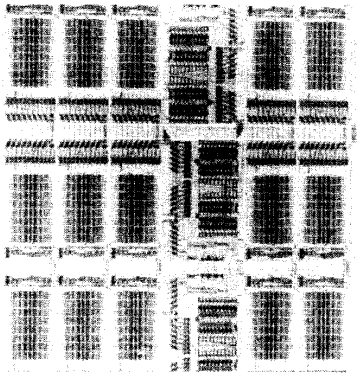

Fig. 7 Die Photograph of the Programmable Filter

Experimental Results

The programmable filter structure of Fig. 2 which contained 3 biquadratic blocks was fabricated in a $3\mu m$ CMOS process. A die photograph is shown in Fig. 7. The total die area was $7900\mu m \times 9200\mu m$ although significant reductions in die area are readily attainable.

With the modest tradeoffs which were made between number of control bits and resolution on logarithmic axis, each biquadratic block can implement slightly over 4×10^{17} different filter structures. Because of the large number of filter structures which can be obtained, experimental results will be presented for only a small representative cross section. In Fig. 3, the experimental results of the f_0 and bandwidth adjustment range is presented. Contained in this range are filters with a pole-pair Q in excess of 100. Both adjustment range and resolution are in close agreement with theoretical predictions with a modest loss in resolution for the high Q settings at medium to high frequencies due to parasitics in the OTA, the capacitor array and the layout.

The reconfigurability is depicted by the experimental results shown in Fig. 8 and Fig. 9. In the responses shown in Fig. 8, the circuit has been programmed to realize second–order lowpass, bandpass, highpass and notch functions. A 6^{th}–order Elliptic bandpass function realization is shown in Fig. 9. The programmability is depicted in Fig.

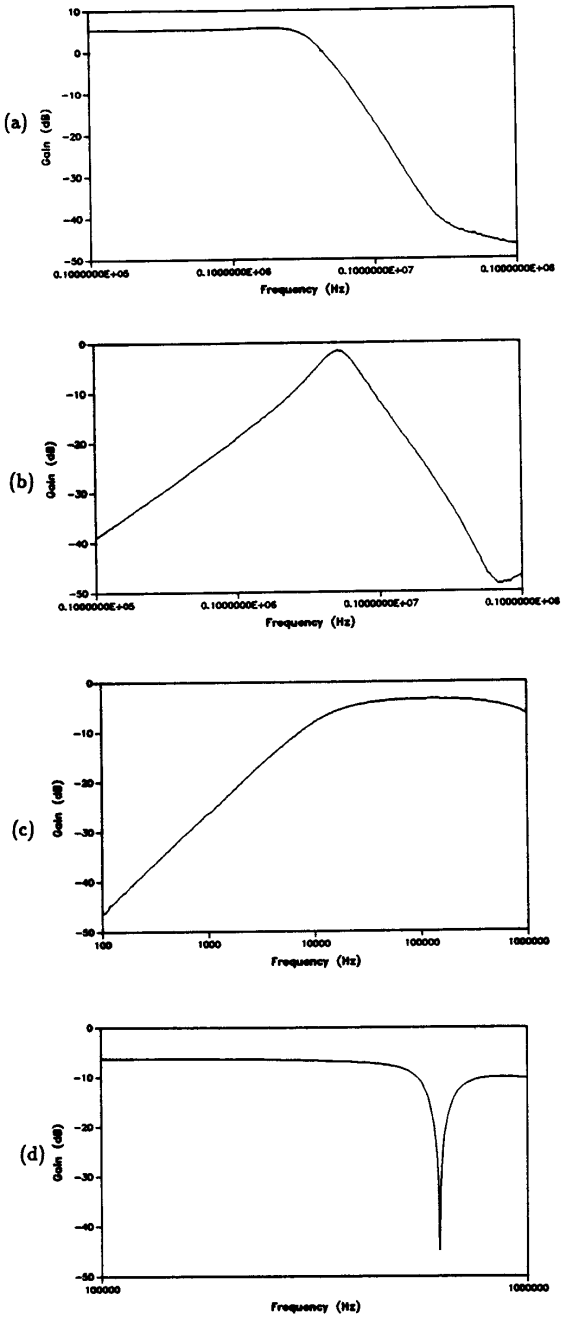

Fig. 8 Second–Order Filter Functions; a) Lowpass, b) Bandpass, c) Highpass, d) Notch

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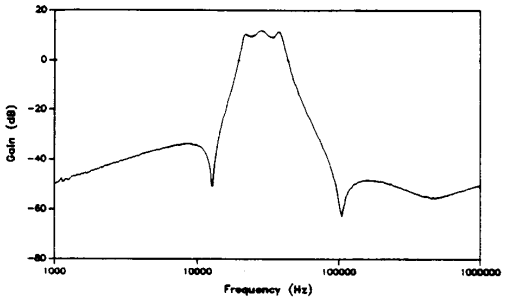

Fig. 9 6^{th}–Order Elliptic Bandpass Filter Function

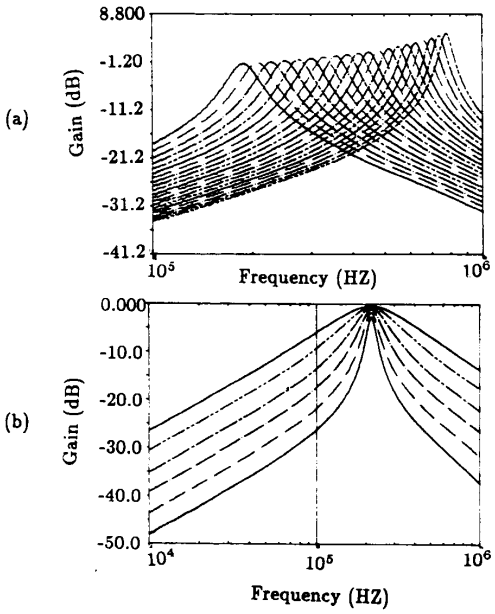

Fig. 10 Programmability of Biquadratic Filter Structure; a) f_0 Adjustment with Fixed Q b) Q Adjustment with Fixed f_0

f_0	Q	Signal Swing V_0* p-p	Noise Density $\mu V/\sqrt{Hz}$	Dynamic Range dB
10 kHz	1.0	1.95	2.52	69.0
100 kHz	0.96	4.36	2.1	66.1
100 kHz	12	4.64	10.0	64.5
1 MHz	1.2	2.10	0.57	63.2
1 MHz	15	2.18	4.5	56.5
1 MHz	142	1.07	32.4	52.6

* Measured at 1% THD.

Table 1 Signal Swing and Noise Performance of Second–Order Bandpass Filter Configuration

10. In Fig. 10(a) the center frequency of a second–order bandpass structure is adjusted by changing $C_6 = C_7 = C_i$ in a nearly constant–Q manner. In Fig. 10(b) the pole Q of the bandpass filter is adjusted in a constant f_0 manner with different values of $g_{m4} = g_{m5} = g_m$.

The measured noise and signal swing performance characteristics for a second–order bandpass filter are summarized in Table 1. The dynamic range in this table is defined to be equal to the ratio of the RMS output voltage at 1% THD divided by the total output RMS noise voltage in the passband of filter.

The results presented in the figures are representative of the performance potential of this structure. At some extreme settings of the circuit parameters and/or at extremes of the excitation, a significant degradation of performance occurs; these are manifested in parasitic oscillations, jump resonance, Q enhancement or degradation, dynamic range reduction and increased nonlinearities. An intelligent controller can thus be used to mitigate these limitations.

Conclusions

A completely programmable and reconfigurable digitally controllable active structure has been presented. A specific implementation which has over 3 decades of adjustment range and is capable of realizing any even-order filter function of up to 6^{th}–order was fabricated and tested. This filter operates over the 1kHz to 1MHz frequency range. Experimental results confirmed both the reconfigurability and programmable characteristics of this structure.

References

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