VERY HIGH PRECISION ANALOG TRIMMING USING FLOATING GATE MOSFETS

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ABSTRACT

The addition of a floating gate MOS transistor option to basic CMOS or BiMOS processes is becoming recognized as a viable option with improvements in thin gate technology and the practical acceptance of increased process complexity. The use of the devices as infinite resolution nonvolatile storage devices and as precision analog trim elements are discussed. Experimental results focusing on the programming resolution and time-stability of the charge retention are presented.

INTRODUCTION

Floating gate MOS transistors currently receive widespread use as the data storage element in EPROM and EEPROM circuits. An example of a floating gate transistor is depicted in Fig. 1. Data is stored in the form of charge on the floating gate of this type of device. These devices have proven practical for binary information storage [1-3] because of the long term charge retention (ten years or more at room temperature) realized for charge stored on the floating gate which is completely surrounded by an insulating layer of SiO_2. In current applications binary information storage is achieved by either placing large amounts of charge on the floating gate or by effectively removing this charge through an open-loop program or erase cycle. These devices can be manufactured quite reliably as is indicated by the fact that one megabit level memory circuits are currently commercially available that use floating gate transistors for data storage.

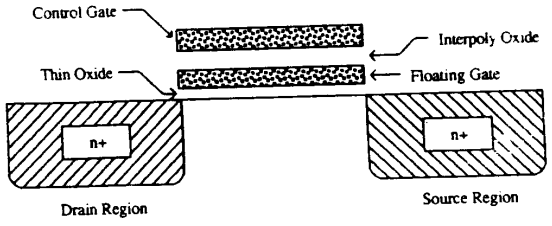

Fig. 1 Cross Sectional View of Floating Gate MOS Transistor

The floating gate transistor has received minimal attention as an analog circuit element [4-5], but it is in this area where unique application potential exists. To utilize the floating gate transistor as an analog circuit element it is necessary to program it using a closed-loop/feedback mode rather than the open-loop mode used for binary applications. To accomplish this it is necessary to understand and control the transfer of charge onto and off of the floating gate of the floating gate transistor. This charge transfer is accomplished using Fowler-Nordheim tunneling of electrons through a thin tunnel oxide beneath the floating gate of the floating gate transistor [6]. By controlling the magnitude and polarity of the electric field established in the tunnel oxide the transfer of charge can be controlled. The charge transfer rate from Fowler-Nordheim tunneling is exponentially related to the electric field in the tunnel oxide, so a wide range of transfer rates can easily be achieved. The transfer of charge onto or off of the floating gate of a floating gate transistor effects the threshold voltage of this device. Using an arbitrarily slow charge transfer rate and dynamically monitoring the threshold voltage of the floating gate device, the amount of charge transferred can be controlled with nearly infinite precision. Since the floating gate transistor can be used, in conjunction with other components, to establish voltage and/or current levels in a circuit which are dependent on the charge on the floating gate, these voltages and/or currents can be trimmed with nearly infinite precision using a dynamically programmed floating gate transistor. Potential applications include offset adjustment, precision trimming and matching, and general analog data storage.

Some of the problems which plague the floating gate transistor in the present applications may be of reduced concern in analog applications. The primary failure mechanism in large EPROM and EEPROM applications is the failure of a small number of floating gate devices to successfully program and retain data after a modest number of program/erase cycles (10^3 - 10^5 cycles). Although only one or a small number of floating gate devices fail, it is unacceptable since the overall memory circuit is no longer fully functional. This device wearout mechanism is related to the total fluence of charge transferred

through the tunnel oxide [7]. In binary operations the fluence of charge for a single program/erase cycle is typically much larger than for analog operations since most trimming or offset adjustments will require transferring small amounts of charge. Along with that, because analog applications will only require a few trim devices, the probability of failures due to device wearout mechanisms is much smaller for analog applications than for the current digital applications.

While the floating gate transistor has good long term charge storage properties, charge is lost off of the floating gate. The charge loss rate is greatest initially and decreases exponentially with time. For binary data storage the loss of a small percentage of the charge stored on the floating gate is not important since only two data states need to be distinguished. For analog applications, however, the loss of a small amount of charge can be of concern. For this reason it is necessary to periodically refresh the programmed state of floating gate transistors used in analog applications. The frequency at which refreshing is required is determined by the precision demanded by the particular application in which the floating gate transistors are used.

A test structure consisting of a floating gate transistor and a series "access" transistor was evaluated in the laboratory. Emphasis was placed upon the charge transfer characteristics and controllability of this device along with its charge retention characteristics. The test structure is shown in Fig. 2.

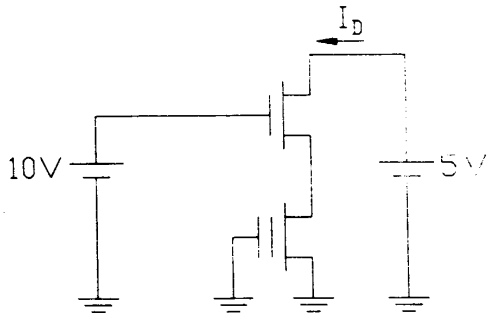

Fig. 2 Read Circuit

CHARGE TRANSFER CHARACTERISTICS

A series of short duration programming pulses were used to transfer charge onto and off of the floating gate of the floating gate transistor. The magnitude, polarity, and duration of these pulses were used to characterize the charge transfer mechanism. Table 1 shows the node voltages applied to the test structure to transfer charge. The amount of charge on the floating gate was determined indirectly by measuring the drain current conducted by the test structure when the bias voltages shown in Fig. 2 were applied.

The results of one charge transfer experiment are shown in Fig. 3. Data are shown for a series of 10μs programming pulses with programming voltages of 18V, 19V, and 20V. From this curve, it should be clear that extremely small increments in drain current conducted by the floating gate transistor can be achieved if programming voltage is dynamically adjusted as part of a feedback based programming algorithm.

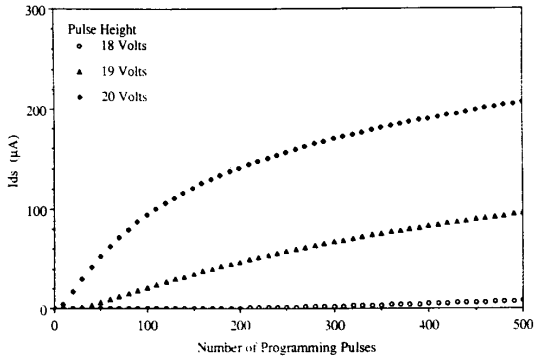

Fig. 3 Drain Current vs Number of Programming Pulses

Data like that shown in Fig. 3 can be converted to show the change in the threshold voltage of the floating gate transistor. This was done to produce Fig. 4 which shows threshold voltage for the floating gate transistor versus the pulse width of the applied programming pulses for several different numbers of 20V programming pulses.

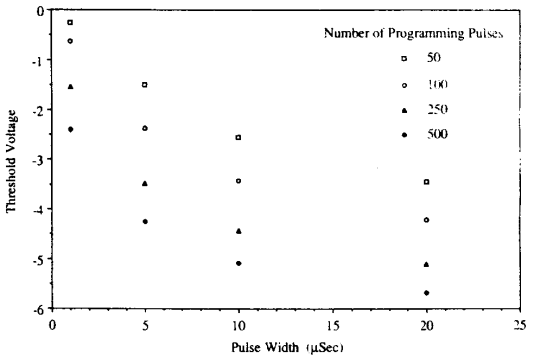

Fig. 4 Threshold Voltage vs Pulse Width of Programming Pulses

An expression can be derived to explicitly show the change in threshold voltage of the floating gate transistor as a function of programming voltage and time [8]. The expression shown below is for net positive accumulation of charge on the floating gate.

$$\Delta V_t\,(V_{pr},\ t) = -V_{pr} + \frac{A}{ln\left(exp\left(\frac{A}{V_{pr}}\right) + Bt\right)} \qquad (1)$$

where A and B are constants determined by device geometries and materials and V_{pr} is the programming voltage as defined in Table 1. A similar expression, obtained by multiplying the right hand side of (1) by -1, characterizes the net negative charge accumulation as well

CHARGE RETENTION

The primary mechanism for charge loss off of the floating gate of a floating gate transistor is thermionic emission of electrons [9]. An expression modeling this mechanism is shown below,

$$\frac{Q(t)}{Q(0)} = exp\left(\nu t\ exp\left(\frac{-\Phi_B}{kT}\right)\right) \qquad (2)$$

where Q(0) and Q(t) represent the amount of charge on the floating gate immediately and at a time t after programming the device respectively, υ represents the frequency of interactions for the charged particles on the floating gate, Φ_B represents the energy barrier that a charged particle on the floating gate must overcome to leave the floating gate, k represents Boltzman's constant, and T represents the temperature in Kelvin.

The value for Q(t)/Q(0) can be derived from measured values of $V_T(t)$ and $V_T(0)$. It is easily shown in that,

$$\frac{Q(t)}{Q(0)} = \frac{(V_T(t) - V_{T0})}{(V_T(0) - V_{T0})} \qquad (3)$$

where $V_T(t)$ is the threshold voltage of the floating gate transistor at time t after programming, $V_T(0)$ is the threshold voltage of the floating gate transistor immediately after programming, and V_{T0} is the threshold voltage of the floating gate transistor before any charge has been transferred onto it.

The acceleration of charge loss between two temperatures can be shown to be,

$$A_{cc} = exp\left[\left(\frac{-\Phi_B}{k}\right)\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right] \qquad (4)$$

Thus, if it took t_2 hours to lose a fixed percent of stored charge at the temperature T_2 it would take $A_{cc}*t_2$ hours to lose the same percentage of stored charge at temperature T_1. The exponential relationship between time and temperature allows for substantial accelerations for relatively small changes in temperature. Experiments were conducted at elevated temperatures to determine the rate of charge loss for both positive and negative net charge accumulation on the floating gate of the floating gate transistor. The results of those experiments are shown in Fig. 5 and Fig. 6.

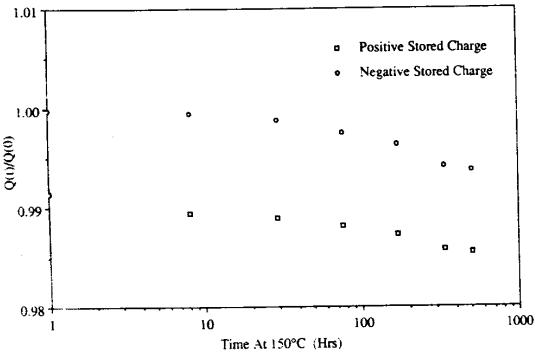

Fig. 5 Charge Lost Off Floating Gate at 150°C

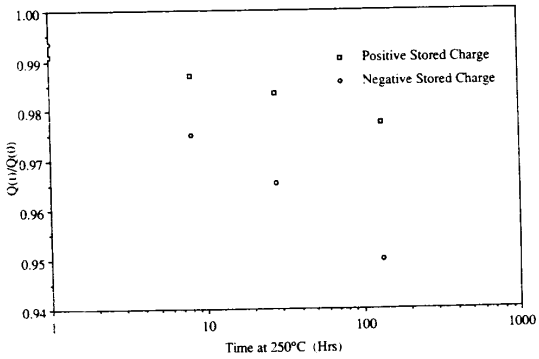

Fig. 6 Charge Lost Off Floating Gate at 250°C

Using the data collected on this long term charge loss mechanism it can be shown that the acceleration factor between 250 degrees centigrade (523 K) and 150 degrees centigrade (423 K) is approximately 31 for net negative accumulations and 16.5 for net positive accumulations. Based on this, for operation at 25 degrees centigrade less than 2% stored charge would be lost in 10 years for net positive charge accumulations and less than 1% would be lost for net negative accumulations.

CONCLUSIONS

The data presented clearly indicate that very fine and predictable resolution of the amount of charge transferred onto or off of the floating gate of a floating gate transistor can be achieved by the selection of programming voltage and time. A dynamic programming scheme in which measurements are made between programming steps to determine the amount of charge on the floating gate can be used to program/trim analog circuits with nearly infinite precision. Charge is lost off of the floating gate at a relatively slow rate and can be compensated for by reprogramming the device on a periodic basis. Using these two key concepts, dynamic programming and periodic refreshing, the floating gate transistor can be applied in a whole new range of analog applications.

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