BASE RESISTANCE AND PN JUNCTION CAPACITANCE EXTRACTION ON VERTICAL BIPOLAR TRANSISTORS

Moisés E. Robinson G.[1], Horacio Nevárez–Lozano,[1], Jaime Ramírez–Angúlo[1], Randall L. Geiger[1], Peter Wang[2] and Larry Goff[2].

[1]Department of Electrical Engineering
Texas A&M University, College Station, TX 77843–USA

[2]Texas Instruments Inc.
Dallas, TX 75265–USA

Abstract–The base resistance and the pn junction capacitances are two of the most important electrical parameters that characterize bipolar transistors. Many attempts have been made in the past years to accurately obtain these two parameters, but the high non-linearity associated with both the base resistance and the pn junctions in general have made it very difficult to obtain these parameters. In this paper we review the general concepts and a formulation that can be adopted to extract the base resistance for typical transistor structures. We also introduce a formulation for the calculation of zero-bias space–charge–region capacitances of pn junctions. This formulation gives very good agreement between simulated and measured capacitance values (better than 5% agreement) even for subpicofarad devices.

I. INTRODUCTION

The base resistance (R_b) is a distributed and nonlinear resistance. It's value depends on the collector current density of the transistor (J_C) as well as on several physical mechanisms. R_b limits the rate at which the input capacitance can be charged and is therefore one of the reasons why bipolar transistors do not operate at the frequencies predicted by the values of the forward transit time [1]. R_b also plays a major role on the dc, ac and noise performance of bipolar transistors. A valid formulation must be adopted to match this distributed base resistance to an equivalent lumped base resistor that can be useful for lumped circuit analysis.

Based on a one–dimensional analysis of physically unrealistic transistor structures, several researchers derived a group of equations that have been widely used by bipolar transistor designers for the calculation of the maximum value of the base resistance (RB) [3-5]. Due to the limited applicability of these equations, a power conservation method has been proposed recently for the extraction of the distributed base resistance (extrinsic plus intrinsic components) [2,6,7,8]. In this approach, an equivalent lumped base resistor is assumed to dissipate the same amount of power that is dissipated by the base current in the base region of the actual distributed transistor. Using this power conservation method, Hébert and Roulston [7] derived a new group of equations for the calculation of RB. These equations can be used to compute the base resistance for single and double base contact bipolar transistors with rectangular emitters, given the mask dimensions and the resistivity of the extrinsic and intrinsic base regions. The same power dissipation approach can be used to extract the base resistance of arbitrarily shaped bipolar transistors. In Section II of this paper we discuss the general implementation of this approach.

The capacitances of pn junctions also play a significant role in the switching speed and frequency response of bipolar devices. In particular, the base– collector capacitance is very important in determining the ac performance of a bipolar transistor. The importance arises because of the Miller effect. In Section III we introduce a new formulation for the calculation of the zero-bias capacitance of pn junctions.

II. BASE RESISTANCE OF VERTICAL BIPOLAR TRANSISTORS

The resistivity of the extrinsic base region is very low compared to the resistivity of the intrinsic base region. For non–walled emitter transistors, most of the base current takes the low resistivity path to the active region where it supplies carriers for recombination in the base and to be injected into the emitter as depicted in Fig. 1(a) [9].

A power dissipation method can be adopted to extract the value of the equivalent lumped base resistor that will dissipate the same amount of power that is dissipated by the base current in the base region of the transistor. Consider the single base–contact vertical transistor shown in Fig. 2(a) and the

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equivalent circuit approach discussed in [2,6] to approximate the distributed system with a finite lumped system. A single uniform grid is superimposed on the structure. Each of the square elements can be grouped into one of three mutually exclusive groups denoted as,

a) Contact b) Extrinsic Base c)Active Transistor.

A lumped circuit model of the overall structure is obtained by mapping each square into a lumped circuit. The equivalent circuit for each of these groups is shown in Fig. 2(b), (c) and (d). These approach is similar to the one discussed in [2,6]. These elemental circuits are then interconnected to form a pseudo three–dimensional model of the BJT where the elemental nodes labeled B, C and E respectively, form the equivalent Base, Collector and Emitter nodes of the single equivalent transistor that is being modeled.

In the contact elemental circuit of Fig. 2(b), the resistance R_{CT} denotes the vertical elemental resistance from the contact to the extrinsic base region and R'_{BE} characterizes the lateral base resistance underneath the base contact. R'_{BE} is related to the sheet resistance ρ'_{be} in the diffusion under the contact by

$$R'_{BE} = \frac{\rho'_{be}}{2} \tag{1}$$

The elemental extrinsic base region of Fig. 2(c) is comprised of an interconection of four resistors R_{BE}. These are obtained from the sheet resistance in the extrinsic base region (ρ_{be}).

$$R_{BE} = \frac{\rho_{be}}{2} \tag{2}$$

The elemental transistors in Fig. 2(d) are characteristic of the process. Parameters for these transistors can be obtained from either impurity profile data or from measurements made on specific test structures. The lateral grid connections are provided through the $R_{BI}(x,y)$ grid where R_{BI} characterizes the intrinsic lateral base resistance and is found from the sheet resistance of the intrinsic base region ($\rho_{bi}(x,y)$).

$$R_{BI}(x,y) = \frac{\rho_{bi}(x,y)}{2} \tag{3}$$

A general purpose bipolar transistor simulator has been developed to analyze arbitrarily shaped bipolar transistors. We used this simulator to extract the value of *RB* for single and double base contact vertical *npn* transistors with square emitters based on the power conservation approach. The test structures are shown in Fig. 3. In this simulation, we used parameters $R_{CT} = 0\Omega$, $R'_{BE} = R_{BE} = 65\Omega$, $R_{BI} = 2500\Omega$, $\beta = 100$, $R_E = 60\Omega$, $R_C = 25K\Omega$ (R_E and R_C are inversely proportional to the step size of the discretization grid). These are typical of current bipolar processes. The results of the simulation are summarized in Table 1 and the are in good agreement with the equations derived by Hébert and Roulston [7].

III. CLOSING THE GAP BETWEEN MEASURED AND CALCULATED CAPACITANCE VALUES

Although the capacitance of pn–junctions has been the focus of intensive research during the past three decades [10–15], a unique and reliable model which accurately predicts the actual capacitances is yet to be adopted by circuit designers. As modern IC technology continues to scale down device sizes, it becomes more important to develop models that take into account the physical nonlinearity and three dimensional effects inherent to pn junctions; models capable of predicting capacitance values in good agreement with values obtained using high-precision measurement techniques.

In this section we present a novel formulation for the calculation of the zero-bias–space charge capacitance of pn junctions, but first we will introduce one of the concepts that will be used in this formulation. Kennedy and O'Brien [16] made a comprehensive mathematical investigation of the impurity atom distribution within a planar pn junction. They carried the analysis for two fundamentally different diffusion processes. In one of the processes, a fixed quantity of impurity atoms was involved in the entire diffusion process; in the other, a constant impurity atom concentration was maintained at the semiconductor surface. By a rigorous mathematical solution of these diffusion processes, they showed that both types of processes exhibit a greater penetration of impurity atoms in a direction perpendicular to the semiconductor surface (Fig. 4), and that the calculated contour of maximum constant atom density (W_M) is smaller than the mask opening (W_E). The transition from bottom (or planar) to sidewall (or peripheral) region occurs at point A' and B' and not at points A and B as assumed in most of the currently used models. We define a shrinking factor (SF) as the distance from the edge of the diffusion mask (points A and B) to the point where the maximum constant atom density is reached (points A' and B').

$$SF = \frac{W_E - W_M}{2.0} \tag{4}$$

SF can be formally treated as a process parameter which characterizes sidewall encroachment in diffused junctions.

Liou and Yuan [10] recently presented a comprehensive 2-D (planar and peripheral) quasi-static emitter-base space-charge region capacitance model, but they neglected some of the 2-D effects inherent to the junction. They neglected the capacitance introduced by all four corners and they included only two of the four peripheral regions that are present on pn

junctions with square emitters. We concentrate our discussion on the base to emitter capacitance of bipolar transistors but the proposed formulation is suitable for extracting the zero–bias capacitance of any planar pn junction.

Consider the top view of the single base contact transistor of Fig. 5. Liou and Yuan [9] presented a comprehensive 2–D (planar and peripheral) quasi–static base to emitter space–charge–region capacitance model, but they neglected the capacitance introduced by all four corners and they included only two of the four peripheral regions that are present on the base to emitter junction of the transistor in Fig. 5.

The total base to emitter capacitance can be written as:

$$\begin{aligned} C_{BE} = & (L_E - 2.0 * SF) * (W_E - 2.0 * SF) * C_{bottom} + \\ & 2.0 * (L_E - 2.0 * L_C) * C_{sidewall} + \\ & 2.0 * (W_E - 2.0 * L_C) * C_{sidewall} + \\ & 4.0 * C_{corner} \end{aligned} \quad (5)$$

where C_{bottom}, $C_{sidewall}$ and C_{corner} are the capacitance densities corresponding to the bottom, periphery and corners of the pn junction respectively. SF is the shrinking factor and L_C defines the transition point from periphery to corner. All these parameters can be obtained from measurements made on carefully designed test structures or from three dimensional simulations of the junction. W_E and L_E are the drawn width and length of the emitter region. Table 2 shows a comparison between measured and calculated capacitances values. The shrinking factor was obtained by extraction from measurements made on a special test structure. As can be seen in this table, very good agreement between theoretical and experimental data can be obtained using the proposed formulation even for subpicofarad capacitances.

CONCLUSION

The implementation of the power conservation approach for the extraction of the base resistance of bipolar transistors has been reviewed. Also, a new formulation for the calculation of the zero–bias capacitance of pn junctions has been presented. A general purpose bipolar transistor simulator has been used to extract both the base resistance and the pn junction capacitances of arbitrarily–shaped bipolar transistors based on the discussed formulations. Simulated results are in good agreement with values obtained using high–precision measurement techniques.

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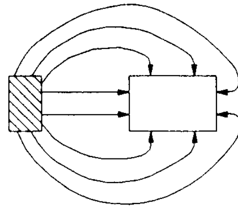

Fig. 1 Base current path for non–walled emitter, single base contact transistor [9].

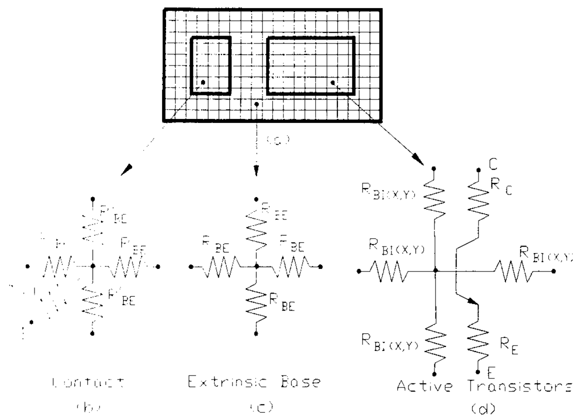

Fig. 2 Pseudo three–dimensional model of the vertical bipolar transistors; (a) Top view showing rectangular grid, (b) Elemental contact model, (c) Elemental extrinsic base resistance model, (d) Elemental active transistor model.

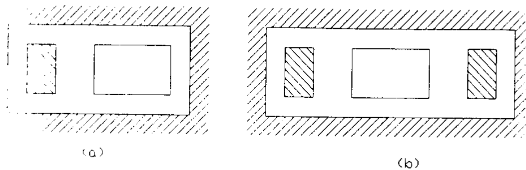

Fig. 3 Test Structures Simulated (vertical bipolar transistors). (a) Single–base contact transistor, (b) Double–base contact transistor.

Single Contact Transistor	311
Double Contact Transistor	224

Table 1 RB for single and double base–contact transistors(in Ω).

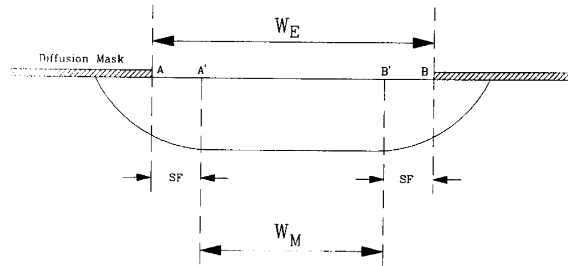

Fig. 4 Contour of constant impurity atom density on a planar pn junction and geometrical description of the shrinking factor.

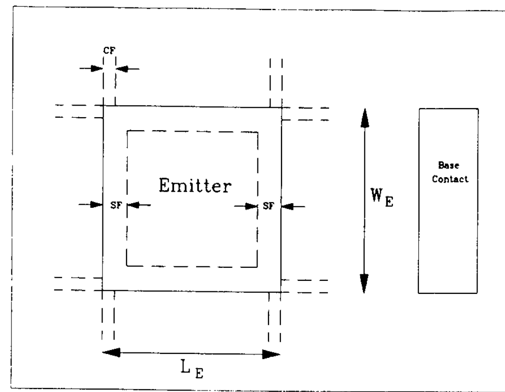

Fig. 5 Top view of a single base contact transistor showing the geometrical and physical parameters needed for the calculation of the base to emitter capacitance.

W (mil)	L(mil)	Simulated	Measured
0.65	0.65	365.5 ff	370 ff
1.46	1.46	1.13 pf	1.1 pf
1.75	3.5	3.07 pf	3.0 pf

Table 2 Base to emitter capacitance values for rectangular junctions of different sizes. SF = 1.8*(emitter vertical diffusion depth).