

AN ALGORITHM TO COMPENSATE FOR SOURCE SPECTRAL IMPURITY IN DYNAMIC RANGE MEASUREMENTS

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Abstract- *Dynamic testing of high-speed, high-performance, analog-to-digital converters (ADCs) requires instruments that must have better dynamic range (signal-to-noise ratio) than the ADC under test to achieve reliable results. A major limitation in these measurements is the distortion of the signal generator, which is used as the input excitation, especially at frequencies over 1 MHz. A novel algorithm is described to compensate for the effect of signal source distortion in the measurement of dynamic performance of ADCs. The algorithm uses two sets of measurements: one set taken with the function generator and another taken with an all-pass filter inserted between the function generator and the ADC. Simulation results indicate that ADCs with a dynamic range of 60-70 dB can be measured with an absolute accuracy of better than 0.2 dB using a signal generator that has -40 dB distortion components.*

INTRODUCTION

The most important performance indicator of ADCs is the signal-to-noise plus distortion ratio (SNDR) or equivalently the number of effective bits [1]. The measurements are typically done either in the analog domain or in the digital domain[2]. In the analog domain, the output of the ADC is fed to a digital-to-analog converter (DAC) and the analog output is analyzed using either a spectrum analyzer or a distortion analyzer to measure the SNDR. This method is very sensitive to noise and distortion generated by the DAC and is therefore unreliable for testing high-performance ADCs. A typical digital domain measurement that uses the Fast Fourier Transform (FFT) to perform the SNDR measurement is shown in Figure 1. Here, the ADC output data is first stored in a digital memory. The data is then analyzed using the FFT to determine the SNDR. In both the analog and digital domain testing methods, the test stimulus is a full-scale sine wave. Regardless of the method used, the SNDR of the function generator must be better than that of the ADC in order to measure the true SNDR of the ADC. The ideal dynamic range of an n-bit ADC is equal to $6.02n + 1.78dB$, where n is equal to the number of bits [1]. Therefore, the spectral purity of the input sinewave must be better than this value to measure the true SNDR of the ADC. For example, if a 12-bit converter (ideal SNDR=74.02dB) has an actual SNDR of 70dB due to a second harmonic at 72.2 dB, the function generator must have a linearity of better than -100dB to be able to measure the true SNDR with an absolute accuracy of better than 0.27dB (this calculation assumes an in-phase addition at the ADC output of a second harmonic due to the function generator and a second harmonic due to the ADC). Table 1 lists the linearity specifications of some of the commonly used commercially available signal generators (the measured values are usually 5 to 10dB better than the specified values). It is clear from this Table that the best non-linearity specification is about -100dB for frequencies less than 200KHz and degrades for higher frequencies. However, 12-bit ADCs operating beyond this frequency range are commercially available [3] and therefore the absolute measurement error will

be worse than predicted above, if this function generator were used. This situation is only worsened when we take into account ADCs that have more aggressive specifications than the one above. For example, the ADC in [4] has 10-bits of resolution and operates at 60MHz. Ideally, this ADC could have a dynamic range of 61.96dB. From Table 1, it is clear that there is no function generator that has a linearity even close to this value, in the frequency range of interest.

It is obvious from the above discussion that the nonlinearity of the signal source has a major influence on the measured results and puts an upper bound on the measurable dynamic range of ADCs. In a practical measurement setup this problem is usually circumvented by using a band-pass filter to filter out the harmonics in the signal source. However, this has the disadvantage of having to tune the filter for every frequency the ADC is being tested at.

In this paper, an algorithm is presented that compensates for the effect of the source spectral impurity on the measured SNDR of the ADCs. It is assumed, for the sake of illustration of results, that an FFT based method is being used to measure the SNDR of the ADC. Although an ADC is taken as an example to test the algorithm, the algorithm is very general in nature and can be applied to any similar situation where the nonlinearity of a mixed analog/digital circuit is being measured using a spectrally impure signal source and the measured results are available in the digital form.

DESCRIPTION OF THE ALGORITHM

Let the input to the device under test (DUT) be a sum of complex exponentials given by:

$$V_i(t) = A_1 \exp^{j\omega t} + A_2 \exp^{j2\omega t} + A_3 \exp^{j3\omega t} \quad (1)$$

where terms containing A_2 and A_3 model the second and third harmonic distortion components present in the signal source. Additional harmonics should be included to this model if the source non-linearity is not sufficiently modeled by the second and third harmonics. In the absence of any non-linearities in the DUT, the system response to $V_i(t)$ would be that of a linear system. In the presence of weak non-linearities, the DUT can be modeled as a weakly non-linear or a quasi non-linear system [5]. The system (modeled as a weakly non-linear system) response due to the first term of Eq. 1 can be written as:

$$V_{o1}(t) = H_{11}A_1 \exp^{j\omega t} + H_{12}(A_1 \exp^{j\omega t})^2 + H_{13}(A_1 \exp^{j\omega t})^3 + \dots \quad (2)$$

Similarly, the output due to the second and third terms can be written as:

$$V_{o2}(t) = H_{22}A_2 \exp^{j2\omega t} + H_{24}(A_2 \exp^{j2\omega t})^2 + \dots \quad (3)$$

$$V_{o3}(t) = H_{33}A_3 \exp^{j3\omega t} + H_{36}(A_3 \exp^{j3\omega t})^2 + \dots \quad (4)$$

where H_{12}, H_{13} etc... are complex gain factors of the non-linear system.

When all three terms in Eq. 1 are considered as input to the DUT, in addition to the responses given above, there will be additional terms as a result of the inter-modulation among the three input components. If the nonlinearity of the source and the DUT are small, these inter-modulation products can be neglected [5]. Under this assumption, the system response equals the summation of Eq. 2, Eq. 3 and Eq. 4, and the sum can be written as:(neglecting terms higher than the third harmonic):

$$V_{OS}(t) = OS_1 \exp^{j\omega t} + OS_2 \exp^{j2\omega t} + OS_3 \exp^{j3\omega t} \quad (5)$$

where

$$OS_1 = H_{11}A_1 \quad (6)$$

$$OS_2 = H_{12}A_1^2 + H_{22}A_2 \quad (7)$$

$$OS_3 = H_{13}A_1^3 + H_{33}A_3 \quad (8)$$

Fundamental to the above equations is the assumption that the system response is a result of the superposition of the response of the different input signal components. As long as the system remains weakly non-linear and the distortion of the signal source is small, this assumption is valid.

From Eqs. 7 and 8 we see that a knowledge of the complex gain terms is necessary to separate the measured harmonic energy into the contribution from the ADC (the quantity of interest) and the contribution from the signal source. However, this will require another set of *independent* equations similar to Eqs. 7 and 8, so that the resulting sets of equations can be solved for the complex gain factors.

The second set of independent equations can be obtained by placing an all-pass filter in front of the DUT as shown in Figure 2. This process will change the phase of all harmonic components of the function generator and result in a new set of inputs being applied to the ADC, *without* changing the distortion generated by the ADC. Theoretically, any linear circuit that gives a non-linear phase response can be used in place of the all-pass filter as long as three requirements are satisfied. First, the impedance seen by the signal source must be the same when it drives either the ADC or the filter. This will guarantee that the distortion of the signal source (which depends on loading conditions) remains unchanged. Second, the magnitude of the signal to the ADC must be the same, whether it has the filter or the signal source in front of it. This assures that the distortion generated by the ADC is the same for both cases. Finally, the linearity of the filter must be much better than that of the DUT. A family of passive *constant-impedance* all-pass ladder filters that fulfill these requirements is presented in [6].

In Fig. 2, the signal at the output of the all-pass filter is given by (assuming that the filter has negligible nonlinearity):

$$V_{if}(t) = A_1T(j\omega)\exp^{j\omega t} + A_2T(j2\omega)\exp^{j2\omega t} + A_3T(j3\omega)\exp^{j3\omega t} \quad (9)$$

where $T(j\omega)$ is the filter transfer function. The response at the output of the DUT to this input is given by:

$$V_o(j\omega t) = OT_1 \exp^{j\omega t} + OT_2 \exp^{j2\omega t} + OT_3 \exp^{j3\omega t} \quad (10)$$

where:

$$OT_1 = H_{11}A_1T(j\omega) \quad (11)$$

$$OT_2 = H_{12}(A_1T(j\omega))^2 + H_{22}A_2T(j2\omega) \quad (12)$$

$$OT_3 = H_{13}(A_1T(j\omega))^3 + H_{33}A_3T(j3\omega) \quad (13)$$

The above equations together with equations (7) and (8) can be used to find the desired complex gains H_{12} and H_{13} . The resulting expressions are given below:

$$H_{12}A_1^2 = OS_2 \frac{T(j2\omega) - T(j\omega)}{T(j2\omega) - T(j\omega)^2} - \frac{T(j\omega)}{T(j2\omega) - T(j\omega)^2} OS_1 \left(\frac{OT_2}{OT_1} - \frac{OS_2}{OS_1} \right) \quad (14)$$

$$H_{13}A_1^3 = OS_3 \frac{T(j3\omega) - T(j\omega)}{T(j3\omega) - T(j\omega)^3} - \frac{T(j\omega)}{T(j3\omega) - T(j\omega)^3} OS_1 \left(\frac{OT_3}{OT_1} - \frac{OS_3}{OS_1} \right) \quad (15)$$

Knowing what the corrected 2nd and 3rd harmonic outputs are, the signal-to-noise plus distortion ratio can be easily calculated.

RESULTS

Nonlinearity in high-speed ADCs can be classified into two categories: static nonlinearity and dynamic nonlinearity. Static or DC nonlinearity in ADCs is due to deviations in the threshold voltages that define the trip points of the ADC. The deviation in the threshold voltages itself is a result of component mismatches and other process parameter variations. This type of nonlinearity can be measured using DC signals and expressed as both differential nonlinearity (DNL) and integral nonlinearity (INL). However, high-speed ADCs are notorious for dynamic errors, and static DNL and INL curves do not reveal this kind of errors. For this reason, it is becoming almost a standard practice to specify the dynamic performance degradation of these ADCs by means of SNDR measurements.

As an example of dynamic nonlinearity in high-speed ADCs, let us consider a flash converter. In this type of high-speed ADC, the exact sampling instant of the input signal is undefined due to the finite delay associated with the transmission of the clock and the input signal. This lack of synchronization between the input and the clock signal (due to mismatches in the transmission lines carrying these signals) gives rise to what is commonly known as timing uncertainty and leads to an *instantaneous* error in the sampled voltage. If the voltage error is systematic (signal dependent), it will cause distortion in the ADC, and if it is random (for example, due to clock jitter) it increases the random noise generated by the ADC. This mechanism is one of the major sources of SNDR degradation in flash ADCs [7]. Timing uncertainty in an ADC can be modeled by a timing error associated with the ideal sampling time nT . According to this model, for example, if the input to the ADC is a sine wave ($A \sin \omega t$) then the response of the ADC is given by:

$$V_o(t) = A \sin(\omega(nT + t_{error})) \quad (16)$$

where t_{error} is the timing error at nT . The instantaneous er-

ror in the sampled voltage is a function of both t_{error} and ω . Making t_{error} a function of the input level distorts the output signal. Also, note that this distortion will increase if ω is increased because now for the same instantaneous timing error, the instantaneous voltage error will be larger due to the increased slew rate of the signal. Hence, according to this model, the distortion of the ADC goes up if either the amplitude or the frequency of the input signal (slew rate of the signal) goes up.

Figure 3 shows a possible timing error function t_{error} . This curve may be thought of as a timing delay mismatch between the clock and signal lines of a *hypothetical* 12-bit flash converter with four rows of comparators. The exactness of this curve is not critically important to us; this curve is used only as a model to introduce distortion in the ADC (the exact curve would have a quadratic response rather than a linear response). It has also been observed that this kind of timing error gives rise to strong odd harmonics in the output frequency spectrum of the ADC.

Figure 4 shows the SNDR curve (for the simulated 12-bit converter) that was obtained using the behavioral model represented in equation (16) and the t_{error} function shown in Figure 3, assuming a spectrally-pure signal source ($V_i(t) = A \sin \omega t$ in Eq. 1). In this Figure, SNDR is plotted as a function of the input amplitude for a frequency of 1.56 MHz; this curve was generated by taking samples of Eq. 16, applying the Fast Fourier Transform (FFT) on the resulting sequence, and estimating the harmonics. Mathematically, SNDR can be expressed as:

$$SNDR = \sqrt{\frac{|H_{11}A_1^2|^2}{|H_{12}A_1^2|^2 + |H_{13}A_1^3|^2 + |H_{14}A_1^4|^2 + \dots + e^2}} \quad (17)$$

where e^2 is the background noise. In Figure 4, observe that random noise dominates SNDR when the signal level is low, and distortion dominates the SNDR at full scale input.

For simulation purpose, the ratio between the input frequency and the clock frequency was so chosen that the spectral leakage due to windowing was negligible. In this way, the computational errors caused by using the FFT in estimating the harmonics are kept to a minimum, and therefore the errors in the compensated harmonics are purely errors resulting from the algorithm itself.

Now, if we assume that the signal source has 2^{nd} and 3^{rd} harmonics at 40dB below the fundamental, the resulting SNDR curve is as shown in Figure 5 (solid curve). It is evident from this Figure that the measurable dynamic range is always limited to less than 37dB due to the nonlinearity of the source. The dotted curve is the SNDR curve after applying the correction algorithm. To see the exact difference between this recovered SNDR curve and the ideal SNDR curve (Figure 4), the difference is plotted in Figure 6. As can be seen the algorithm performs extremely well with the indicated distortion process.

The transfer function used in the simulation for the all-pass filter is:

$$T(j\omega) = \frac{1 - j\omega RC}{1 + j\omega RC} \quad (18)$$

This is an ideal first order transfer function and in a practical realization of this transfer function, component nonidealities such as parasitics associated with passive elements will result in a nonideal transfer function. In addition, the measurement of the resulting transfer function itself is going to introduce some errors. These effects must be taken into account in a practical realization of the all-pass filter.

Table 2 lists the simulation results for several combinations of source distortion levels. Note that the errors due to compensation get larger as the source distortion goes up. To investigate the effect of measurement error that may result in measuring the all-pass filter transfer function, a 1% error was deliberately introduced to the $T(\omega)$ terms in equations (14) and (15). The resulting performance of the algorithm (assuming a signal source with a 2^{nd} and 3^{rd} harmonic 60dB below the fundamental) is also listed in Table 2.

CONCLUSIONS

An algorithm to measure the *true* dynamic performance of high-speed ADCs using a spectrally impure signal source has been described. Basically, the algorithm separates the observed nonlinearity into contributions from the signal source and the ADC. Hence, it is also possible to characterize the signal source itself. The limitation to the algorithm comes from the assumptions made about the nonlinearity of the ADC. With present day converters where gross nonlinearities (such as nonmonotonicity) are rare phenomena, this algorithm is expected to perform as described. Finally, the algorithm provides a very economical solution to testing high-performance ADCs using low-cost function generators.

REFERENCES

- [1] Understanding High-Speed A/D Converter Specifications. Analog Devices, Computer Labs, 1974.
- [2] Product note 5180A-2, Hewlett-Packard, "Dynamic Performance Testing of A/D Converters."
- [3] Donald A. Kerth *et al*, "A 12-bit 1-MHz Two-Step Flash ADC", *IEEE J. Solid-State Circuits*, vol.24, No. 2, pp. 250-255, Apr. 1989.
- [4] Chuck Lane, "A 10-bit 60 MSPS Flash ADC", *Proceedings of the Bipolar Circuits and Technology Meeting*, Minneapolis, MN, pp. 44-47, Sept. 1989.
- [5] Donald D. Weiner and John E. Spina, "Sinusoidal Analysis of Weakly Non-linear Systems", Van Nostrand Reinhold Company, 1980.
- [6] Arthur Williams *et al*, *Electronic Filter Design Handbook*. Chapter 7, McGraw-Hill Publishing Co., 1988.
- [7] Michihiro Inoue *et al*, "A Monolithic 8-bit A/D Converter with 120 MHz Conversion Rate," *IEEE J. Solid-State Circuits*, vol. SC-19, NO.6, pp. 837-841, Dec. 84.

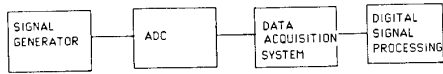


FIGURE 1 Typical Dynamic Range Measurement Setup for ADCs

Table 1. DISTORTION IN SIGNAL GENERATORS

Model	Frequency Range	Distortion	Op. Freq.
Bruel & Kjaer 1049	0.2Hz - 200KHz	-96 dB	20Hz - 200KHz
HP 3326	0 - 13MHz	-80 dB	10Hz - 100KHz
		-65 dB	100KHz - 1MHz
HP 3335	200Hz - 81MHz	-45 dB	200Hz - 10 MHz
		-40 dB	10MHz - 81MHz
HP 3325	1MHz - 20MHz	-60 dB	50KHz - 200KHz
		-40 dB	200KHz - 2MHz
		-30 dB	2MHz - 15MHz
		-25 dB	15MHz - 20MHz

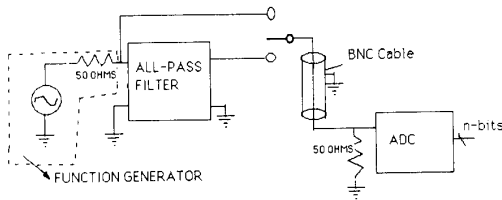


FIGURE 2 Typical Setup for Implementing the Correction Algorithm

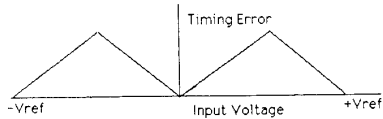


FIGURE 3 Timing Error (Terror) as a Function of Input Level

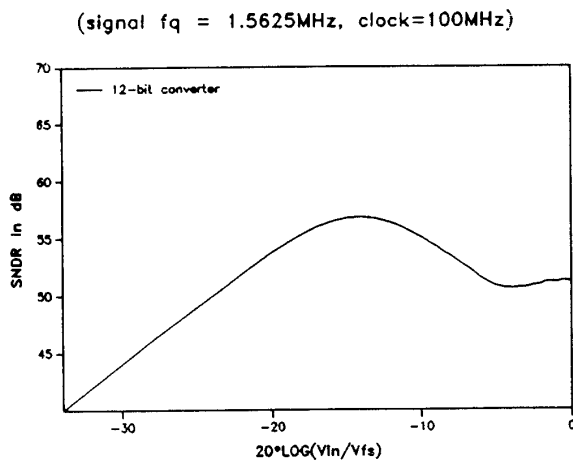


Figure 4: SNR Reduction due to Timing Error Shown in Fig. 3

(signal fq = 1.5625MHz, clock=100MHz)

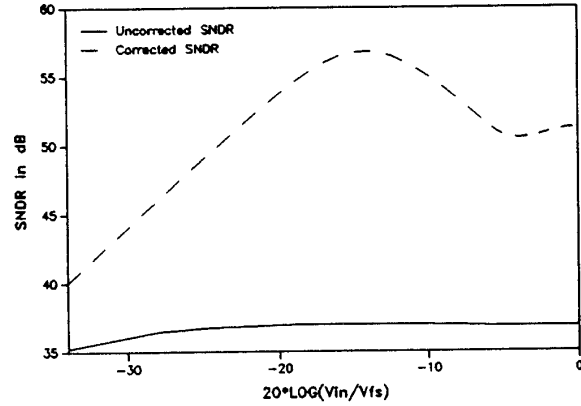


Figure 5: SNR Curves When the Signal Source has 2nd and 3rd Harmonics at -40dB.

(signal fq = 1.5625MHz, clock=100MHz)

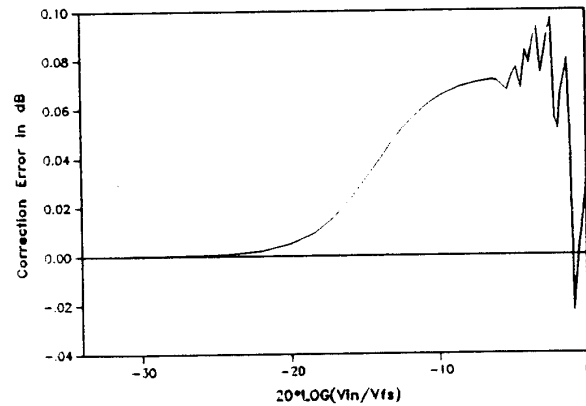


Figure 6: Correction Error when the Signal Source has -40dB Harmonics

TABLE II

SIMULATED PERFORMANCE OF THE CORRECTION ALGORITHM

Source Spectral Impurity	Maxm. Measurable SNDR without Correction	Maximum Correction Error
2nd Harmonic -40dB	37dB	0.1db
3rd Harmonic -40db		
2nd Harmonic -20dB	17dB	1.3db
3rd Harmonic -20dB		
2nd Harmonic -60dB	57dB	0.6dB
3rd Harmonic -60dB		
1% Error in T(ω)		