A PROGRAMMABLE DIGITALLY-TUNED CMOS OTA-C BANDPASS FILTER ARCHITECTURE FOR HIGH-ACCURACY APPLICATIONS

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ABSTRACT

An architecture is presented of a digitally programmable CMOS OTA-C (operational transconductance amplifier and capacitor) analog filter which is controlled, characterized and tuned by a microprocessor in the field. Two elements of this architecture, the highly accurate performance measurement system and the tuning algorithm, are discussed in detail. Experimental results show that this versatile architecture is suitable for high-accuracy, high-frequency or high-Q continuous-time filtering applications, as well as those requiring in-field self tests or in-field programming.

1. INTRODUCTION

Active continuous-time filters fabricated in a monolithic CMOS technology are considered viable for filtering continuous-time waveforms, particularly in high-frequency applications. These filters typically require post-fabrication tuning to correct for process variations, temperature changes, aging, parasitic variation and over-ordering effects. Phase-lock loop or vector-lock loop technologies are commonly used to tune the frequency response of the filter, either directly or indirectly [1–5]. The frequently used indirect tuning strategies [1–4] are sensitive to component mismatch between the tuned block and the filter, as well as being limited at high frequencies by tuning-circuitry performance and filter over-ordering effects that cause deviations from an ideal response at frequencies dissimilar to the tuning circuit's reference frequency. Direct tuning strategies [5] are less developed, but eliminate the sensitivity to mismatch while retaining the high-frequency limitations. A novel microprocessor-based direct tuning strategy that addresses these high-frequency limitations and over-ordering effects by directly tuning the filter's gain transfer characteristics at multiple frequencies is presented here.

2. DIGITAL TUNING STRATEGY

Three interrelated functional blocks comprise the digital tuning strategy in this architecture (Fig. 1). The tuning algorithm adjusts certain digital control words within each of the programmable biquadratic blocks of the analog filter with the goal of adjusting a parametric representation of the biquad's gain frequency response to a user-supplied specification. This parametric representation typically corresponds to, but is not restricted to, the mathematical terms of the transfer function (e.g., f_o and Q). The performance monitor extracts this parametric data by using curve-fitting techniques on a series of discrete frequency and gain coordinates that characterize the filter's gain frequency response.

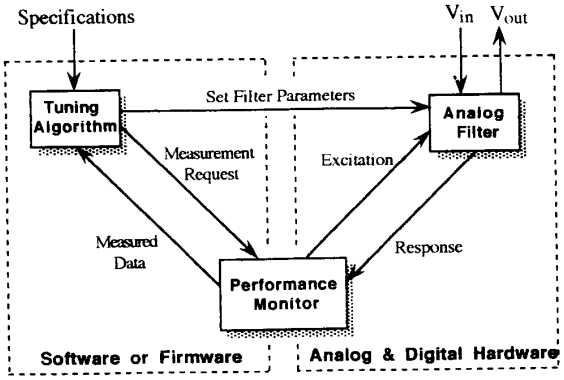

Fig. 1. Block diagram of the digital tuning strategy used in this architecture.

The functional blocks are physically, as well as functionally, distinct. A software or firmware program containing the tuning algorithm and higher-level functions of the performance monitor runs on a microcomputer or microprocessor. This program communicates with the filter and measurement circuitry that may or may not be integrated on the same substrate.

2.1 CONTINUOUS-TIME FILTER

The analog filter illustrated in Fig. 2, described mathematically in Eq. (1), and presented in detail in [6, 7] is robust and flexible with independent, continuous control mechanisms. The filter is designed to be reconfigured to support various 2nd-order transfer functions. Multiple independent control mechanisms provide a wide adjustment range without sacrificing resolution. The control mechanisms are overlapping for continuous control and exhibit monotonic control relationships that provide stability for the tuning algo-

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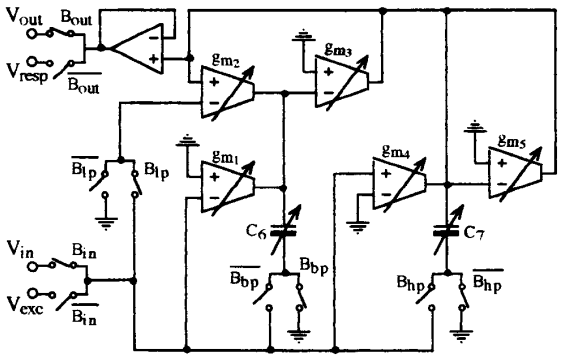

Fig. 2. Circuit schematic of a reconfigurable, fully-programmable, 2nd-order biquadratic filter.

tuning strategy insensitive to prevailing problems found in existing technologies—imprecision in the control mechanisms and nonideal cross-couplings between controlled filter parameters and "independent" control mechanisms. The analog filter in this architecture exhibits cross-couplings, as shown in Fig. 3, but these unintentional relationships do not interfere with the overall performance of the filter since over-ordering effects that distort the filter's frequency response can be minimized by the tuning algorithm. Imprecision is also not of major concern because the tuning algorithm compensates for parasitic mismatch. By reducing the design constraints of imprecision and over-ordering effects, this architecture allows the control range to be extended significantly and resolution to be greatly increased.

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{(B_{hp})\,s^2 + \left(\frac{g_{m4} - g_{m3}\,B_{bp}}{C_7}\right)s + \left(\frac{g_{m1}\,g_{m3} + g_{m2}\,g_{m3}\,B_{lp}}{C_6\,C_7}\right)}{s^2 + \left(\frac{g_{m5}}{C_7}\right)s + \left(\frac{g_{m2}\,g_{m3}}{C_6\,C_7}\right)} \quad (1)$$

The components that determine the configuration and response of the filter are shown in Fig. 2. Switches B_{lp}, B_{bp} and B_{hp} allow selection of the transfer function that defines the 2nd-order filter structure, and switches B_{in} and B_{out} allow the filter to be shared between the user's application and the performance monitor. The parallel array of integrating capacitors (C_6 and C_7) and the parallel

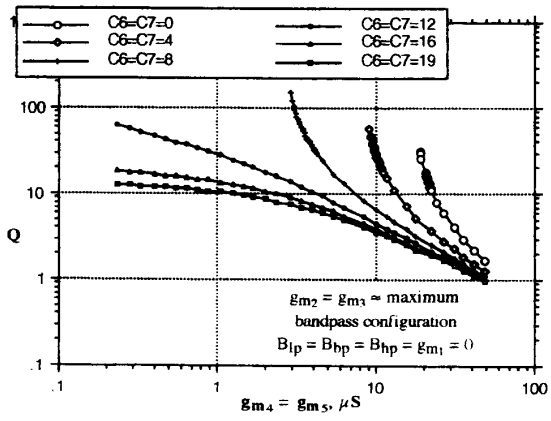

Fig. 3. Example of cross-coupling in a bandpass filter where adjusting the f_o of the filter by varying the capacitance of C_6 and C_7 indirectly affects the filter Q. Ideally, the curves showing the filter Q response to variation in the Q control mechanisms g_{m4} and g_{m5} should be identical regardless of the capacitor's setting.

array of current-mirror output stages internal to the OTAs (g_ms) are digitally switched to give independent coarse control. Independent fine control is achieved by adjusting the bias current of each OTA over a small range through the use of D/A converters.

2.2 Performance Monitor

The performance monitor increases the efficiency of the architecture by minimizing the number of gain/frequency measurements required for a single characterization and by reducing the accuracy requirements of the digitally controlled oscillator and data acquisition system.

A filter characterization algorithm and a gain measurement algorithm make up the performance monitor as shown in Fig. 4. The filter characterization algorithm extracts parametric data by applying modern heuristic numerical analysis routines that first bracket and search for a given feature (e.g. a 3dB point or peak). Secondly, a least-squares curve is fitted to data in the region surrounding the feature, thereby increasing the overall accuracy of the chacterization. The accuracy can be further enhanced by collecting a few additional coordinates. With each iteration of the algorithm, a sampling frequency is computed from previous results and then physically generated by an excitation system under the direction of the gain measurement algorithm. Assuming that the frequency control mechanism is monotonic, some inaccuracy in the frequency selection is tolerated since the characterization algorithm is heuristic. The excitation system consists of a digitally controlled oscillator that generates the excitation frequency and inputs it to the filter and a digital frequency counter that accurately measures the excitation frequency. The gain response of the filter at the excitation frequency is estimated by utilizing the A/D converter internal to the data acquisition system to collect voltage samples of the excitation and response sinusoids at equal time intervals and to analyze them using expected-value probability theory as detailed in Eq. (2).

$$\mathrm{rms}(V_x) = \sqrt{\underset{1 \le i \le n}{E}\left\{[V_x(t_i)]^2\right\} - \left[\underset{1 \le i \le n}{E}\left\{V_x(t_i)\right\}\right]^2} \quad (2a)$$

$$\mathrm{gain} = \frac{\mathrm{rms}(V_{resp})}{\mathrm{rms}(V_{exc})} \quad (2b)$$

In this equation, $V_{exc}(t_i)$ and $V_{resp}(t_i)$ correspond to equally-spaced time-domain samples of the excitation and response waveforms, respectively. This estimation theory averages out inaccuracies in the A/D converters, thereby increasing the overall accuracy of the gain measurements without increasing system cost.

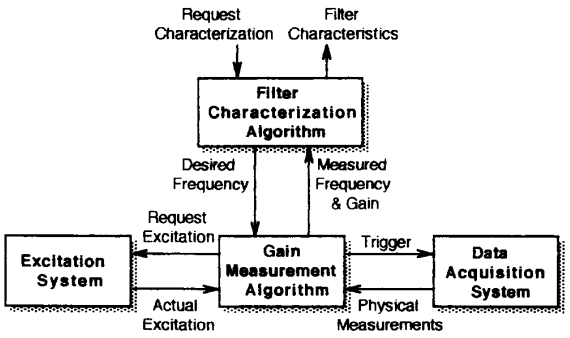

Fig. 4. Block diagram of the performance monitor.

Fig. 5 is an example of the filter characterization algorithm extracting the peak gain, peak frequency and the two 3dB frequencies of a bandpass filter response. This particular characterization required collection of 22 frequency/gain measurements around the key features of the frequency response and application of polynomial and linear least-squares curve fits to accurately identify these features.

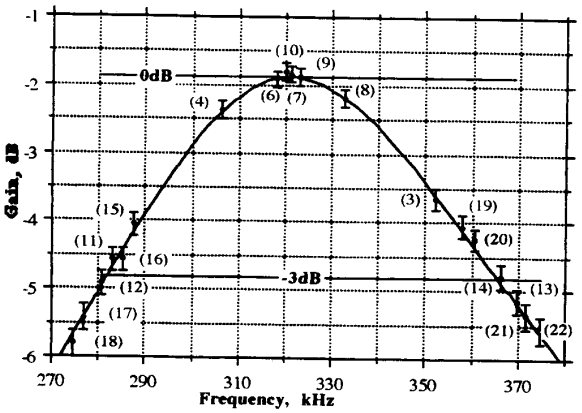

Fig. 5. Numbered points on this frequency response of a simulated filter indicate the order of sampling by the filter characterization algorithm. Gain measurement tolerance is indicated by vertical error bars.

2.3 TUNING ALGORITHM

The tuning algorithm, summarized in Fig. 6, repeatedly models and adjusts each of the control mechanisms, monitoring the effects that these changes have on each filter parameter in a progressive attempt to achieve the desired filter response.

```
compute initial filter realization & program initial filter
tune filter...
    repeat
        measure the filter's current characteristics
        tune the necessary components...
            repeat
                develop new control models
                compute new filter settings via extrapolation
                analyze & prioritize the current tuning needs
            until no models switch from coarse to fine
        update filter settings according to the tuning needs
    until tuned
check tune...
    ultra-fine tune each filter parameter, if necessary
```

Fig. 6. Pseudo-code representing the basic tuning algorithm.

A control model is developed that maps each digital control word to all of the filter parameters. Generally, these relationships are nonlinear, a mathematically intractable state that is remedied by predistorting the digital control words to more readily-modelled linear control mechanisms. The model begins as a linear system passing through a single data point and is developed by varying a single control mechanism at a time and fitting a least-squares curve through the resulting additional data points. With each iteration of the algorithm the model becomes increasingly accurate with the potential to reach a 2nd-order system.

Several models are developed in this fashion in an order that is determined by the algorithm at each iteration. The model or models with the fewest cross-couplings are selected to be applied in the next iteration, thereby determining the next data point to be collected. Once the models become linear, application of all models occurs simultaneously. Convergence is reached when all models reach a certain level of maturity, and the models converge upon a single solution. Verification of the solution is accomplished by making slight adjustments to each control word in the filter to check the accuracy of the tune. Further fine adjustments are then made, if necessary.

The efficiency of this algorithm is significantly enhanced by carefully prioritizing the order in which the control mechanisms are adjusted to minimize the parasitic cross-coupling effects discussed above. Fig. 3 shows that adjusting the capacitance value of the capacitor array inadvertently alters the position of a parasitic zero, thereby modifying the Q of the filter and the slope of the Q control model as a function of g_{m_4} and g_{m_5}. These adverse cross-coupling effects are circumvented and the convergence of the tuning algorithm is enhanced by simply adjusting the capacitor array first.

This tuning algorithm is quite efficient. For example, a six control mechanism, three parameter filter is accurately tuned by 15 to 20 iterations, typically. This includes one iteration per control mechanism—coarse and fine—to develop a rudimental model, two to four iterations to refine the model, two to three iterations to tune the filter, and one iteration per controlled filter parameter to verify the accuracy of the tune.

4. EXPERIMENTAL RESULTS

This system is implemented with a single custom analog IC, a rack of instrumentation and an IBM compatible PC. The filter is integrated into a 3μm CMOS p-well process with dual high frequency sample-and-holds used in conjunction with the data acquisition system. The tuning algorithm and higher-level functions of the performance monitor are implemented in Pascal on an IBM PC that communicates with other instrumentation through an HP-IB bus. The digitally controlled oscillator and frequency counter are prototyped with commercially available instrumentation. The A/D is implemented with an hp5180A Waveform Recorder which has a 10-bit resolution and approximately 8.5-bits of accuracy. This implementation is limited to characterization and tuning of 2nd-order bandpass filter responses.

The basic filter design provides a typical resolution of 0.5% over an adjustment range in excess of 3 decades. This design uses ±5V supplies and operates on signals not exceeding $2V_{p\text{-}p}$. The filter uses a 6-bit logarithmic D/A to finely adjust the g_m control mechanism over a 1 to 1.85 range. The current-mirror output stage has a 6-bit resolution, spanning a 2-decade control range. An additional decade of adjustment is provided by a 20-element capacitor array. Experimental characterization of the filter's control mechanisms are summarized in Table 1. In high-frequency high-Q operation, the filter exhibits a sensitivity to Q-enhancement which reduces the resolution of the Q and peak gain controls, and in extreme cases produces gaps in the control range and causes the filter to jump res-

onate. Furthermore, Q-enhancement increased the sensitivity of the filter's frequency response to amplitude dependencies which can be characterized as a shift in the filter parameters as the signal amplitude is increased.

Table 1. Summary of experimental performance of the filter's control range and resolution.

Parameter	Range	Resolution
f_{peak}	2kHz ≤ f_{peak} ≤ 2MHz	0.25%
Q	less than 0.1 ≤ Q < ∞	≥0.5%
H_{peak}	-45dB ≤ H_{peak} ≤ 45dB	≥0.025dB

The excitation system has the capability of setting and measuring frequencies ranging from 1Hz to 20MHz, maintaining accuracies of less than 0.1% over this entire range. The basic data acquisition system has a -50dB SNR, which yields accuracies of 0.025dB per voltage sample. This system collects 1024 voltage samples per rms measurement, obtaining gain accuracies as high as 0.01dB or more. The overall accuracy of the gain measurement system is limited by the timing jitter associated with sampling the sinusoidal waveforms. This system has the capability of detecting filter oscillation and jump resonances.

The performance monitor is designed to accurately determine the peak gain, peak frequency and the two 3dB points via a combination of modern numerical analysis techniques—golden bisection, golden uphill step, parabolic interpolation based on Brent's method and the Van Wijngaarden-Dekker-Brent's method [8]. Using least-squares curve fitting techniques improved the accuracy of the extraction by a factor of 3 and enhanced the reliability of the system. Based on 100,000 peak gain extractions on a simulated gain measurement system with only a 0.1dB accuracy, only 18 cases locked on a peak outside of a 0.2dB window. Reliabilities are expected to be much higher on the 0.01dB accurate gain measurement system characterized above.

The tuning algorithm was tested over a wide range of filter specifications. In each case, the filter was tuned in 15 to 20 iterations to an accuracy limited either by the resolution of the filter or the accuracy of the performance monitor. A few of these case studies are summarized in Table 2. In general, the tuning algorithm operated well in control regions containing considerable cross-coupling effects, though in extreme situations producing gaps in the control region, the algorithm had difficulties tuning. Lastly, the algorithm does not have the capability of avoiding control regions producing jump resonance problems or oscillations.

Table 2. Characteristic experimental results of the tuning algorithm based on measurements taken by the performance monitor.

Filter Parameter	Test Description	Low Frequency	Medium Frequency	High Frequency
f_{peak} (Hz)	Specification	63,096	398,107	1,000,000
	Initial Value	74,083	477,928	933,160
	After Tuning	62,986	398,052	1,000,103
	Accuracy	-0.174%	-0.014%	+0.010%
Q	Specification	10.000	25.119	10.000
	Initial Value	8.739	15.150	19.122
	After Tuning	10.024	25.180	10.029
	Accuracy	+0.240%	+0.243%	+0.290%
H_{peak} (dB)	Specification	0.000	0.00	0.00
	Initial Value	-2.488	-2.50	4.00
	After Tuning	0.004	0.04	0.00
	Accuracy	+0.046%	+0.46%	+0.00%
	Iterations	18	14	15

5. CONCLUSIONS

An architecture is presented of a digitally programmable CMOS OTA-C analog filter which is controlled, characterized and tuned by a microprocessor in the field. Two elements of this architecture, the highly accurate performance measurement system and the tuning algorithm, were discussed in detail. Experimental results show that this versatile architecture is suitable for high-accuracy, high-frequency continuous-time filtering applications, as well as those requiring in-field self tests or in-field programming. Furthermore because the tuning algorithm and the higher-level operations of the performance monitor are implemented in a highly-flexible software/firmware, this system can be extended to meet the diverse needs of a particular application, and address such problems as reducing over-ordering effects by performing pole/zero cancellation in a similar manner as a vector-lock loop system.

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