A CMOS Transconductance–C Integrator Structure with Wide-Band Programmabilty and Phase Lead/Lag Compensations

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Abstract

The design of a digitally programmable transconductance amplifier (TA) suitable for high-frequency signal processing is presented. The circuit uses switchable differential transconductance elements and a differential folded cascode output stage. An integrator structure based upon this fully differential TA is proposed to serve as the basic building block of programmable continuous-time filters. The structure employs compensation scheme which provides phase error correction at unity gain frequencies throughout its adjustment range. Limitation on practical filter applications of this structure has also been addressed. Simulation shows that the unity gain frequency of this integrator structure can be programmed between 200KHz and 20MHz with $3pF$ load. The transconductance gain of a prototype transconductance amplifier fabricated in a $2\mu m$ CMOS process is experimentally adjusted and measured from $3\mu A/V$ to $1.3mA/V$.

Introduction

In the past decade, monolithic transconductance amplifiers–capacitors (TAC) filters have been subjects of considerable research because their potential for viable high-frequency signal processing [1][2]. Attempts have also been made to realize digitally programmable TAC filters which can be used in wide-band, reconfigurable applications [3]. Previous implementation of the programmable transconductance amplifier (PTA) as presented in [3] was based upon the switchable–mirror structure which suffers from limited operating speed and a digitally dependent output resistance. Tuning such filters is thus dependent upon sophisticated mathematical computations, and the tuning accuracy and performance is plagued by uncharacterized and uncontrollable phase errors. In this paper, a new programmable TAC integrator structure is proposed which can serve as the basic building block of wide-band, reconfigurable digitally programmable TAC filters. The structure is based upon a fully-differential folded cascode transconductance amplifier and is made programmable by switching the simple differential pair input stages. Besides the adjustable unity gain frequency, the integrator is facilitated with extra adjustable components to compensate the leading or lagging phase errors occurring at lower and higher unity gain frequencies, respectively. Simulation results show that the unity gain frequency of this integrator structure can be programmed to achieve more than two decades of adjustment range with reasonable dynamic range. It is believed that, with appropriate analog and/or digital tuning schemes, the new structure can provide a viable solution for digitally programmable, wide-band and reconfigurable signal processing applications.

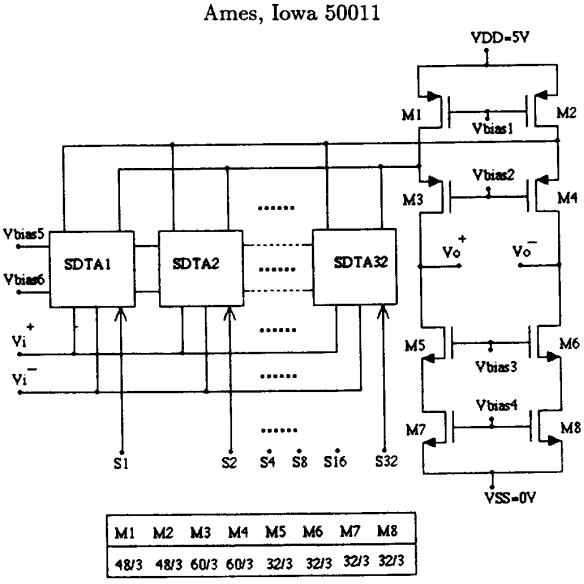

Fig.1 The Switchable Transconductance Amplifier Structure

Basic Programmable Transconductance Amplifier Structure

Fig.1 shows the schematic diagram of a digitally programmable transconductance amplifier (TA) structure. The TA consists of six parallel, switchable differential transconductance amplifiers (SDTA) directly coupled to a folded-cascode output stage. With this structure, improvements in speed as well as output impedance can be achieved. The SDTA, as shown in Fig.2, can be either turned on/off by the switching signal S or fine-tuned through biasing voltages. When the SDTA is to be turned on, transistors M7 and M9 are used to deliver the biasing voltages. On the other hand, the SDTE can be turned off by cutting off transistors M3–M5 through M8 and M10; while M6 is used to prevent node A from floating and thus to keep M1 and M2 in their cutoff region. Sizings of the six SDTAs are bi-

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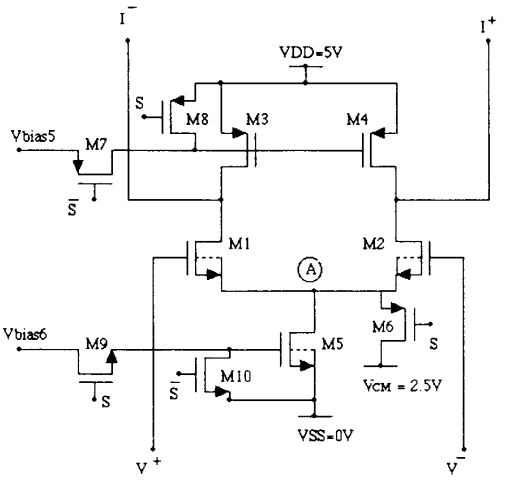

	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
SDTA32	96/6	96/6	96/3	96/3	128/3	6/2	6/2	6/2	6/2	6/2
SDTA16	48/6	48/6	48/3	48/3	64/3	6/2	6/2	6/2	6/2	6/2
SDTA8	24/6	24/6	24/3	24/3	32/3	6/2	6/2	6/2	6/2	6/2
SDTA4	12/6	12/6	12/3	12/3	16/3	6/2	6/2	6/2	6/2	6/2
SDTA2	6/6	6/6	6/3	6/3	8/3	6/2	6/2	6/2	6/2	6/2
SDTA1	3/6	3/6	3/3	3/3	4/3	6/2	6/2	6/2	6/2	6/2

Fig.2 Schematics of the Switchable Differential Transconductance Amplifier

narily weighted such that the total transconductance gain can be programmed in 2 decades. All SDTAs are biased with the same voltages so as to maintain the same input linear range for all SDTAs.

The complete schematics for generating biasing voltages including the common-mode feedback (CMFB) stabilizing biasing are given in Fig.3. The biasing circuitry of the SDTAs is designed to be independent from that of the folded-cascode output stage. The extra freedom of biasing provides a means to adjust the output resistance, or equivalently, the open-loop gain of the TA. The reason why such adjustability is provided will be discussed later in this paper. With the CMFB circuit, the output dc voltages V_o^+ and V_o^- can be stabilized to approximately V_{cm} such that the output signal has ample linear swinging range.

Characteristics of TAC-based Integrators

An ideal TAC integrator has the transfer function given by

$$\frac{v_o}{v_i} = \frac{g_m}{sC} \tag{1}$$

where g_m and C are the transconductance and load capacitance of the trasconductance amplifier, respectively. The following parameters of the ideal integrator can thus be obtained:

$$\omega_u = \frac{g_m}{C} \tag{2}$$

and

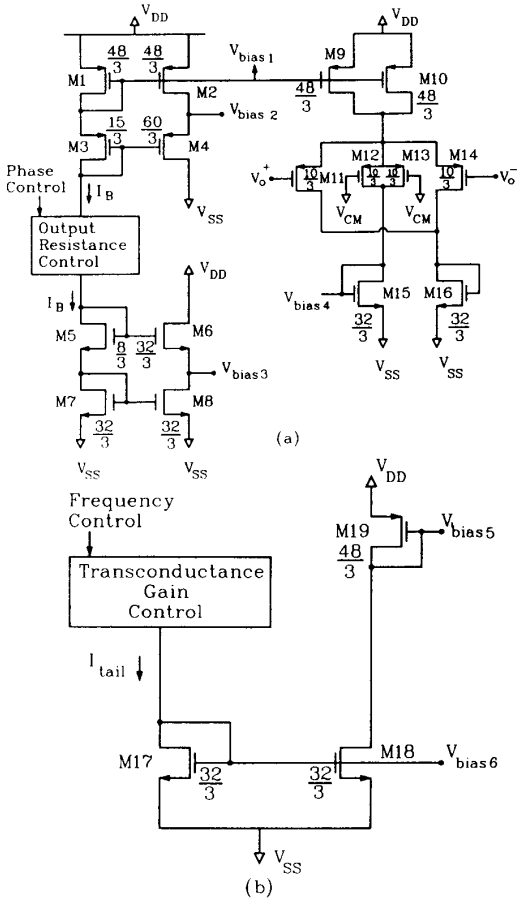

Fig.3 Biasing and Common-Mode Feedback Circuits for the Transconductance Amplifier a)Output Stage Biasing Circuit b)SDTA Biasing Circuit

$$\phi(\omega) = -\frac{\pi}{2} \tag{3}$$

for all frequencies, where ω_u and ϕ are the unity gain frequency and the phase of the integrator, respectively. In a real integrator, the finite output resistance and internal parasitic poles cause phase and gain errors. In Fig.4, an equivalent integrator circuit including these nonidealities is modeled by an effective internal parasitic pole, a finite output resistance, a parasitic output capacitance, and a load capacitor in series with a compensating resistor. In the case of $R_c = 0$, the integrator transfer function is given by

$$\frac{v_o}{v_i} = \frac{g_m R_o}{(1 + sR_o(C_L + C_{p2}))} \frac{1}{(1 + sR_{p1}C_{p1})} \tag{4}$$

According to (4), at lower frequencies, finite output resistance introduces a leading phase. On the other hand, the effective parasitic pole will cause a lagging phase at higher frequencies.

A common scheme to compensate the integrator lagging phase at higher frequencies is to use a series resistor

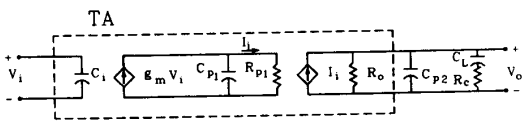

Fig.4 Linear Macromodel of Nonideal TAC Integrator

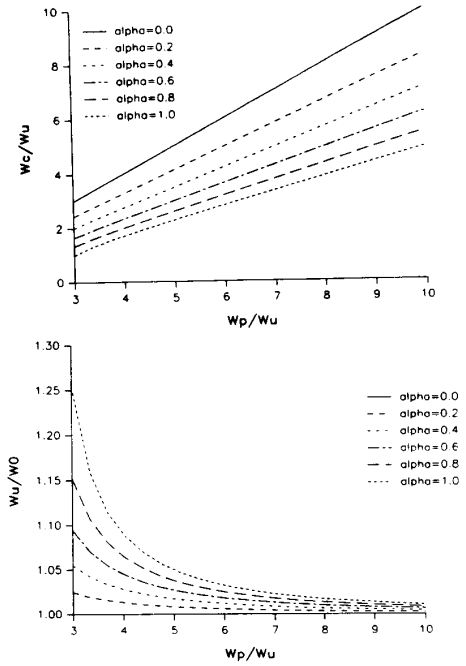

Fig.5 Nonideal Compensation Effects due to Parasitic Load Capacitance a) Effects on the Compensating Zero ω_c b) Effects on the Unity Gain Frequency ω_u

R_c in Fig.4 to create an extra zero to cancel the effect of parasitic poles[4]. If $R_c << R_o$, the integrator transfer function can be approximated by

$$\frac{v_o}{v_i} = \frac{g_m R_o}{(1+sR_o(C_L+C_{p2}))} \frac{1}{(1+sR_{p1}C_{p1})} \frac{(1+sR_cC_L)}{(1+sR_c(\frac{C_LC_{p2}}{C_L+C_{p2}}))} \quad (5)$$

It can be observed in (5) that another pole at $\frac{1}{R_c(\frac{C_LC_{p2}}{C_L+C_{p2}})}$ is introduced by this compensating scheme. This new parasitic pole is usually insignificant as long as C_L is relatively large comparing to C_{p2}. Now if we define α to be the ratio of the parasitic load capacitance to the load capacitor, i.e., $C_{p2} = \alpha C_L$, then (5) can be rewritten as

$$\frac{v_o}{v_i} = \frac{g_m R_o}{(1+sR_oC_L(1+\alpha))} \frac{1}{(1+sR_{p1}C_{p1})} \frac{(1+sR_cC_L)}{(1+sR_cC_L(\frac{\alpha}{1+\alpha}))} \quad (6)$$

As α increases, the new parasitic pole becomes more and more significant. The compensating zero, ω_c, can thus be determined to cancel the phase error at unity gain frequency by solving the nonlinear equation derived from (6)

$$tan^{-1}\frac{\omega_u}{\omega_c} - tan^{-1}\frac{\omega_u}{\omega_p} - tan^{-1}\frac{\omega_u}{\omega_c}\frac{\alpha}{1+\alpha} = 0 \quad (7)$$

where $\omega_c = 1/R_cC_L$, $\omega_p = 1/R_{p1}C_{p1}$, and the finite gain effect is neglected at high frequencies. The effects of α can be best illustrated by the nonlinear equation solutions as obtained in Fig.5. Fig.5(a) shows that ω_c approaches closer to the unity gain frequency as α increases. Analysis shows that when α exceeds certain critical value with a particular ω_p, there can be no solution for ω_c. Another observation is that the integrator frequency response can be also deteriorated due to the α effect. As shown in Fig.5(b), the unity gain frequency deviates from the nominal value given by $\frac{g_m}{(1+\alpha)C_L}$. The frequency response distortion at high frequencies can thus limit the accuracy of the TAC filters if only analog automatic tuning loop(s) is(are) applied since the filters carry severe over-ordering effects.

To correct the low-frequency leading phase errors, an effective approach is to adjust the output resistance R_o of the TA such that the open loop gain can be increased and the 3dB rolloff frequency can be pushed to a lower frequency. The biasing circuitry in Fig.3(a) is thus useful to achieve this phase-correcting scheme.

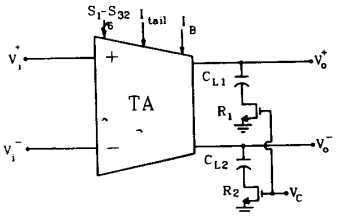

Fig.6 Schematics of the proposed TAC Integrator

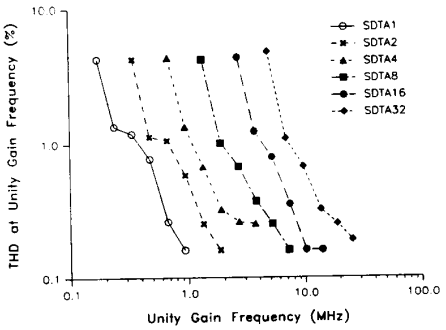

Fig.7 SPICE Simulated Frequency Adjustment Domain and Associated Total Harmonic Distortions of the TAC Integrator

Simulation Results

The schematics of the fully differential TAC integrator structure consisting of the previously described TA, two $3pF$ fixed load capacitors and the associated series voltage controlled MOS resistors for phase compensation are given

in Fig.6. SPICE simulation shows that, using MOSIS $2\mu m$ parameters, the dominant high-frequency pole, ω_p, of this integrator is approximately 150MHz, and that the input capacitance can be as high as $0.3pF$.

The programmability of the TAC integrator has been functionally verified through extensive SPICE simulations. The unity gain frequency adjustment domain and the associated total harmonic distortions are shown in Fig.7. The results show that the unity gain frequency can be programmed between $157KHz$ and $24MHz$ with $3pF$ loads on both output nodes. It can be seen that continuous adjustments of the unity gain frequency can be achieved with capability of handling modest amplitude signals ($0.5V_{p-p}$) over the entire adjustment range.

Experimental Results

The PTA structure has been fabricated by the MOSIS $2\mu m$ CMOS P-WELL process. The dc short-circuit transconductance gains have been experimentally measured. The full-range programmability of the PTA is given in Fig.8 in which the results show seven separative segements corresponding to different digital settings. It is observed that the transconductance of the PTA structure is adjustable from $3\mu A/V$ to $1.3mA/V$. The Power Supply Rejection Ratios (PSRR) have been measured at 57dB with respect to V_{DD} and 81dB with respect to V_{SS}. The Common-Mode Rejection Ratio (CMRR) has been measured at 53dB. Note that both PSRR and CMRR measurements were measured by setting only S_{32} on and setting $I_{tail} = I_B = 160\mu A$. The open circuit dc gain of the PTA with such settings is measured at 110 or 40.8dB. The summarized measured results on the total harmonic distortions (THD) are given in Table 1. Due to severe mismatches, the THD performance of the PTA is observed somewhat worse than expected, as shown in Fig.8.

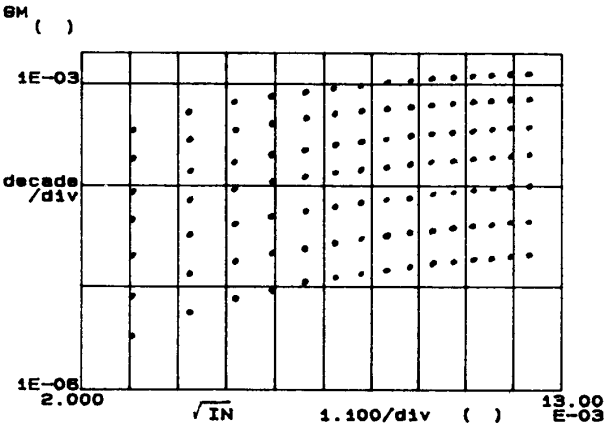

Fig.8 The experimental results demonstrating the full range programmability of the short-circuit transconductance gains of the PTA

Active Stage(s)	Signal Swing V_{pp} at 1% THD
S_1	0.435
S_2	0.46
S_4	0.485
S_8	0.5
S_{16}	0.5
S_{32}	0.5
All Stages	0.35

$^*I_{tail} = 72\mu A \quad I_B = 128\mu A$

Table 1 The measured 10KHz-sinusoidal input amplitudes at 1% THD.

Conclusions

A new programmable TAC integrator structure which is designed for high-frequency, wide-band and reconfigurable signal processing applications has been presented. The CMOS integratable structure exploits a compensation resistor to create an zero to correct excess phase at its unity gain frequency. An extra freedom of adjusting output resistance of the transcoductance amplifier is given to allow an alternative phase correction scheme. Simulation results have shown that the unity gain frequency can be adjusted over a 2-decade range. The accuracy limitation of the proposed integrator structure applied to filter synthesization has also been addressed. Experimental results measured from the CMOS prototype implementation show the functionality as well as wide-range programmability of the transconductance amplifier. Further improvement on its linearity can be achieved by designing the differential input stages with readily available linearization techniques.

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