A Versatile Digitally Controlled Continuous-Time Filter Structure with Wide-Range and Fine Resolution Capability

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Abstract—**A digitally programmable and reconfigurable filter structure is presented. The design is based on a versatile continuous-time biquadratic block realized by means of digitally controllable transconductance amplifiers and programmable capacitor arrays. A specific implementation, integrated in a 3-μm p-well CMOS process, which is capable of synthesizing a large number of even-ordered transfer functions of up to sixth-order with complete control of all pole-pairs and zero-pairs is discussed. The programmable filter exhibits typical pole and zero resonant frequency resolution of $\pm 0.25\%$ and typical bandwidth resolution of $\pm 0.5\%$ over the three-decade adjustable range from 1 kHz to 1 MHz and features typical dynamic range of 60 dB.**

I. Introduction

CONTINUOUS-time signal processing is required in many signal processing applications. Although implementations can be achieved with either continuous-time or sampled-data architectures, continuous-time approaches are capable of operating at higher frequencies than the sampled-data counterparts, such as switched-capacitor and digital filtering approaches. Besides high-frequency filtering, many broadband applications also exist where absolute accuracy as well as reconfigurability to widely different transfer functions are crucial for the viability of the system.

Throughout the past several decades, the theory of continuous-time filters has become well developed. Continuous-time filter implementations, however, usually suffer from degraded performance due to inaccurate realization of the filter components. The development of viable monolithic continuous-time filters has been slowed by the unavailability of good practical resistors and large capacitors. Accuracy issues are even more problematic for monolithic continuous-time filters [1]–[4] since the filter precision is particularly difficult to control due to large inherent process variations and the presence of large and uncontrollable parasitic components. Existing MOS continuous-time structures that are programmable over a wide adjustment range also suffer from significant dynamic range degradation with the adjustable parameters and fully reconfigurable continuous-time structures are essentially nonexistent.

In this paper, a digitally programmable continuous-time filter structure, which provides a very wide adjustment range, fine adjustability, and complete reconfigurability, is introduced. The architecture of the filter and the corresponding building blocks are presented in Section II. The design and implementation of the specific programmable filter structure that can realize user-selectable even-order transfer functions up to sixth order is described in Section III. Experimental results measured from this specific implementation are discussed in Section IV.

II. Filter Architecture

The basic filter architecture is shown in Fig. 1. The system consists of an analog bus, a digital bus, a local digital controller, a performance monitor and a number of digitally programmable biquadratic sections. The analog bus delivers system input and output signals in analog form. Output signals from any biquad are routed to the system analog bus while the input signals to any biquad are obtained from the analog bus. The local digital controller serves as an analog bus controller and allows for arbitrary interconnection of the biquads and the system input and output lines. Each biquadratic section can be programmed via the digital bus to implement arbitrary second-order filters. The local digital controller is also used to configure each biquadratic block as well as control the analog bus connections. The digital bus can communicate with an external host to implement field-programmable user applications. By properly configuring and connecting the biquads, the filter structure can effectively realize arbitrary even-ordered transfer functions.

To achieve high-precision signal processing, some form of self-correcting or tuning must be provided. In this architecture, tuning can be achieved either by equipping the local digital controller with sufficient tuning intelligence or by performing tuning algorithms from an external tuning con-

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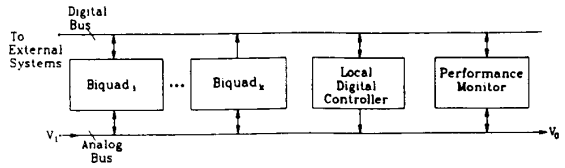


Fig. 1. The programmable continuous-time filter architecture.

troller. The tuning algorithm, based upon an understanding of the inherent control relationships of the filter structure, is used to iteratively tune the filter characteristics (e.g., pole resonant frequency and pole Q) to a user-supplied specification. The performance monitor block in Fig. 1, in response to requests by the tuning algorithm, characterizes the response of the filter.

Conventional analog tuning loop techniques [5] that have been exploited in most other precision monolithic continuous-time filters, such as phase-locked loop and vector-locked loop strategies, are not used in our filter structure. In general, researchers have been quite successful in using analog tuning for moderate-precision filters that are designed to implement a specific transfer function. Practical extensions of analog tuning loops to programmable and/or reconfigurable structures have not evolved, nor have analog tuning loops for very high-precision applications. Analog tuning is plagued, in part, by the inherent limited accuracy in the tuning circuit itself. In addition, for those tuning strategies based on the master–slave structure, which has been a major research focus in recent years, precision is further limited by mismatches between the master and slave circuits.

III. Specific Filter Implementation

Filter structures based upon transconductance amplifiers and capacitors (TAC) filters, noted for both high frequency performance and programmability, are amenable for integration in existing monolithic processes. In this section, a CMOS monolithic implementation of the digitally controlled continuous-time filter is described. The filter, depicted in block diagram form in Fig. 2, consists of three TAC-based digitally programmable biquadratic blocks that can be used to synthesize even-order functions up to sixth order. All biquads use V_{bias} to bias cascode transistors of the bias current sources in the input stage of the transconductance amplifiers. V_{ref}^{+} and V_{ref}^{-} together provide reference voltages for digital-analog converters that are used for fine adjustments of the tail current of the differential input stage of the transconductance amplifier. Each biquad is addressable by the local controller. The local controller can be used to adjust all of the filter parameters in the biquads by storing desired programming words placed on the data bus on a digital latch internal to the biquads. A second digital latch in each biquad is also addressable by the local controller through the system bus and is used to reconfigure the biquads. The analog switch latch governs the analog bus and is driven over the system bus by the local controller. The operation of this filter structure can be classified into two phases. In the "tuning" phase, the excitation and response signals V_{exc} and V_{resp} are generated and monitored, respectively, by the externally connected performance monitoring system (PMS). The V_{in} and V_{out} lines, on the other hand, serve as the input and output, respectively, in the "signal processing" phase. The analog bus connections and the biquad configurations are controlled by the local controller which, in the present implementation, predecodes commands from an external tuning host. Alternatively, with the appropriate control algorithm, the structure either serves as an adaptive filter, or as one in which the PMS tunes the system in the presence of an input signal.

A. Biquadratic Structure

The digitally controlled TAC filter biquadratic building blocks denoted as biquads 1–3 in Fig. 2 is shown in Fig. 3. Each consists of five programmable transconductance amplifiers (TA's), two programmable capacitor arrays (PCA's), an analog buffer stage, and several analog configuration switches. The transfer function of this circuit is given by

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{(B_{hp})s^2 + \left(\frac{g_{m4} - g_{m3}B_{bp}}{C_7}\right)s + \left(\frac{g_{m1}g_{m3} + g_{m2}g_{m3}B_{lp}}{C_6C_7}\right)}{s^2 + \left(\frac{g_{m5}}{C_7}\right)s + \frac{g_{m2}g_{m3}}{C_6C_7}} \tag{1}$$

where the Boolean variables B_{hp}, B_{bp}, and B_{lp} can take on the value of 0 or 1, depending on whether the corresponding analog switch is open or closed. From (1), the following definitions of biquadratic filter parameters are made:

$$\omega_p = \sqrt{\frac{g_{m2}g_{m3}}{C_6C_7}} \tag{2}$$

$$BW_p = \frac{g_{m5}}{C_7} \tag{3}$$

$$\omega_z = \sqrt{\frac{g_{m1}g_{m3} + g_{m2}g_{m3}B_{lp}}{C_6C_7}} \tag{4}$$

$$BW_z = \frac{g_{m4} - g_{m3}B_{bp}}{C_7} \tag{5}$$

where ω_p is the pole resonant frequency, BW_p is the pole bandwidth, ω_z is the zero resonant frequency, and BW_z is the zero bandwidth. By properly setting configurations on the digital bus, as shown in Table I, the biquad structure can effectively realize arbitrary second-order filter functions including bandpass, high-pass, low-pass, and notch filters, etc. From (2)–(5) it can be seen that the fundamental filter parameters, specifically, the resonant frequencies and bandwidths (alternatively the quality factors or Q values), can be

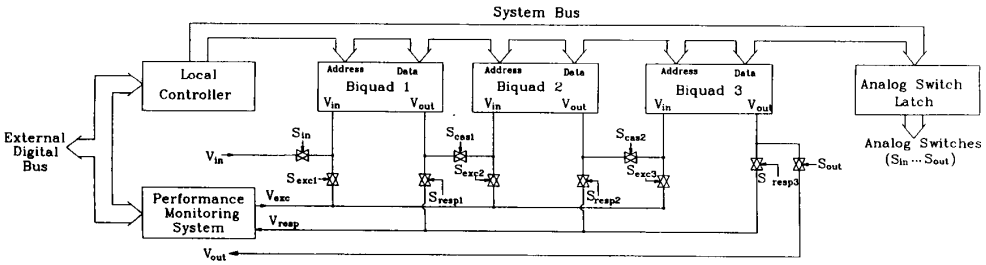


Fig. 2. A specific implementation of the digitally programmable continuous-time filter structure.

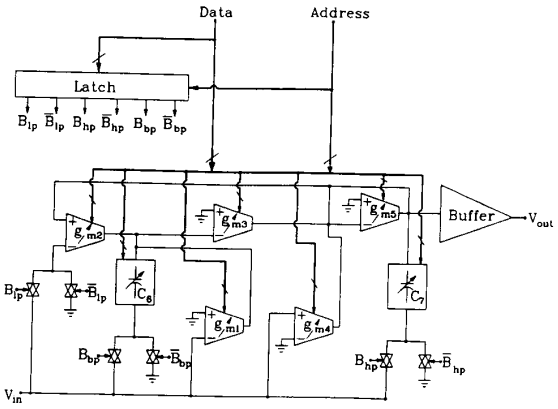


Fig. 3. A TAC-based biquadratic building block.

TABLE I
MEMORY MAP FOR SECOND-ORDER FILTER CONFIGURATIONS

	B_{hp}	B_{bp}	B_{lp}	Special Conditions
High-pass	1	0	0	$g_{m1} = g_{m4} = 0$
Band-pass	0	0 or 1	0	$g_{m1} = 0$
Low-pass	0	0	0 or 1	$g_{m4} = 0$
All-pass	1	1	1	$g_{m1} = g_{m4} = 0$ $g_{m3} = g_{m5}$
Low-pass notch	1	0	1	$g_{m4} = 0$ $g_{m1} > g_{m2}$
High-pass notch	1	0	0	$g_{m4} = 0$ $g_{m1} < g_{m2}$

sequentially or independently and arbitrarily determined. For example, g_{m2} and g_{m3} can be used to independently control the pole and zero resonant frequencies without changing bandwidths, while g_{m4} and g_{m5} can be adjusted to change bandwidths with fixed resonant frequencies.

B. The Programmable Transconductance Amplifier

The programmable transconductance amplifier (PTA), as the basic active building block of the TAC filters, should maintain good linearity over a wide adjustment range. Since a wide-range adjustable filter usually implies operating at different frequencies, the TA must have satisfactory frequency response over the entire g_m-adjustment frequency range. The PTA should also maintain fine resolution over the entire g_m adjustment range.

A single-ended output PTA structure is shown in the block diagram of Fig. 4 and is comprised of an embedded TA, a logarithmic digital-to-analog converter (DAC) used for tail current adjustment in the embedded TA with V_{tail}, and a decoder used to configure the output mirrors of the embedded TA. The embedded TA, shown in Fig. 5, is comprised of a differential transconductance stage and three current mirrors of which two (CM1 and CM3) are digitally programmable. The overall transconductance gain is given by

$$g_m = \frac{I_0}{V_2 - V_1} = g_{md}M \tag{6}$$

where g_{md} is the transconductance of the differential stage

$$g_{md} = \frac{I_1 - I_2}{V_2 - V_1} \tag{7}$$

and where M is the gain for the current mirrors given by

$$M = \frac{I_0}{I_1 - I_2} = M_1 = M_2 M_3 \tag{8}$$

where it is assumed that the product of the mirror gains $M_2 M_3$ is equal to M_1. The transconductance gain can be adjusted either by adjusting V_{tail} on the transconductance elements through the DAC or by digitally changing the output current mirror gains as depicted in Fig. 4. With this structure, V_{tail} will be used for smaller (fine) adjustment while the switchable mirrors will be used for more significant (coarse) adjustment. This transconductance adjustment scheme has been adopted to provide better linearity, better frequency response, and better dynamic range, for a wide range of operation, than is achievable with conventional tail current-controlled TA structures. A complete circuit diagram of a specific implementation of the PTA is given in Fig. 6. Each of the six "coarse" control bits ($D_6 - D_{11}$) is used to turn on/off an associated current mirror stage with a particular aspect ratio. The linearized transconductor proposed by Nedungadi [6] was used (transistors M1–M19) for the input transconductance stage to achieve better linearity. Complete device sizings of the MOS transistors in Fig. 6 are listed in Table II. From [6], the overall transconductance gain can be expressed by

$$g_m = g_{md}M = 2\sqrt{\frac{k_a k_b}{3}}\left((V_{\text{tail}} - V_{SS}) - V_T\right)M \tag{9}$$

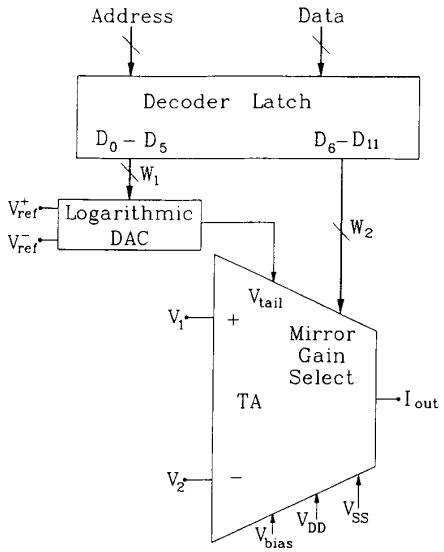


Fig. 4. Programmable transconductance amplifier structure.

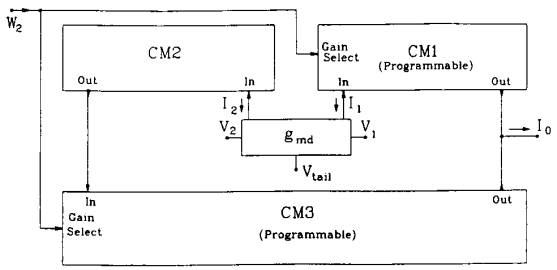


Fig. 5. Basic embedded transconductance amplifier.

where V_T is the threshold voltage of the n-channel devices, M is the output current mirror gain programmed by the "coarse" control word, and V_{tail} is the output voltage of a DAC controlled by a 6-bit "fine" adjustment word. Constant k_a is determined by the input matched-pair transistors M1 and M2, given by

$$k_a = \frac{\mu_n C_{ox}}{2} \frac{W_1}{L_1} \tag{10}$$

and k_b is a constant corresponding to bias transistors M10–M15, given by

$$k_b = \frac{\mu_n C_{ox}}{2} \frac{W_{10}}{L_{10}}. \tag{11}$$

In order to achieve uniform resolution of filter resonant frequency and bandwidth throughout the adjustment domain, successive g_m values must be uniformly spaced logarithmically, is i.e.,

$$g_{md}^{[i]} = Bg_{md}^{[i-1]}, \qquad i \in \{0, 1, \cdots, 63\} \tag{12}$$

where g_{md} is the differential stage transconductance in (9) and i corresponds to the digital setting of the fine adjustment control word. Logarithmic spacing of the "fine" adjustment range is achieved by using a logarithmic DAC that provides successive increments in V_{tail} that are equal to a constant factor B, $B > 1.0$, times as big as the previous increments. This relationship can be formulated by

$$V_{\text{tail}}^{[i+1]} - V_{\text{tail}}^{[i]} = B\left(V_{\text{tail}}^{[i]} - V_{\text{tail}}^{[i-1]}\right), \qquad i \in \{1, \cdots, 62\}. \tag{13}$$

From (9) and (13), it follows that

$$g_{md}^{[i+1]} - g_{md}^{[i]} = B\left(g_{md}^{[i]} - g_{md}^{[i-1]}\right), \qquad i \in \{1, \cdots, 62\}. \tag{14}$$

It is noted that (12) can be satisfied if the following relationship is established with (13) and consequently (14).

$$g_{md}^{[1]} = Bg_{md}^{[0]}. \tag{15}$$

If we assign $V_{\text{tail}}^{[0]} = V_{\text{ref}}^-$ and $V_{\text{tail}}^{[63]} = V_{\text{ref}}^+$, which are the minimum and maximum (i.e., references) DAC output voltages, respectively, it follows from (13) that $V_{\text{tail}}^{[i]}$ can be expressed as

$$V_{\text{tail}}^{[i]} = V_{\text{ref}}^- + \frac{1 - B^i}{1 - B^{63}}\left(V_{\text{ref}}^+ - V_{\text{ref}}^-\right). \tag{16}$$

It remains to determine V_{ref}^- and V_{ref}^+. These are determined by the minimum desired values of g_m, $g_{md}^{[0]}$ and B. It follows from (9), (15), and (16) that

$$V_{\text{ref}}^- = V_{SS} + V_T + \sqrt{\frac{3}{4k_a k_b}}\, g_{md}^{[0]} \tag{17}$$

$$V_{\text{ref}}^+ = B^{63} V_{\text{ref}}^- + (1 - B^{63})(V_{SS} + V_T). \tag{18}$$

By properly setting the range spanned by the 6-bit logarithmic DAC, the resulting fine resolution in g_m can be maintained at less than our arbitrary target specification of $\pm 0.5\%$, which corresponds to a value of $B = 1.01$. As implied by (2)–(5), if the g_m resolution is maintained at less that $\pm 0.5\%$, then the fine resolutions in ω_p and ω_z will remain at less than $\pm 0.25\%$ while the fine resolutions in BW_p and BW_z will remain below $\pm 0.5\%$.

Logarithmic spacing the coarse adjustment range can be achieved by properly selecting the current mirror gains M_1 and M_3. To ensure that there are no adjustment "gaps" between successive coarse codes, the mirror gain resolution, r_A, should be limited by the g_m range spanned by the fine adjustment, B^{63}. Thus, for a $\pm 0.5\%$ resolution in g_m (i.e., $B = 1.01$), we must satisfy the expression

$$r_A < B^{63} = (1.01)^{63} = 1.8717. \tag{19}$$

A value of $r_A = 1.618$, which is somewhat smaller than the limiting value of 1.8717, was intentionally selected to avoid adjustment "gaps" due to model errors at the fine

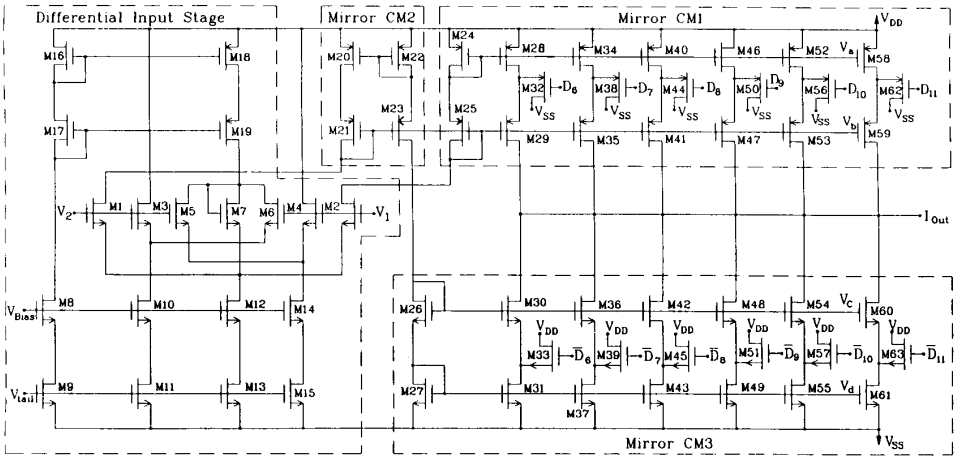


Fig. 6. Schematic of programmable transductance amplifier with two-decade programmability.

TABLE II
SIZINGS OF MOS TRANSISTORS IN PROGRAMMABLE OTA

Device	Size (microns) W	L	Device	Size (microns) W	L
M1-M2	8	5	M32-M33	7	3
M3-M4	16	5	M34-M37	6	9
M5-M6	8	5	M38-M39	7	3
M7	7	5	M40-M43	15	9
M8-M9	40	3	M44-M45	7	3
M10-M15	80	3	M46-M49	21	6
M16-M17	60	3	M50-M51	7	3
M18-M21	120	3	M52-M55	17	3
M22-M23	60	3	M56-M57	7	3
M24-M25	120	3	M58-M61	44	3
M26-M27	60	3	M62-M63	17	3
M28-M31	5	11			

adjustment/coarse adjustment transition points. The specific value of $r_A = 1.618$ was selected for reasons that will be discussed later.

The required number of logarithmically spaced coarse adjustment stage remains to be determined. With a fixed number of bits of fine adjustment and a fixed fine resolution ($\pm 0.5\%$), the number of coarse adjustment stages will define the overall adjustment range of the filter. To make this determination, assume both g_m values and capacitor values are adjustable and are adjustable with the same number of bits and same coarse resolution. Consider the pole "bandwidth" of (3), which is of the form

$$BW_p = g_m / C. \tag{20}$$

If g_{m0} and C_0 represent the minimum and maximum values for g_m and C, respectively, then the maximum value of the bandwidth is given by

$$BW_{p_{\max}} = \frac{(g_{m0}) r_A^{N-1}}{C_0 / r_A^{N-1}} B^{63} = \left(\frac{g_{m0}}{C_0}\right) r_A^{2N-2} B^{63} \tag{21}$$

where N is the number of uniform logarithmically spaced coarse component values. For a targeted three-decade adjustment range we must thus satisfy the equation

$$B^{63} r_A^{2N-2} > 10^3. \tag{22}$$

With $r_A = 1.618$ and $B = 1.01$, we obtain $N > 7.53$. The same constraint is obtained if we consider the pole/zero frequencies adjustment range as can be seen by investigating the functional form of (2)-(5). We have selected a value of $N = 11$ to offer a somewhat larger adjustment range.

It remains to practically implement the 11 logarithmically spaced programmable current mirror gains defined by the sequence

$$M_{pi} = M_{p1} r_A^{i-1}, \qquad i = 1, \cdots 11 \tag{23}$$

where M_{p1} is the minimum mirror gain. One obvious method would be to realize this with 11 separate mirrors, with the individual mirror gains characterized by (23). This would require a 4-bit control word encoded to an 11-bit bus used to select the 11 different gains. Both the bussing structure and the total area required to realize the individual current mirrors are unacceptably large.

One alternative is to realize M_{p1} with the first mirror that has gain A_1, M_{p2} with a second mirror that has gain A_2 and M_{p3} with both the first and second mirrors enabled. This process can be repeated by realizing M_{p4} with the third mirror that has gain A_3, M_{p5} with the first, second, and third mirrors, etc. This scheme is summarized in Table III. With this strategy, the successive mirror gains must satisfy the relationship

$$A_k = \begin{cases} M_{p1}, & k = 1 \\ M_{p1} r_A^{2k-3}, & k > 1 \end{cases} \tag{24}$$

and the summed enabling requirement dictates that

$$\sum_{i=1}^{k} A_k = M_{p1} r_A^{2k-2} \quad \text{for} \quad k > 1. \tag{25}$$

Whereas (24) can be satisfied for any M_{p1} and r_A, the constraint of (25) will only be satisfied for some specific

TABLE III
COARSE CONTROL WORD MAPPINGS TO CURRENT MIRROR GAINS

D_{11}	D_{10}	D_9	D_8	D_7	D_6	Gain
0	0	0	0	0	1	$(1.618)^{-10} = .00813$
0	0	0	0	1	0	$(1.618)^{-9} = .01316$
0	0	0	0	1	1	$(1.618)^{-8} = .0213$
0	0	0	1	0	0	$(1.618)^{-7} = .0344$
0	0	0	1	1	1	$(1.618)^{-6} = .0557$
0	0	1	0	0	0	$(1.618)^{-5} = .0902$
0	0	1	1	1	1	$(1.618)^{-4} = .1459$
0	1	0	0	0	0	$(1.618)^{-3} = .236$
0	1	1	1	1	1	$(1.618)^{-2} = .382$
1	0	0	0	0	0	$(1.618)^{-1} = .618$
1	1	1	1	1	1	$(1.618)^{0} = 1.000$

values of r_A. Substituting (24) into (25) and using an identity for the sum of a finite geometric series, we obtain the relationship

$$\left[1 - r_A^{2k-2}\right] \cdot \left[1 + r_A - r_A^2\right] = 0. \tag{26}$$

Equating the second multiplicand to zero, we finally obtain the relationship

$$1 + r_A - r_A^2 = 0 \tag{27}$$

which has, as a unique positive solution, $r_A = 1.618$. This value of r_A satisfies the fine range overlap requirement of (19) and is the specific reason the value of $r_A = 1.618$ was specified earlier.

Whereas the original scheme of using one mirror for each mirror gain required 11 mirrors and an 11-bit decoded control bus to drive these mirrors, the proposed scheme requires only six mirrors and a 6-bit decoded control bus (decoded from a 4-bit word) resulting in a significant reduction in mirror and bus area. The encoded 6-bit control words that control the six current mirrors are included in Table III.

Based on MOSIS 3-μm parameters, the transconductance gain gm of the digitally programmable TA is designed to be adjustable from 0.19 μs to 43 μs uniformly on a logarithmic axis with a fine resolution of less than $\pm 0.5\%$ and a coarse resolution of 61.8% such that full overlapping throughout the whole adjustment range can be ensured.

C. The Programmable Capacitor Array

Another important building block is the PCA. As mentioned previously, the PCA's can be incorporated with PTA's to achieve a wider frequency adjustment range. As can be seen from (2)–(5), capacitor adjustment of ω_o with the capacitor arrays provides for a convenient fixed-Q adjustment. The structure shown in fig. 7, provides for this coarse adjustment.

To be consistent with the previous g_m adjustment approach, it would be natural to pick $r_A = 1.618$ and use a 6-bit encoded control word to appropriately select from a set of six capacitors.

In the specific implementation of the PCA, we used an existing design that does not conform to the transconductance resolution. A finer adjustment resolution of 13% was used

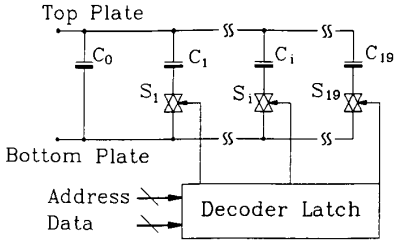


Fig. 7. Programmable capacitor array.

for the capacitor array. Equation (22) is modified to

$$B^{63} r_{A_g}^{N_g - 1} r_{A_c}^{N_c - 1} < 1000 \tag{28}$$

where r_{A_g} and r_{A_c} denote the course g_m and capacitor resolutions, and where N_g and N_c are the number of logarithmically spaced g_m and capacitor values, respectively. Substituting $B = 1.01$, $r_{A_g} = 1.618$, $N_g = 11$, and $r_{A_c} = 1.13$, we obtain $N_c > 13$. In our specific implementation, we picked $N_c = 20$ and realized this capacitor array by physically switch selecting from a set of 20 capacitors. The corresponding 5-bit control words, given in hex, which were decoded to select the appropriate capacitors, are summarized in Table IV. The capacitor values ranged from 2.44 pf to 21.26 pF. This larger capacitor array and the inherent finer resolution was used only because this array was already available as a cell used in an earlier design.

D. The Performance Monitoring System

A block diagram of the PMS appears in Fig. 8. Physically, the system is composed of a voltage-controlled oscillator (VCO) with automatic gain control, a dual channel high-speed sample-and-hold circuit, a 10-bit successive approximation analog–digital converter (ADC), and the timing/control logic. From this integratable hardware system under the direction of a performance controller, a series of measurements can be made from which the filter characteristics can be extracted.

E. The Tuning System

The overall system performance is strongly dependent upon the algorithm used to automatically tune the filter structure. Although the tuning problem has been addressed in the literature [8], [9], often in the context of deterministic trimming rather than the functional trimming that is preferred here, the problem of tuning a general robust structure, such as that of Fig. 1, remains open. Emphasis here will be placed on presenting result based upon a tuning algorithm for bandpass functions that have a single local maximum in the passband with a focus on the accuracy attainable with such algorithms. Additional details about this algorithm and a more general tuning algorithm will be addressed in a separate paper.

The bandpass tuning algorithm is based upon identifying the morphological features of the system transfer function of interest; specifically, the frequency where the gain is a maximum, the maximum gain, and the two 3-dB edges. This is achieved by randomly sampling the input and output under

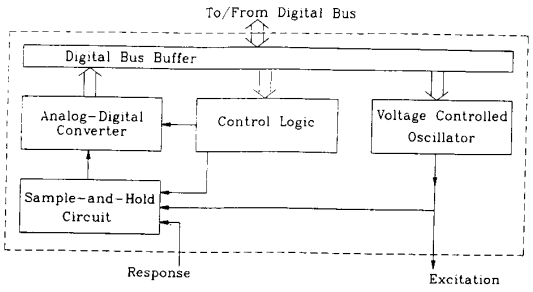


Fig. 8. The performance monitoring system.

TABLE IV
THE PCA CAPACITANCE MAPPING

N	Digital Input (hex)	$C_{top-bot}$ (pF)	N	Digital Input (hex)	$C_{top-bot}$ pF)
0	00	2.441	10	0A	7.345
1	01	2.706	11	0B	8.235
2	02	3.012	12	0C	9.251
3	03	3.360	13	0D	10.396
4	04	3.750	14	0E	11.706
5	05	4.182	15	0F	13.188
6	06	4.676	16	10	14.855
7	07	5.234	17	11	16.745
8	08	5.852	18	12	18.865
9	09	6.558	19	13	21.26

sinusoidal excitation a large number of times at a small number of known frequencies. The frequencies, although not precisely controlled, can be readily determined by frequency referencing to a stable system clock. The current algorithm requires a fast sample and hold, and a low-speed low-resolution ADC. Following identification of the system parameters of interest, a model of the system that includes the nominal parametric relationship between the tunable components and the morphological parameters of interest is invoked to predict the relative changes in the tunable components needed to meet the desired system specifications. Once this prediction is obtained, the tunable components are adjusted accordingly and the performance of the system is again measured. This iterative process is then repeated until the desired system specifications are attained. Extensive simulations of the system, including over-ordering model errors associated with parasitics, quantization and noise errors in the ADC, and large process parameter variations, showed excellent convergence characteristics.

IV. Experimental Results

A die microphoto of the specific implementation discussed in the previous section fabricated in a 3-μm CMOS process appears in Fig. 9. The physical die is 7900 μm $\times$ 9200 μm. The 64-pin package is mounted on a single-chip microcomputer-based protoboard that is interfaced to a personal computer through a serial port. The personal computer serves as a tuning host and performs the functions that will be performed by the local digital controller in the block diagram of Fig. 1. The external tuning host was used so that high level languages could be used to investigate alternative tuning strategies with emphasis placed upon analog performance and tuning accuracy.

From the design values given in the previous section, the theoretical attainable pole/zero frequency/bandwidth adjustment range of the biquad can be calculated to be from less than 2 kHz to 2 MHz with a fine resolution of less than $\pm 0.5\%$ in pole/zero bandwidths and less than $\pm 0.25\%$ in pole/zero resonant frequencies. For each biquad, each of the five programmable TA's can be programmed to select one of $11 \times 64 = 704$ logarithmically spaced transconductance values, while each of the two PCA's can be programmed to select on of 20 logarithmically spaced capacitance values. The three configuration switches in each biquad can be set to select one of eight different combinations. These numbers give each biquad $704^5 \times 20^2 \times 2^3 = 5.53 \times 10^{17}$ different transfer function settings. A portion of these settings ideally realize the same transfer function. By cascading the three biquads, the programmable filter can effectively realize a very large number of even-order transfer functions up to sixth order with more than 10^{53} different settings. The implications associated with testing an analog circuit with such programmability have not been addressed in the literature and are beyond the scope of this paper.

In this section, experimental results for a few representative filter implementations obtained with the structure of Fig. 9 are presented.

Initially, the performance of the transconductance amplifiers will be considered. The measured transconductances of the TA of Fig. 6 are shown in Fig. 10 for the 11 coarse g_m adjustments as a function of the continuous voltage V_{tail}. The quantized adjustment of V_{tail} to achieve 64 uniformly spaced fine adjustment g_m values, though not depicted, was achieved with the logarithmic DAC. The results show that g_m spans the range $0.21\ \mu A/v \leq g_m \leq 46.6\ \mu A/v$ and that the fine adjustment range overlaps the coarse adjustment range as expected. The dc transfer characteristics for the maximum mirror gain are shown in Fig. 11. This structure exhibited less than a 1% nonlinear error of the transconductance gain when driving a short circuit load for inputs up to 4 v_{pp} throughout the fine adjustment range for eight of the eleven coarse g_m settings and maintained inputs of at least 1 v_{pp} with less than 1% nonlinear error over the entire g_m adjustment range.

In Fig. 12, the experimental attainable ranges of both pole frequency and pole bandwidth for a single biquadratic section are compared with the theoretical adjustment range. The results show that the actual attainable pole frequency range spreads over three decades and is somewhat smaller than the theoretical adjustment range. This modest reduction in adjustment range is due to model errors associated with neglecting parasitic capacitances in the model but it is not problematic since the theoretical adjustment range can be readily expanded at minimal cost if a larger adjustment range is required. For extreme settings such as the right bottom "x" point in Fig. 12, a pole Q in excess of 100 is achieved at a pole frequency of nearly 1.0 MHz.

In order to further illustrate the programmability, a set of

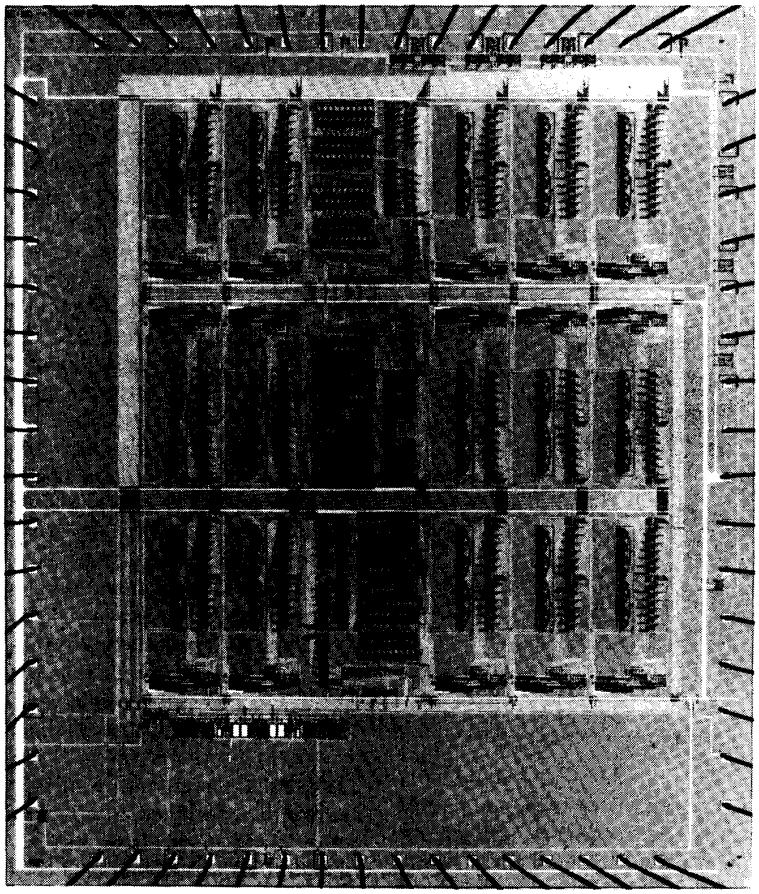


Fig. 9. Die photograph of the programmable filter.

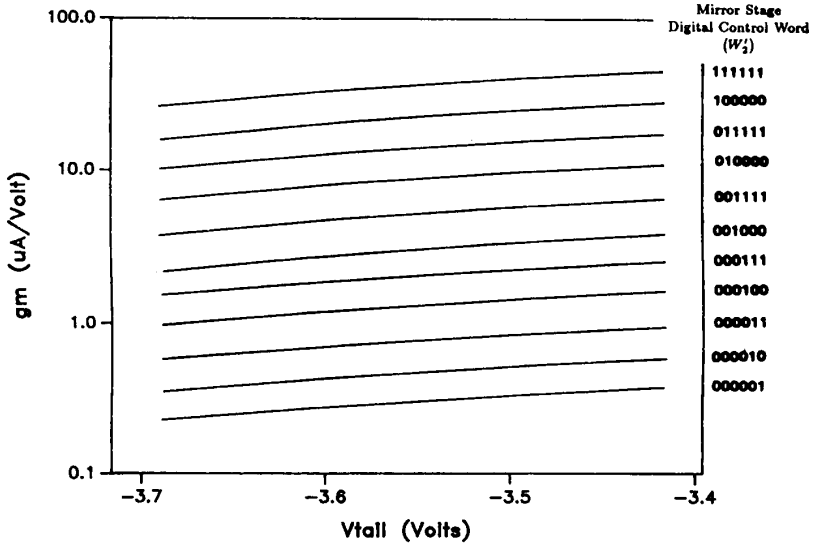


Fig. 10. g_m versus V_{tail} for 11 coarse settings of the transductance amplifier.

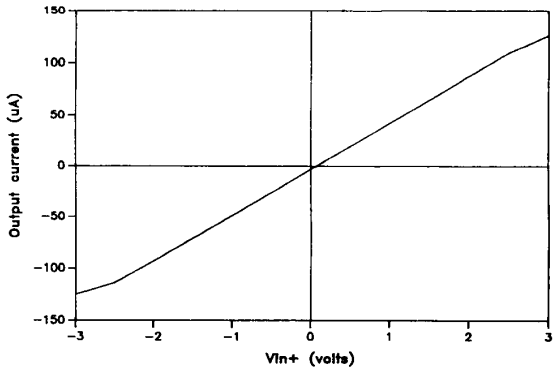


Fig. 11. Experimental dc transfer characteristics for maximum transconductance gain with noninverting input terminal shorted to ground.

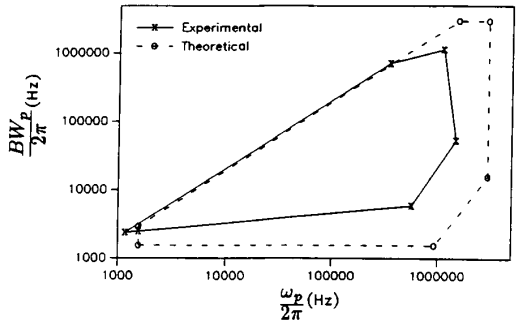


Fig. 12. f_0 and bandwidth adjustment domain.

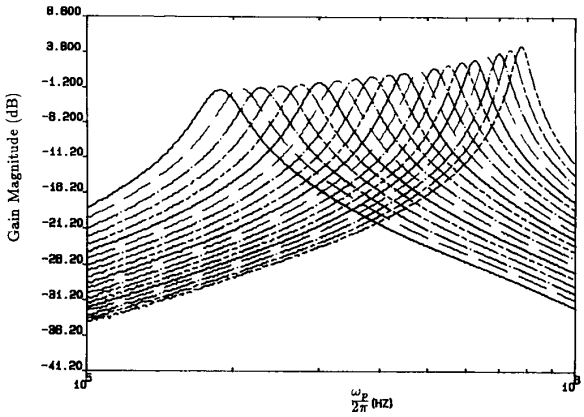


Fig. 13. f_0 adjustment with fixed Q.

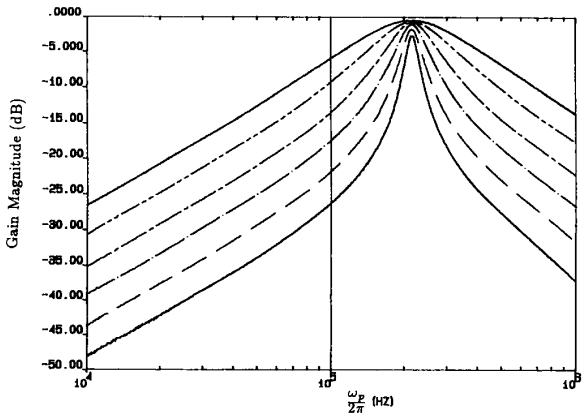


Fig. 14. Q adjustment with fixed f_0.

measurements specifically on second-order bandpass filter structures (as Table I) was conducted. Fig. 13 shows the frequency response as the pole frequency is adjusted by programming the PCA's through the coarse adjustment of C_6 and C_7, both assumed equal, in a nearly constant-Q manner. The modest, decreasing gains associated with increasing digital settings (i.e., increasing capacitor values) are caused by the added parasitic zeros due to the parasitic resistance in the analog switches of the PCA.

By programming g_{m4} and g_{m5} with the coarse adjustment of the TA's, the pole bandwidth (as well as the pole Q) is adjusted in a constant f_0 manner as depicted in Fig. 14 in which modest Q degradation can be observed. The resonant frequency with nominally constant bandwidth with adjustment of g_{m2} and g_{m3} (with $g_{m2} = g_{m3}$) is shown for six different PCA settings in Fig. 15. It should be noted that either Q enhancement of Q degradation occurs at medium and high frequencies and that moderate loss in Q resolution is observed for extreme Q's values.

Measured total harmonic distortion (THD) versus resonant frequency is presented in Fig. 16 with a fixed bandwidth of 30 kHz by incrementing digital settings of the TA's that define g_{m2} and g_{m3}. For each measurement, the input was $V_i(t) = 1.0 \sin(2\pi f_0 t)$ where f_0 is the resonant frequency of the filter. Each separative curve corresponds to a full-range fine adjustment for one coarse setting. The responses for only six coarse settings were measured out of the 11 possible settings so that a pole Q of greater than 0.5 was always maintained. It can be observed from Fig. 16 that the linearity is sensitive to the digital settings but the THD remains below 1% for $2v_{pp}$ sinusoidal inputs over all of the frequency adjustment range.

To demonstrate the reconfigurability, second-order lowpass, bandpass, high-pass, and notch functions were realized with the settings of Table I. The frequency response measurements are shown in Fig. 17. In Fig. 18, the frequency responses show nominal sixth-order Elliptic and Butterworth bandpass filters synthesized by three cascaded, *manually* pretuned biquads. Notable high-frequency feedthroughs can be observed in Fig. 17 and 18. This is believed to be caused by parasitic capacitance due to improper substrate groundings and measurement setups.

The measured dynamic range performance characteristics of selective second-order bandpass functions are summarized in Table V. The dynamic range in this table is defined to be equal to the ratio of the RMS output voltage at 1% THD for a

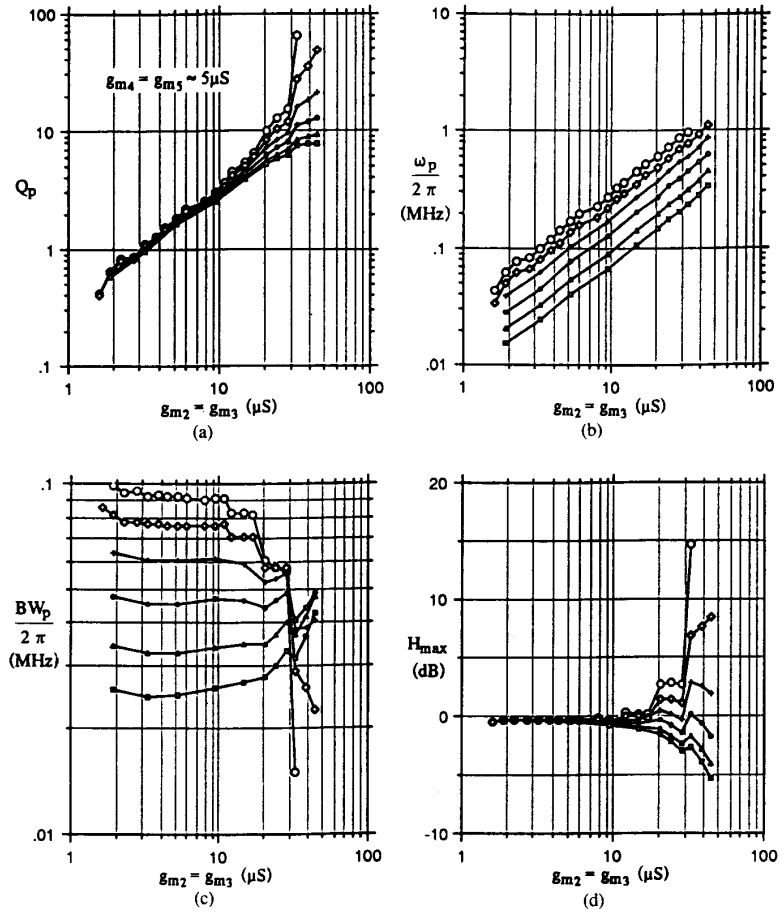


Fig. 15. f_0 adjustment with fixed bandwidth.

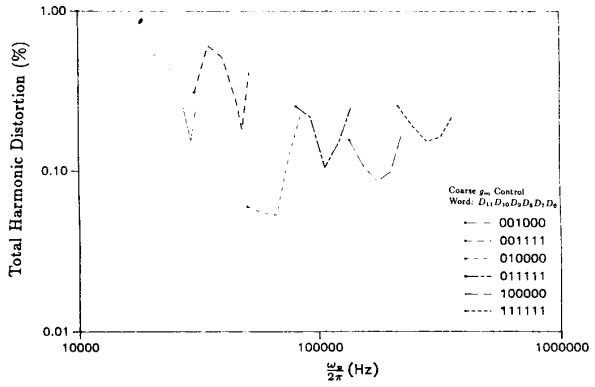
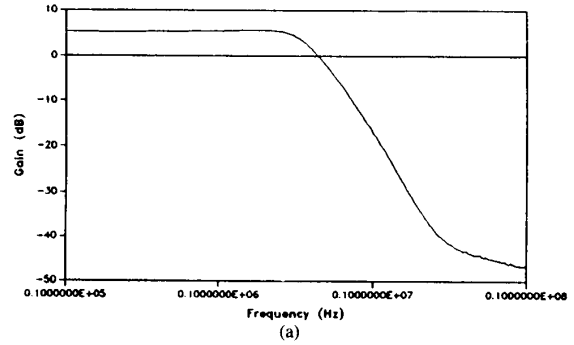


Fig. 16. THD versus f_0 with fixed bandwidth.

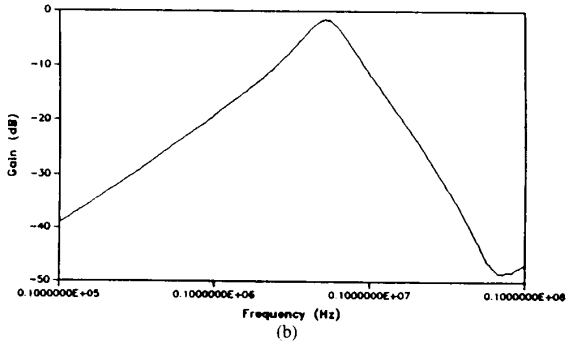
midband sinusoidal input signal divided by the total output RMS noise voltage in the passband of filter. In general, dynamic range decreases while the pole frequency or pole Q increases.

The heuristic tuning algorithm discussed previously was used to automatically tune the second-order bandpass structure. A summary of representative experimental tuning test appears in Table VI. As can be seen, extreme precision is attainable with this approach. The accuracy achievable with the current tuning algorithm is limited by the resolution of the programmable capacitor arrays and the programmable transconductance amplifier. The tuning algorithm has successfully tuned second-order bandpass filters with Q's as high as 25 to a resolution of $\pm 0.32\%$ and pole resonant frequencies as high as 1 MHz to a resolution of $\pm 0.17\%$ under severe Q enhancement in only 15–20 iterations.

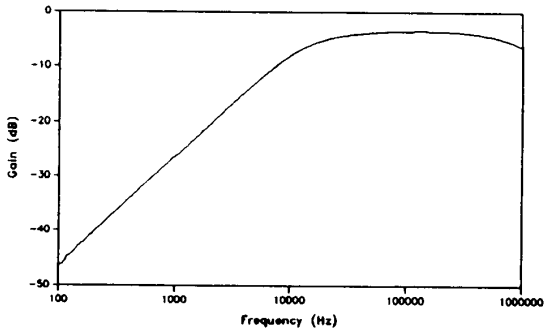
It should be noted that the tuning accuracy is directly dependent upon the performance monitor accuracy. Experiments showed that the existing performance monitor successfully extracted bandpass filter Q characteristics with Q's as high as 50 within $\pm 1.3\%$ of the actual Q value and pole resonant frequencies as high as 2 MHz within $\pm 0.03\%$ of the actual value. At lower Q's in the range of 5–10, the performance monitor exhibited an accuracy of $\pm 0.1\%$ [10]. Improvements in the sample and hold circuit and improvements in the performance of ADC, both of which are readily obtainable, should result in even better accuracy in measur-



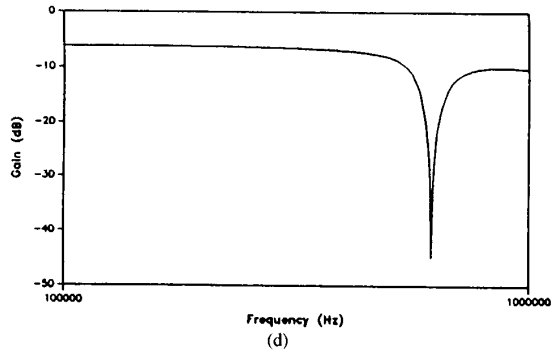
(a)



(b)

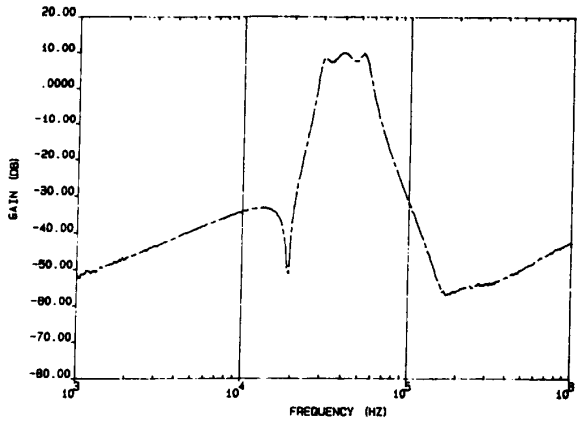


(c)

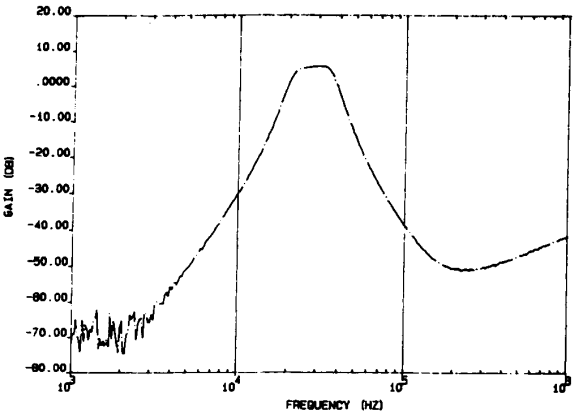


(d)

Fig. 17. Second-order filter functions. (a) Low-pass. (b) Bandpass. (c) High-pass. (d) Notch.



(a)



(b)

Fig. 18. Filter responses of three cascaded biquads. (a) Sixth-order elliptic bandpass filter function. (b) Sixth-order Butterworth bandpass filter function.

TABLE V
SIGNAL SWING AND NOISE PERFORMANCE OF SELECTIVE SECOND-ORDER BANDPASS FILTER CONFIGURATION

f_0	Q	Signal Swing V_0^*p-p	Noise Density $\mu v/\sqrt{Hz}$	Dynamic Range dB
10 kHz	1.0	1.95	2.52	69.0
100 kHz	0.96	4.36	2.1	66.1
100 kHz	12	4.64	10.0	64.5
1 MHz	1.2	2.10	0.57	63.2
1 MHz	15	2.18	4.5	56.5
1 MHz	142	1.07	32.4	52.6

*Measured at 1% THD.

ing and tuning the filter structure. Tuning accuracy is also dependent upon the linearity of the filter blocks which, in turn, is dominated by the linearity of the transconductance amplifiers and the analog switches in the present structure. As with op-amp based active filters, transconductance amplifier based filters can also experience jump resonance effects and oscillation if the Q-enhancement is too excessive. The biquadratic structure of Fig. 3 does exhibit jump resonance for some extreme inputs and oscillation due to Q-

TABLE VI
TUNING RESULTS

		Test 1	Test 2
$\omega_p/2\pi$	Specification	1 000 000 Hz	63 096 Hz
	Initial	933 160 Hz	74 083 Hz
	After Tuning	1 000 103 Hz	62 986 Hz
Q	Specifications	10.0	10.0
	Initial	19.122	8.739
	After Tuning	10.029	10.024
H_{max}(decibels)	Specification	0.0	0.0
	Initial	4.0	−2.488
	After Tuning	0.0	0.004
	Number of Iterations	15	18

enhancement for high-frequency high Q settings. Neither effect is problematic since the tuning algorithm can contain provisions for identifying and subsequently suppressing the undesired mode of operations.

V. CONCLUSIONS

A fully digitally programmable and totally reconfigurable filter structure has been introduced in this paper. A specific CMOS implementation consisting of three cascadable biquads with more than three decades of adjustment range that is capable of realizing a very large number of even-order filter functions up to sixth order has been discussed. Experimental results of this specific structure have demonstrated the performance potential of the filter structure in versatile wideband signal processing applications with typical absolute precision to $\pm 0.25\%$ in resonant frequencies and to $\pm 0.5\%$ in bandwidths. The concept itself is extendable to much high precision with practical increases in resolution of the programmable components and improvements in the performance measurement system and the tuning algorithm.

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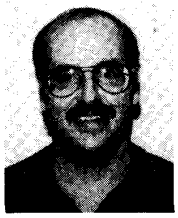

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