Very Low Voltage Operational Amplifiers Using Floating Gate MOS Transistor

Chong-Gun Yu and Randall L. Geiger
Electrical Engr. and Computer Engr. Dept.
Iowa State University
Ames, Iowa 50011

Abstract

A threshold voltage tunable op-amp structure that can be operated with a very low power supply is presented. Use of floating gate MOS transistors as the basic op-amp circuit element makes it possible to obtain a very low voltage op-amp because of the threshold voltage adjustability of the floating gate transistors. Good matching can also be achieved by tuning the threshold voltages. A two-step threshold voltage tuning scheme is presented. Due to the long term charge retention property of the floating gate transistors, the threshold voltage tuning does not have to be done frequently, and thus, near continuous-time operation of the op-amp can be achieved.

I. Introduction

With emergence of an increasing number of battery-operated applications, great interest has been aroused in low voltage circuit techniques. The research efforts for low supply voltage based operation have been focused mainly on digital circuits [1], especially on the high density memory circuits such as DRAMs and SRAMs [2],[3].

The current technology trends for low voltage operation are paralleling the scaling of device feature sizes and threshold voltages. Very low voltage operation can be possible through device scaling if the threshold voltage can be scaled down in propotion to the supply voltage scaling [4]. A 0.1μm CMOS device called a low-impurity-channel transistor has been reported in [5], where the threshold voltage can be scaled down below 0.1V. The scaling of the threshold voltage, however, requires much more complicated technologies called "substrate engineering". One problem with the scaling is the increased threshold voltage variation. There also exists a lower limit in scaling down the threshold voltage because the scaled down devices experience problems such as increased leakage currents, short channel effects and parasitic effects which are much more severe than in large feature size devices.

On the other hand, a floating gate MOS transistor is capable of having a very low threshold voltage without device scaling and without any substrate engineering. The floating gate transistor (FGT) has been used primarily as a data storage device in EPROM and EEPROM circuits [6],[7]. Recently, however, the device has started to attract considerable interests as a nonvolatile analog storage device and as a precision analog trim element because it has the threshold voltage programmability with nearly infinite resolution as well as the long term charge retention. Experimental results have demonstrated that the threshold voltage of a test FGT can be adjusted in sub-milivolt range increments with a charge loss less than 2% in 10 years at room temperature [8].

Motivated by the unique and promising characteristics of the floating gate MOS transistors, a threshold voltage tunable op-amp structure for very low voltage (e.g. 0.5V) operation is presented in this paper. To utilize the FGTs as op-amp circuit elements, their threshold voltages must be programmed and tuned. A two-step tuning method is used. One is coarse tuning, and the other is fine tuning. Two fine tuning methods are presented.

0-7803-1254-6/93$03.00 © 1993 IEEE

II. Threshold Voltage Tunable Op-amp Structure

To obtain an op-amp which can operate with a very low power supply, the threshold voltages of the floating gate MOS transistors composing the circuit must be reduced. The FGTs should also have very similiar characteristics with those of conventional MOS transistors. This has been validated in the literature [11].

The structure and the programming operation principles of a floating gate MOS transistor are well known and will not be described in detail here, except to note that when a large enough field is present across the gate oxide, in most existing FGTs Fowler-Nordheim electron tunneling allows charge to be transferred to or from the floating gate, depending on the polarity of the field. The charge amount to be transferred depends on the magnitude and duration of the programming pulse that is needed to produce a large enough electric field in the tunnel oxide. Since charge transfer to or from the floating gate affects the threshold voltage of the FGT, three variables, the magnitude, polarity, and duration of the programming pulse, can be used to control the threshold voltage.

One method of tuning the threshold voltage entails placing the FGTs in an array as shown in Fig.1. Each cell terminology is shown in Fig.2. Each cell consists of 6 transistors: a FGT, three select transistors (SD, SG, and SS) and two switch transistors (S1 and S2). The select MOS transistors are required to tune the threshold voltage of the selected FGT only, and thus, the other FGTs that are not selected will not be affected by the tuning process. The switch transistors are used to connect or disconnect the FGT with other FGTs. A switch transistor at the source terminal of the FGT is not required since high voltages are not applied at the source terminal during the threshold voltage tuning. Although each cell has two switch transistors as shown in Fig.1, two switch transistors are not always required for all cells.

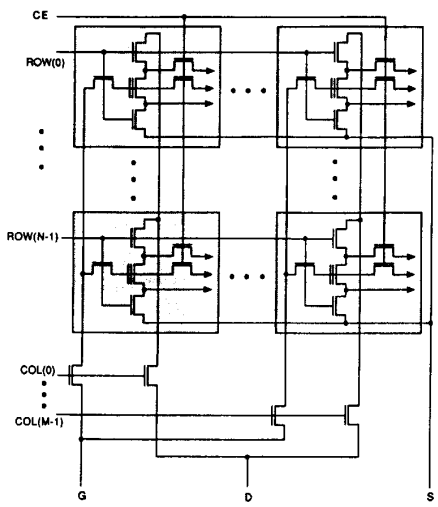

Figure 1: Floating gate MOS transistor array

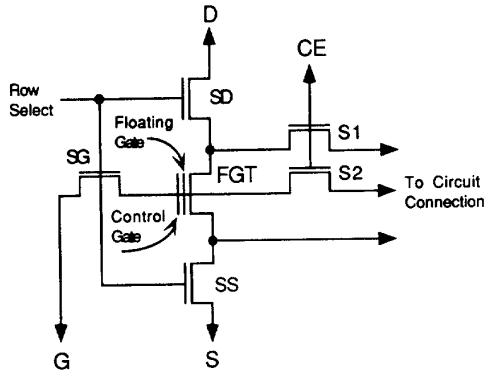

Figure 2: Floating gate MOS transistor cell terminology

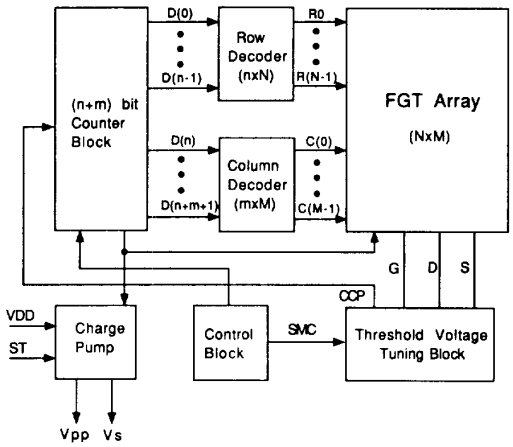

Figure 3: Simplified block diagram of the V_{th} tunable low voltage circuit

The number of switch transistors can be reduced and depends upon the circuit topology.

The threshold voltage (V_{th}) tunable op-amp circuit has two operating modes: a V_{th} tuning mode and a normal mode. In a V_{th} tuning mode the cells are disconnected from the main circuit and sequentially selected through the row and column selection lines so that the threshold voltages of the FGTs can be tuned. In a normal mode the cells are connected to each other according to the circuit topology by turning on the switch transistors, S1, and S2 in Fig.2. The signal CE is used to connect or disconnect the cells from the circuit.

III. V_{th} Tuning Strategy

One V_{th} tuning strategy is presented here. The simplified entire block diagram of the V_{th} tunable low voltage op-amp circuit is shown in Fig.3. A counter, a row decoder, and a column decoder can be used to sequentially select the cells of the FGT array. The V_{th} tuning is performed in two steps: a coarse tuning and a fine tuning. The coarse tuning is a preliminary step to provide an environment where the on-chip charge pump and the main circuit are capable of operating with a low voltage. The fine tuning is for providing a good matching properties and a desired operating point.

In the coarse tuning all the FGTs that are the elements of the FGT array are approximately programmed in a one-tuning cycle to have a very low threshold voltage (e.g. 100mV) using an external high voltage (e.g. 20V). The coarse tuning can be performed using either a closed-loop mode or a open-loop mode. This action is performed only once just after the circuit is fabricated. After the coarse tuning the entire circuit operates with a very small power supply (e.g. VDD=0.5V). The fine tuning is performed under the external control signal ST. Whenever the signal ST is detected, the fine tuning is performed, and the circuit automatically returns to a normal mode when the fine tuning is finished. The fine tuning need not be a frequent event because of the long-term charge retention characteristics of the FGTs. This can afford the possibility of near continuous-time operation.

In a fine tuning mode a high voltage is also required to adjust the threshold voltages of the FGTs. The high voltage V_{pp} is developed from VDD with an on-chip charge pump, and thus, no external high voltages are required. The charge pump consists of an oscillator, diode-connected floating gate MOS transistors, capacitors, and a voltage regulator as shown in Fig.4. The detailed operation principles of the charge pump can be seen in [9]. To make the charge pump operate with a low power supply, the oscillator and the voltage regulator circuits are also constituted of FGTs. The threshold voltages of the FGTs in the charge pump circuit are also adjusted to a very low value (e.g. 100mV) during the coarse tuning step. After that the charge pump can generate a high voltage V_{pp} from VDD, and the internally generated V_{pp} is used for the fine tuning.

When the tuning of all cells in the FGT array is completed, the circuit automatically returns to a normal mode, and the oscillator of the charge pump circuit is also disabled. Thus, the charge pump does not generate the high voltage V_{pp} any more in the normal mode and is left in a state where it awaits another ST signal. In the normal mode the switch transistors must be turned on for the circuit to function correctly. Since the switch transistors are conventional MOS transistors, they will not be turned on by the very low supply voltage. Hence, another charge pump circuit is required which can generate a voltage that is high enough to turn the switch transistors on in the normal mode. The power dissipation by the generated voltage will be very small since it is applied at only gate terminals of the MOS transistors and possibly one or two small drain or source diffusions. The frequency of the charge pump oscillator for the switch transistors does not have to be high because the load resistance is very high.

IV. Fine Tuning Method

There can be many fine tuning methods to obtain a good matching property and a desired operation of the coarsely tuned op-amp circuit. Two fine tuning methods are presented here. The first method is to adjust the threshold voltages of all FGTs to a predetermined value. The second method is to adjust the intermediate node voltages of the circuit to pre-assigned values by adjusting the threshold voltages. The

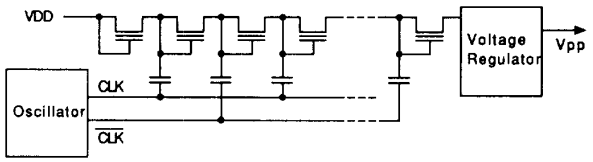

Figure 4: The charge pump circuit constituted of floating gate transistors

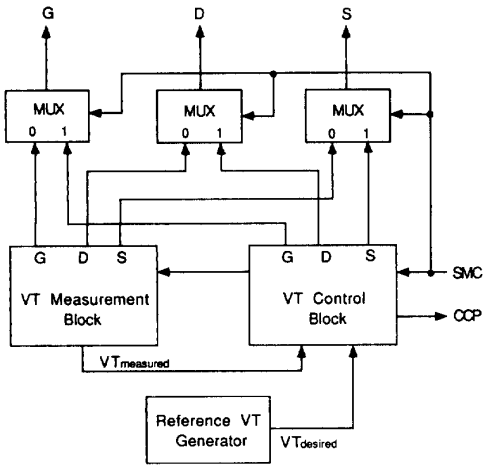

Figure 5: The block diagram of the fine tuning block

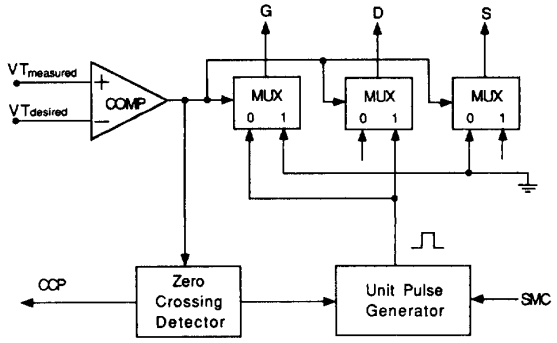

Figure 6: The VT control block

first method will be simpler and more generally applicable to all kinds of circuit structures than the second method. However, the second method will give better matching results because it can provide the node voltage matching while the first method can provide only the threshold voltage matching of the presumably matched transistors.

A. Threshold Voltage Fine Tuning Method

The block diagram of the fine tuning block for threshold voltage tuning is shown in Fig.5. During a V_{th} tuning mode this block alternately measures the threshold voltage of a selected FGT and adjusts it to a desired threshold voltage. It is controlled by the control signal SMC generated from the control block. The VT control block shown in Fig.6 compares the measured V_{th} with the desired V_{th} and then, determines the adjustment direction and also determines through a zero crossing detector whether to keep adjusting or to finish it. If further adjusting is required, the unit pulse generator generates a unit programming pulse for V_{th} adjustment. The resolution of the V_{th} tuning depends on the magnitude and width of the unit programming pulse.

The accuracy of the tuning results also depends on the performance of the VT measurement block. A simple scheme can be used to measure the threshold voltage. For example, $V_{th} \approx V_{GS}$ may be assumed at low I_{DS} [10]. This method is very simple, but the measurement error is somewhat large. Using this kind of simple method, good absolute accuracy can not be obtained, but a good threshold voltage matching can be obtained for equally sized devices. To obtain more accurate tuning, a more complicated measurement circuit is required at the expense of much larger area.

B. Node Voltage Fine Tuning Method

To obtain a better transistor pair matching of the op-amp, the internal node voltages can be adjusted to pre-assigned values by adjusting the threshold voltages. For node voltage fine tuning, a sequential tuning method for a circuit structure is required because the adjustment of one node voltage may affect the other node voltages. The order of the FGTs to be tuned must be carefully determined, and the FGTs must be placed in the FGT array according to the order. To use the node voltage fine tuning method, the circuit should be changed a little. Switch transistors for the nodes to be tuned are additionally required in the FGT array for comparison with pre-assigned values. No measurement circuit is, however, required because the node voltages are directly compared with the pre-assigned values, as defined by a reference voltage generator which can generate the same number of reference voltages as the number of nodes to be tuned. The reference voltages can be selected by the same counter and decoding circuits that are used for the FGT array.

To demonstrate the node voltage fine tuning method, an example circuit of a NMOS, instead of an n-type FGT, differential input stage which is shown in Fig.7 was simulated because there does not exist a good simulator for FGTs. In this simulation it was assumed that an n-type floating gate transistor and the NMOS transistor have very similiar characteristics except that the former can be adjusted to have various threshold voltages. This assumption has been validated in the literature [11]. The node voltage changes were simulated by changing the threshold voltages of the NMOS transistors. The simulation results have shown that the change of V_{T5} changes all the node voltages, V1, V2, and V3, and the change of V_{T1} also changes all the node voltages significantly. The change of V_{T3}, however, causes very small changes in V2 and V3. A change of 10mV in V_{T3} results in changes of less than 0.3mV in V2 and V3. The node voltages can thus be approximately adjusted to pre-assigned values by selecting the order of transistors to be adjusted. A possible node voltage fine tuning scheme for the differential input stage is as follows:

Step 1 The threshold voltage of M5 is tuned to adjust the node voltage V3 to its desired value.

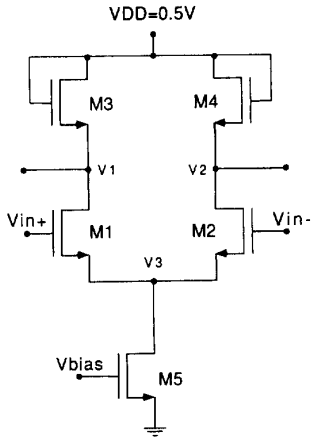

Figure 7: NMOS differential input stage

Step 2 The transistor M3 is tuned to adjust V1 to its desired value. This step little affects the node voltage V3.

Step 3 The transistor M4 is tuned to adjust V2 to its desired value. V3 will also be little affected by this step, but V1 will be a little bit changed.

Step 4 The threshold voltage of M1 is adjusted to obtain V1≈V2 by comparing V1 with V2 and adjusting M1 in the direction of reducing the difference between V1 and V2. This step will provide a good matching although the exactly pre-assigned node voltages can not be achieved. However, their difference will be very small and the convergence speed will be very fast.

The differential input stage has been tuned according to the above procedure. The tuning results are shown in Table 1. The unit step of the threshold voltage which can be adjusted was assumed to be 0.2mV. The pre-assigned node voltages were assumed to be 0.23V, 0.23V, and 0.12V for V1, V2, and V3, respectively. The initial node voltages are shown in Table 1. Step 1 took 44 unit steps to result in 0.11996V for V3. Step 2 took 14 unit steps to obtain 0.23001V for V1. This step changed the node voltage V3 by 0.11mV. Step 3 took 13 unit steps to obtain 0.23001V for V2. This step also changed V3 by 0.11mV and V1 by 0.18mV. After Step 3 all the node voltages are very close to the pre-assigned values. To obtain a good matching between V1 and V2, Step 4 was performed. Step 4 took only 1 unit step, and the consequence is that V1 differs from V2 by 0.13mV. Further reduction of the difference can be obtained by using a narrower unit step, but the improvement will be restricted by the performance of a comparator that will be used for comparing between the node voltages and the pre-assigned values. It should also be noted that adjusting the node voltages to pre-assigned values may push one of the transistors into a linear region, so careful design and selection of the desired node voltages are initially required. The node voltage fine tuning method can provide better matching property and does not require a measurement circuit. The tuning scheme should, however, be changed for other types of op-amp structures.

Table 1. Tuning results of the node voltages of a NMOS differential input stage.

	V1(V)	V2(V)	V3(V)	# of unit steps
Pre-assigned	0.23	0.23	0.12	
Initial	0.24175	0.24175	0.12842	
Step 1	0.22748	0.22748	0.11996	44
Step 2	0.23001	0.22766	0.12007	14
Step 3	0.23019	0.23001	0.12018	13
Step 4	0.23003	0.23016	0.12027	1

V. Conclusions

In this paper a method to obtain very low voltage op-amps has been presented. The op-amp are constituted of floating gate MOS transistors. Adjusting the threshold voltages of the FGTs makes the op-amp have a capability of operating with very low power supply voltages. In the simulation here, operation at a supply voltage of 0.5V was obtained. Operation at substantially lower supply voltage levels can also be readily achieved.

A two-step tuning scheme has been presented. The coarse tuning is used to adjust the threshold voltages of all FGTs to a small value (e.g. 100mV) in a one-shot cycle so that the charge pump can operate with the low voltage and thus, the FGTs of the op-amp can be tuned with an internally generated high voltage from the charge pump. The coarse tuning is performed only once. The fine tuning which is performed under an external control signal is used to provide a good matching property and a desired operation of the op-amp. Two fine tuning methods have been presented and compared, which are a threshold voltage fine tuning and a node volatge fine tuning. The basic low-voltage methodology can be extended to achieve low voltage operation in other analog as well as digital applications.

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