A FULLY DIGITAL SELF-CALIBRATION METHOD FOR HIGH RESOLUTION, PIPELINED A/D CONVERTERS

Eric G. Soenen [1], Randall L. Geiger [2]

[1] Mixed Signal Design Center
Texas Instruments Inc.
P.O. Box 655303, M.S. 8213, Dallas, Tx 75265

[2] Department of Electrical and Computer Engineering
Iowa State University
201 Coover Hall, Ames, Ia 50011-1045

Abstract

In highly accurate pipelined analog/digital converters, precise control of comparator trip-points, inter-stage amplifier gains and effective levels of reconstructing D/A converters is difficult. A new calibration approach allows errors on all these components, and compensates for them in the digital domain. A system identification technique using the converter itself, determines the required digital coefficients. The achievable accuracy is comparable to sigma-delta converters, at effective sampling rates almost two orders of magnitude higher.

Mathematical Description

Fig. 1 shows a schematic of one stage of a pipelined analog/digital converter (ADC). The incoming signal, V^{in}, is compared against a number of reference levels, V^{ref}, using a flash converter consisting of M comparators which generate a local code, cd. The flash section is followed by a reconstructing digital/analog converter (DAC), which subtracts one out of $M+1$ possible voltages, V^{DAC}, from the input signal. The difference signal ($V^{in} - V^{DAC}$) is amplified by a sample/hold (S/H) amplifier with gain A (positive or negative). The resulting signal will be called the residue, V^{res}. A possible input-referred offset of the will be considered a variation on the V^{DAC}'s.

We will consider a converter with L nominally identical stages, numbered 0 (last, or least significant stage) to $L-1$ (input, or most significant stage). For any given code, cd, of a stage, l, a general relation can be written between V_l^{res} and V_l^{in}.

$$V_l^{in} = V_l^{DAC}[cd_l] + \frac{V_l^{res}}{A_l} \tag{1}$$

From the structure of the pipeline, it is clear that $V_{l-1}^{in} = V_l^{res}$. The expression for the input voltage of each stage can then be expanded, to finally yield (omitting the cd_l for clarity):

$$V^{in} = V_{L-1}^{in} = V_{L-1}^{DAC} + \frac{V_{L-2}^{DAC}}{A_{L-1}} + \frac{V_{L-3}^{DAC}}{A_{L-1}A_{L-2}} + \cdots + \frac{V_0^{DAC}}{A_{L-1}\cdots A_1} + \frac{V_0^{res}}{A_{L-1}\cdots A_0} \tag{2}$$

This equation is valid as long as all interstage amplifiers gains are linear and free of hysteresis and the stages do not add any noise to the signal. The equation (and the calibration method) also applies to cyclic converters, in which the residue from a single stage is fed back to that same stage for successive conversions. In both cases, the local codes of all the stages are combined to form the digital conversion result (CR), according to equation (2). The last term expresses the inherent quantization error.

Minimal Converters

A *minimal* (as opposed to redundant) converter has an integer nominal gain value A and reference levels V^{ref} chosen so as to divide the input range (assumed to be between 0 and R) in as many equal parts as the absolute value of the gain, $|A|$. The number of comparators, M, is $|A|-1$. Fig. 2 shows the minimal designs for stages with nominal gains of 2, -2, -3 and 4 and their transfer function. As long as the input signal is within the input range, $0 \cdots R$, *its residue is within the same range.* The last residue will also be limited to $0 \cdots R$, and the resulting conversion error (further called quantization error), ε^{qu}, will be limited.

$$0 \le \varepsilon^{qu} \le \frac{R}{|A_{L-1}\cdots|A_0|} \approx \frac{R}{|A|^L} \tag{3}$$

We will define the range of the quantization error (inherent uncertainty of the conversion), as 1 $lsb = \frac{R}{|A|^L}$. Similarly, the relationship between the input range, R, and the range of the quantization error (1 lsb) can be expressed as the effective number of bits, N_{eff} (overall) or n_{eff} (per stage).

$$N_{eff} = \log_2(\frac{R}{1\ lsb}) = L\log_2(|A|) \text{ and } n_{eff} = \log_2(|A|) \tag{4}$$

Obtaining the conversion result is simplified when the converter is based on a radix of 2, i.e. when the inter-stage gain $A = 2^n$, with n (number of bits per stage) integer. It is then sufficient to convert the thermometer codes cd to n-bit binary and to combine the bits.

Redundancy

Parasitic variations in the reference levels V^{ref} (comparator offsets) will cause non-linearities in the overall transfer curve of a minimal converter [1]. The errors are not caused directly by the V^{ref}'s (since these do not appear in equation (2)), but because the residue of one stage exceeds the input range of the next stage, which in turn causes the next residue to be even further out of range. The last residue can get so large that equation (3) becomes invalid. The quantization error becomes significant. In practice, some of the amplifiers may also clip, which makes matters even worse.

The problem can be avoided by increasing the input range of each stage, beyond the nominal output range of the previous stage. This guarantees that the residues would remain limited, as well as the overall quantization error (within 1 lsb). The input range can be increased using a design where $M > |A|-1$. Either the number of comparators is increased, or the inter-stage gain is decreased with respect to the minimal design. Two possible of redundant stages with nominal gain of 4 are shown in fig. 3, as well as their transfer curves.

Design A uses two extra (redundant) comparators compared to the minimal case, at the top and bottom of the range [2]. One can verify that this provides an overrange capability of $\pm R/|A|$ (25 % in this case). We will call this arrangement "**minimal + 2**". Design B uses one redundant comparator compared to the minimal case and offsets both the V^{ref} and the V^{DAC} by $R/2|A|$ [3. We will call it "**minimal + 1**". It provides an overrange capability of $\pm R/(2\ |A|)$ (here 12.5 %). Either redundant scheme requires some additional logic to derive the conversion result in base-2 converters. This has conventionally been called "digital error correction" [2].

Generalized Digital Error correction

Based on equation (2), a digital error correcting scheme that also compensates for DAC and gain errors can be derived. Equation (2) will provide a correct approximation for the input voltage, as long as its terms are computed using the *actual* values of all converter components. Error correction can be performed by associating small digital look-up tables with each

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stage of the converter. Each table is addressed by the local code of the stage, and generates one term of equation (2). The terms are summed in a pipelined fashion to form the conversion result. No tuning of analog components is necessary. To fit the model of fig. 1 and keep the quantization error within bounds despite the presence of component errors, enough redundancy must be built into each stage. For a "minimal + 1" pipeline, correct operation is guaranteed when

$$(\varepsilon^{ADC} + \varepsilon^{DAC})\ R\ A + \varepsilon^{A}\ R < \frac{R}{2A} \tag{5}$$

With ε^{ADC} the worst-case flash error, ε^{DAC} the DAC error (both relative to R) and ε^{A} the worst-case relative gain error.

The straight table values would be nominally different for each stage. (Successive terms of equation (2) decrease in absolute value). This is a draw-back: the digital hardware cannot simply be duplicated from stage to stage. The structure of figure 4 uses digital multiplication to improve regularity. The table values of each stage are now nominally identical, and nominally equal to the ideal V^{DAC} values. We will call these the *weights*, $W_l[cd]$. Equation (2) now reads:

$$CR = [[[[[\frac{W_{L-1}}{A^{(L)}}]\ A + \frac{W_{L-2}}{A^{(L)}}]\ A + \frac{W_{L-3}}{A^{(L)}}]\ A + \cdots]\ A + \frac{W_0}{A^{(L)}}]\ A \tag{6}$$

With the W_l's defined as:

$$W_l[i] = V_l^{DAC}[i]\ \frac{A^{(L-1-l)}}{A_{L-1} \cdots A_{l+1}} \tag{7}$$

If A is chosen as a power of 2, the extra divisions by $A^{(L)}$ and multiplications by A can be performed by a shifting of bit lines, without additional hardware. The weights are not necessarily fractional values; they must be represented by a sufficient number of bits, to keep any truncation error well below 1 *lsb*.

The "Accuracy Bootstrapping" Algorithm

Equation (7) can only be used to compute the weights if all actual component values are known. This limitation is removed by the *"accuracy bootstrapping"* algorithm. It measures the converter and calculates the weights in an iterative fashion (hence the name). It uses the data path already present to calculate the conversion result. *The basic idea is to individually measure all the DAC levels of each converter stage, using the remaining stages of the pipeline. The measurements are used to update the look-up tables of that stage, and the process is repeated until each stage has been calibrated.* It may seem unlikely that any accuracy could be gained this way. However, for specific configurations, the procedure results in an very stable, fast-converging, iterative numerical problem.

The algorithm requires rearranging of converter stages into a circular structure, (all stages are identical). The residue of the last stage (stage 0) is fed back to the first stage ($L-1$), and so is the digital bus with the conversion result. It is now possible to inject an analog signal at the input of *any* stage, and use the circular sequence of stages back to that same point to perform the analog to digital conversion. Within each stage, the possibility is added to by-pass the flash comparators and control the reconstructing DAC externally rather than through the local codes *cd*. It is also possible to replace the analog input signal by a fixed potential, V^{fix}. The algorithm uses a DAC/subtractor combination like shown on fig. 5. The DAC is composed of a fixed voltage, used to bias the gain stage, and a number of voltages ("*DAC increments*"), which are selectively enabled and subtracted from the input voltage. The more comparators turn on (the larger the input signal). the more increments are subtracted. The depicted stage is of type "minimal + 1", with an input range between 0 and 1, and a gain of 2. The two increments of 0.5 each, result in nominal V^{DAC} values of -.25, .25 and .75 .

The accuracy bootstrapping algorithm proceeds as follows:

1) The weights of all stages are initialized to their nominal values: $W_l[i] = V_l^{DAC,nom}[i]$.
2) The last stage (stage 0) is calibrated first. The analog input of that stage is held at the fixed potential, V^{fix}, while *none* of the DAC increments are enabled. The remaining L stages of the circular structure ($L-1$, $L-2$, $\cdots$ 1), as well as the flash section of stage 0, are used to determine the conversion result, $C_0[0]$. This zero-level measurement will be used to cancel any systematic offset in the stage, as well as the unpredictability of V^{fix}.

   The analog input of the last stage is held at V^{fix} while only the *first* DAC increment is enabled. The same L stages of the circular structure ($L-1$, $L-2$. $\cdots$ 1, and flash section of 0) are used to determine the new conversion result, $C_0[1]$. The *second* DAC increment is then enabled by itself and the same procedure is followed to determine $C_0[2]$. The procedure is repeated until the M DAC increments have been measured ($C_0[1] \cdots C_0[M]$). Each $C_0[i]$ value is a measurement of $A_0\ \Delta V^{DAC}[i]$ (ΔV_i^{DAC} represents one DAC increment, $V_i^{DAC} - V_{i-1}^{DAC}$), since each increment was multiplied by the gain of stage 0 before being converted by the sequence of stages starting from stage $L-1$.

   The value $D_0[1] = (C_0[1] - C_0[0])/A$ is used as an estimate for $\Delta V_0^{DAC}[1]$. Similarly, $D_0[2] = (C_0[2] - C_0[0])/A$ is an estimate for $\Delta V_0^{DAC}[2]$. In general, $\Delta V_0^{DAC}[i]$ is estimated as $D_0[i] = (C_0[i] - C_0[0])/A$, for $i = 1 \cdots M$.

   The D_0 values are now used to estimate the new weights for stage 0 ($W_0[i]$). $W_0[0]$ is arbitrarily kept equal to its nominal value. The other weights are computed by adding the previously obtained $D_0[i]$. $W_0[1] = W_0[0] + D_0[1]$, $W_0[2] = W_0[1] + D_0[2]$, or in general: $W_0[i] = W_0[i-1] + D_0[i]$, for $i = 1 \cdots M$. All original $W_0[i]$ values of stage 0 are now replaced. Correct calibration can still be obtained when the analog components are noisy, by averaging a number of successive measurements for each $D_l[i]$ value.
3) Next, the procedure used on stage 0 is repeated to calibrate stage 1. The DAC increments of stage 1 are measured, using the converter formed by stages 0, $L-1$, $L-2$, $\cdots$ 2, and the comparator section of stage 1.
4) The same procedure is repeated to calibrate the stages $l = 2 \cdots L-1$. The DAC increments of stage l are measured, using the converter formed by stages $l-1$, $l-2$, $\cdots$ 0, $L-1 \cdots l$. The previously calibrated stage is always the first (most significant) stage in the converter used to calibrate the next one. Whenever the weights of stage $L-1$ have been updated, the first step of the calibration is complete.
5) After one iterative calibration cycle through all the stages, one could repeat the procedure starting from step 2), to further refine the estimates of the weights. However, in most cases one cycle is sufficient.
6) The resulting overall transfer characteristic may still be subject to a residual offset or gain error. This can be eliminated by appropriate linear scaling of all weights,

based on a two-point measurement of a reference signal. Adding a fixed value to all weights associated with *one* stage, results in an offset (vertical shifting) of the transfer curve. Multiplying all weights associated with *all* stages by a fixed value, changes the slope (gain) of the transfer curve.

The convergence of the procedure can be explained by the fact that when the DAC increments are estimated, most terms in the measurement for V^{fiz} and for $V^{fiz} - \Delta V_i^{DAC}$ are common, and cancel out when the difference is made. The first term is different and reflects the range between the largest and smallest DAC level in the following stage, scaled by the interstage gain. When additional stages are calibrated, any mismatches are carried forward, resulting in linearization. A detailed analysis is not within the scope of this text. Fig. 6 shows a possible block diagram of a monolithic 16-bit pipelined converter, including look-up tables and pipelined digital data path for real-time operation. A simple controller and an arithmetic unit are needed for on-chip calibration. Obviously, calibration and correction can also be performed off-chip, with dedicated logic or a general-purpose computer.

Simulations

Accuracy bootstrapping was tested through high-level Monte-Carlo simulations of converters with random errors. For a particular run, the residual worst-case non-linearity figures (in lsb) after calibration were tallied. Their mean and standard deviation were used to evaluate each archtecture. As a metric for non-linearity, worst-case INL (integral non-linearity) [4] can be used. However, a digitally corrected N-bit converter can have more than N output bits, more than 2^N transition levels and small non-monotonicities (below 1 *lsb*). Therefore, the definition of INL is generalized. INL is the amount by which the range of the total approximation error *exceeds* 1 *lsb* (inherent quantization error). Similarly, DNL (differential non-linearity) can be defined as: the amount by which the maximum difference between two consecutive digital outputs *exceeds* 1 *lsb*. Total harmonic distortion or total noise can also be used as a measure of non-linearity.

For the simulations presented below, the worst-case residual non-linearity was determined directly from a comparison between actual (found through calibration) and ideal (based on equation (7)) weights. The worst-case differences were calculated on a term-by-term basis, after correction for a possible residual gain or offset error. Although a detailed discussion of the method is beyond the scope of this text, the values are more pessimistic than the worst-case INL.

Some results are summarized in table 1. All runs used "minimal+1" architectures, on which accuracy bootstrapping was found to perform most reliably. The table lists the number of stages (L), nominal gain (A), gain error in % (eA), reference level errors (eV) and DAC errors (eD) in % of the range, input-referred noise of each stage (in *lsb*), the number of averages used during the measurements (Nav), the number of iterations (Nit) and the nominal number of bits (bits). Each batch contained 1000 runs. The table shows the mean and standard deviation of the residual non-linearity (in *lsb*).

Calibration also appears to work on "minimal+2" architectures, but results in larger residual errors and less reliability (larger sigma). A pipelined converter that seems to use a somewhat similar calibration technique with one comparator per stage and a gain smaller than 2, has also been reported [5]. Few details are presently available.

Fig. 7 shows the linearity for a number of 16-bit (16 stages with gain of 2) "minimal+1" converters, expressed in effective bits. Each of them had initial relative errors of 1% on all components. The figure shows the linearity before calibration, then each time after a stage has been calibrated (the newly calibrated stage being first in the pipeline). This is repeated for two passes of the algorithm.

Conclusion

State-of-the-art CMOS technology allows the design of fully differential switched-capacitor amplifiers with linearity and noise performance to the 14 to 16-bit level or beyond at a S/H rate of several Mhz. So far however, the inability to control component matching to the same level, has limited their application to over-sampled converters [6]. The high over-sampling ratios used (usually above 100) limit the over-all performance to audio-frequency conversion rates, where a digitally corrected pipeline could reach *the same accuracy at MHz rates.*

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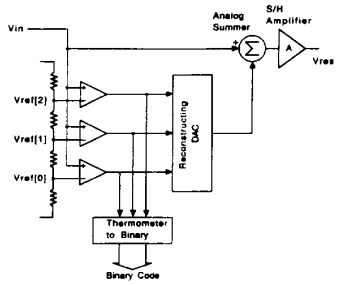

Fig. 1. Schematic of One Converter Stage

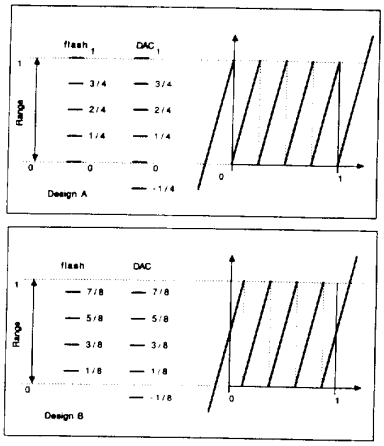

Fig. 3. Redundant Stages

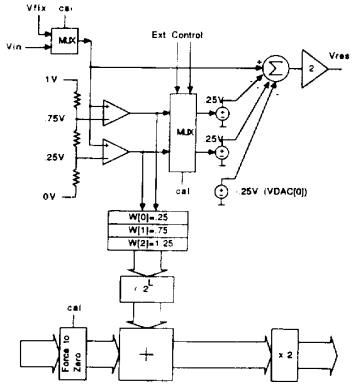

Fig. 5. Stage, Modified for Calibration

L	A	eA	eV	eD	noise	Nav	Nit	bits	mean	sigma
16	2	1	1	1	.1	1	1	16	.68	.22
16	-2	1	1	1	.1	1	1	16	.69	.21
16	-2	1	1	1	0	1	1	16	.67	.20
16	2	1	1	1	.1	1	2	16	.55	.20
16	-2	1	1	1	.1	1	2	16	.56	.20
16	-2	1	1	1	2	1	1	16	2.32	.71
16	-2	1	1	1	2	8	1	16	.91	.26
16	-2	3	3	3	.1	1	1	16	1.33	.57
16	-2	3	3	3	.1	1	2	16	.59	.22
4	4	1	1	1	.1	1	1	8	.30	.09
8	4	1	1	1	.1	1	1	16	.39	.12
20	-2	1	1	1	.1	1	1	20	.79	.24
24	2	1	1	1	.1	1	1	24	.97	.29
10	3	1	1	1	.1	1	1	15.85	.46	.14
16	2	.5	.5	.5	.1	1	1	16	.59	.19
24	-4	1	1	1	.1	1	1	48	2.53	1.26
24	-4	1	1	1	.1	1	2	48	.29	.10

Table 1. Simulation Results

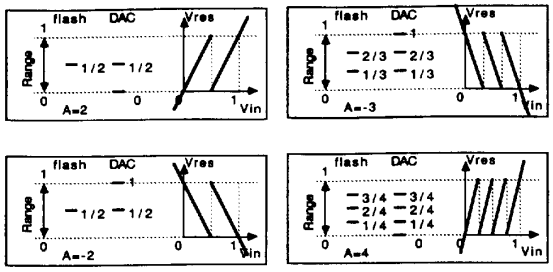

Fig. 2. Minimal Designs

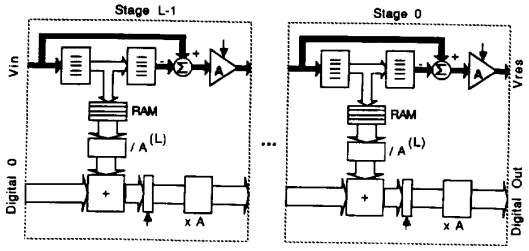

Fig. 4. Nominally Identical Look-Up Tables

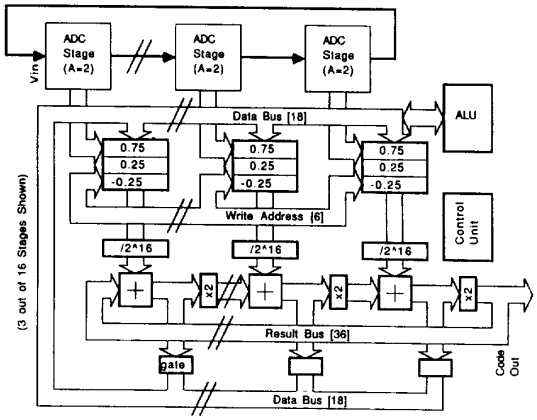

Fig. 6. Calibration Hardware

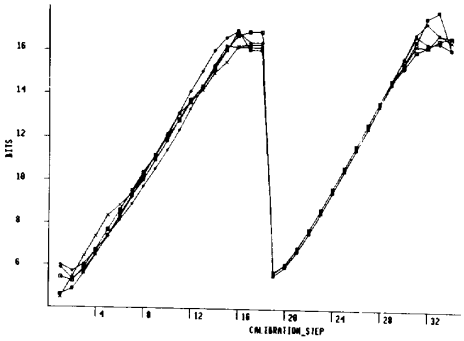

Fig. 7. Progression of the Calibration