

Performance Characterization of an Active Attenuator Using Two Cascaded MOSFETs

Joon-Yub Kim and Randall L. Geiger
 Department of Electrical Engineering and Computer Engineering
 Iowa State University
 Ames, Iowa 50011

Abstract — The practical performance characteristics of an active voltage attenuator suitable for analog integrated circuit applications are presented. The attenuator has attractive performance characteristics including high input impedance, low power consumption, small circuit area, low noise, low THD, and precisely controllable attenuation ratio over a wide range. It can replace conventional resistor attenuators in many monolithic applications. The analysis, design, and performance of the attenuator and an amplifier employing the attenuator in the feedback loop are discussed. An attenuator which has signal to THD ratio of 61.8dB at 100mV input voltage, dynamic range of 75.0dB at 1% THD, and power consumption of 106μW for an attenuation ratio of 1:10 is readily designable with two transistors smaller than 10X10μm². Employing the attenuator in the feedback loop of an amplifier of gain 10, the amplifier has a signal to THD ratio of 81.5dB at 10mV input voltage and dynamic range of 79.3dB at 0.168% THD.

I. INTRODUCTION

Attenuators have useful applications in discrete as well as integrated circuits. Some of the applications are in data converters and in the input stages of transconductance amplifiers as well as in the feedback loops of feedback amplifiers. In discrete applications, attenuators consisting of resistors connected in series are widely used. However, the resistor attenuators are not very attractive in integrated circuit applications because of their large areas, low input impedance, large power dissipation, nonlinearity of diffused resistors, and parasitic capacitances.

An active attenuator using MOSFETs monolithically fabricated in separate wells has been investigated [1-2]. That is an extension of the original two MOSFET attenuator introduced by Van Horn [3]. In this paper, emphasis is placed upon the practical application of the active attenuator. Attention is specifically focused at an active attenuator using two cascaded MOSFETs fabricated in a common substrate that has not been investigated to date. The capability to fabricate the MOSFETs for an attenuator in a common substrate has several advantages. First, both n-channel and p-channel attenuators can be monolithically fabricated in a standard CMOS process. Second, the required area for an attenuator is much smaller. Third, the parasitic capacitance at the well-substrate junction of the separate well for each transistor does not exist.

The attenuator presented in this paper is small in size, has nearly infinite input impedance, low power consumption, good linearity, and good noise characteristics. The operation principle, harmonic distortion analysis, random noise analysis,

and design and performance of the attenuator including power consumption and size consideration are investigated. The harmonic distortion analysis, the random noise analysis, and the performance of an amplifier using the attenuator in the feedback loop are also investigated.

II. ATTENUATOR ANALYSIS

An active attenuator consisting of two n-channel MOSFETs is shown in Fig. 1. The substrate is common for both the transistors and is connected to the source of the bottom transistor M1. The circuit operates as an attenuator when transistor M1 is in the ohmic region and transistor M2 is in the saturation. This condition will be met provided

$$V_{T1} < V_I < V_{DD} + V_{T2} \quad (1)$$

where $V_{T1} = V_{TON1}$, and

$$V_{T2} = V_{TON2} + \gamma(\sqrt{\phi + V_O} - \sqrt{\phi}). \quad (2)$$

If the zero-bias threshold voltages of the two transistors, V_{TON1} and V_{TON2} , are not matched and V_{TON2} is larger than V_{TON1} , then V_{T1} in Inequality (1) should be replaced by V_{TON2} . Since M1 is operating in the ohmic region and M2 in the saturation region, the drain current of each transistor is given by

$$I_{D1} = K' \frac{W_1}{L_1} (V_I - V_{T1} - \frac{V_O}{2}) V_O, \quad (3)$$

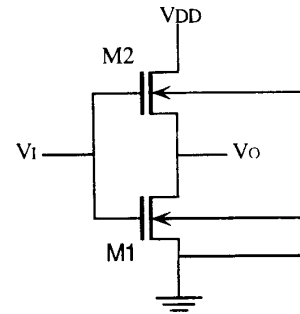


Fig. 1. The circuit diagram of the active attenuator consisting of two n-channel MOSFETs

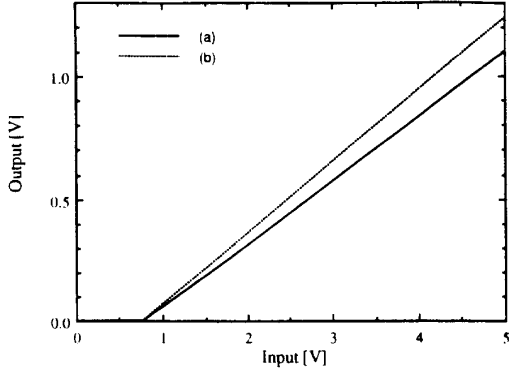


Fig. 2. dc transfer characteristics of the attenuators
(a) Eq. (5), (b) Eq. (7)

and

$$I_{D2} = K' \frac{W_2}{2L_2} (V_I - V_{T2} - V_O)^2. \quad (4)$$

Because the two drain currents should be same, from Eq. (2-4), the transfer characteristic relating V_I and V_O is obtained to be

$$2R(V_I - V_{TON1} - \frac{V_O}{2})V_O = \{V_I - V_{TON2} - V_O - \gamma(\sqrt{\phi + V_O} - \sqrt{\phi})\}^2 \quad (5)$$

where

$$R = \frac{W_1/L_1}{W_2/L_2}. \quad (6)$$

If $\gamma=0$ and $V_{TON1}=V_{TON2}=V_{TON}$, Eq. (5) reduces to a linear equation (7), which is the case where each transistor is fabricated in a separate substrate, the substrate of each transistor is connected to its source, and the zero bias threshold voltage of each transistor is assumed to be same.

$$V_O = (V_I - V_{TON}) \left(1 - \sqrt{\frac{R}{R+1}}\right) \quad (7)$$

The dc transfer characteristics between V_I and V_O calculated from Eq. (5) and (7) for $R=1$, $\gamma=0.5255\text{V}^{1/2}$, $\phi=0.6\text{V}$, and $V_{TON1}=V_{TON2}=V_{TON}=0.777\text{V}$ are shown in Fig. 2. Note that, for $\gamma=0.5255\text{V}^{1/2}$, and $\phi=0.6\text{V}$, which are standard for 2μ p-well CMOS process, the dc transfer characteristic of the attenuator given by Eq. (5) is also very linear as shown in Fig. 2

even though the equation is seemingly nonlinear quadratic. The high degree of linearity exhibited in Fig. 2 suggests applications in high performance applications. Thus, a more detailed analysis is in order to quantify the performance potential of the attenuator.

In order to analyze the small signal attenuation factor and the harmonic distortion, the dc transfer characteristic given by Eq. (5) is expanded into Taylor's series. For $V_I = V_{IQ} + v_i$ where V_{IQ} and v_i are the quiescent and the ac signal components of the input voltage, respectively, the output voltage, V_O , is expanded as

$$V_O = H(V_I) = V_{OQ} + H'(Q)v_i + \frac{1}{2}H''(Q)v_i^2 + \dots \quad (8)$$

where $V_{OQ} = H(V_{IQ})$ is given from Eq. (5), and $H'(Q)$ and $H''(Q)$ are given by Eq. (9) and (10), respectively (see bottom of page). In Eq. (9-10), $V_{TON1}=V_{TON2}=V_{TON}$ has been assumed (this will be assumed henceforth). α defined by Eq. (9) is the small signal attenuation factor of the attenuator.

If $v_i = A \sin \omega t$, then, taking only the first three terms in Eq. (8), we obtain

$$V_O \approx h_0 + h_1 \sin \omega t + h_2 \cos 2\omega t \quad (11)$$

where

$$h_0 = V_{OQ} + \frac{1}{4}H''(Q)A^2, \quad (12)$$

$$h_1 = H'(Q)A = \alpha A, \quad (13)$$

and

$$h_2 = -\frac{1}{4}H''(Q)A^2. \quad (14)$$

In these expressions, h_0 is the total dc, h_1 is the "desired" ac signal, and h_2 is the 2nd harmonic component of the output of the attenuator. Note that the 2nd-order distortion introduces additional dc offset as shown in Eq. (12) which will generally be very small. Using Eq. (5), and (9), the small signal attenuation factor, α , and the output quiescent voltage, V_{OQ} , for given R and V_{IQ} , or the necessary R and the output quiescent voltage, V_{OQ} , for given α , and V_{IQ} can be calculated. Then, using Eq. (10) and (13-14), the signal output, h_1 , and the 2nd harmonic output, h_2 , can be calculated for given input signal amplitude, A .

A noise equivalent circuit of the attenuator based on noiseless transistors and output noise sources, and its equivalent

$$H'(Q) \left(\frac{dV_O}{dV_I} \right)_Q \equiv \alpha = \frac{-RV_{OQ} + \{V_{IQ} - V_{TON} - V_{OQ} - \gamma(\sqrt{\phi + V_{OQ}} - \sqrt{\phi})\}}{R(V_{IQ} - V_{TON} - V_{OQ}) + \{V_{IQ} - V_{TON} - V_{OQ} - \gamma(\sqrt{\phi + V_{OQ}} - \sqrt{\phi})\} \left(1 + \frac{\gamma}{2\sqrt{\phi + V_{OQ}}}\right)} \quad (9)$$

$$H''(Q) \left(\frac{d^2V_O}{dV_I^2} \right)_Q \equiv \alpha = \frac{R\alpha(\alpha-2) + \left(1 + \alpha \left[1 + \frac{\gamma}{2\sqrt{\phi + V_{OQ}}}\right]^2 - 2\frac{\gamma}{\sqrt{\phi + V_{OQ}}} + \{V_{IQ} - V_{TON} - V_{OQ} - \gamma(\sqrt{\phi + V_{OQ}} - \sqrt{\phi})\} \frac{\gamma}{4\sqrt{\phi + V_{OQ}}}\right)}{R(V_{IQ} - V_{TON} - V_{OQ}) + \{V_{IQ} - V_{TON} - V_{OQ} - \gamma(\sqrt{\phi + V_{OQ}} - \sqrt{\phi})\} \left(1 + \frac{\gamma}{2\sqrt{\phi + V_{OQ}}}\right)} \quad (10)$$

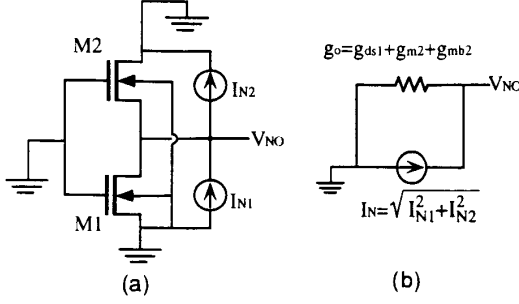


Fig. 3. (a) The noise equivalent circuit of the attenuator based on noiseless transistors and output noise sources. (b) The noise small signal equivalent circuit.

small signal circuit are shown in Fig. 3. At a given quiescent point, the channel conductance of M1, g_{ds1} , the gate-channel transconductance of M2, g_{m2} , and the bulk-channel transconductance of M2, g_{mb2} are, from Eq. (3-4), given by

$$g_{ds1} = \left(\frac{\partial I_{D1}}{\partial V_{DS1}} \right)_Q = K' \frac{W_1}{L_1} (V_{IQ} - V_{TON} - V_{OQ}), \quad (15)$$

$$g_{m2} = \left(\frac{\partial I_{D2}}{\partial V_{GS2}} \right)_Q = K' \frac{W_2}{L_2} \{ V_{IQ} - V_{TON} - V_{OQ} - \gamma (\sqrt{\phi + V_{OQ}} - \sqrt{\phi}) \}, \quad (16)$$

$$\text{and } g_{mb2} = \left(\frac{\partial I_{D2}}{\partial V_{BS2}} \right)_Q = g_{m2} \frac{\gamma}{2\sqrt{\phi + V_{OQ}}}. \quad (17)$$

The total output conductance, g_o , is given by

$$g_o = g_{ds1} + g_{m2} + g_{mb2}. \quad (18)$$

For the output noise sources, since M1 is operating in the ohmic region and M2 is in the saturation region, the respective noise current spectral density for each transistor is given by

$$S_{I1} = S_{IT1} + S_{If1} = 4kTg_{ds1} + \frac{2K_f K' I_{DQ}}{C_{OX} L_1^2 f}, \quad (19)$$

and

$$S_{I2} = S_{IT2} + S_{If2} = \frac{8}{3} kTg_{m2} + \frac{2K_f K' I_{DQ}}{C_{OX} L_2^2 f} \quad (20)$$

where S_{IT1} and S_{IT2} denote the thermal noise current spectral densities and S_{If1} and S_{If2} denote the flicker noise current spectral densities of the two transistors. K_f is the processing dependent flicker noise coefficient. The total noise current spectral density of the attenuator is given by

$$S_I = S_{I1} + S_{I2}. \quad (21)$$

From Fig. 3 (c), the output noise voltage(rms) is given by

$$V_{NO} = \frac{I_N}{g_o} = \frac{\sqrt{I_{N1}^2 + I_{N2}^2}}{g_o} = \frac{\sqrt{\int_{f_1}^{f_2} S_I df}}{g_o}. \quad (22)$$

Thus, from Eq.(15-22),

$$V_{NO} = \left[\frac{L_2}{W_2} \left\{ M + N \left(\frac{1}{2} + \frac{1}{2} \right) \right\} \right]^{1/2} \quad (23)$$

where M and N are given by Eq. (24) and (25) (see bottom of page). Using Eq. (6) and (23-25), the output noise voltage(rms) can be calculated for a given quiescent point, W_1 , L_1 , W_2 , L_2 , and noise frequency band.

III. AMPLIFIER ANALYSIS

In this section, an amplifier consisting of an ideal Op-amp and the active attenuator in the feedback loop as shown in Fig. 4 is considered. The offset inherent in the specific attenuator of Fig. 1 makes the amplifier have different input and output offset. Since the Op-amp is assumed ideal,

$$V_I' = V_O = H(V_I) = H(V_O'), \quad (26)$$

or

$$V_O' \equiv T(V_I') = H^{-1}(V_I') \quad (27)$$

that is, the transfer function of the amplifier, T , is the inverse of the transfer function of the attenuator, H .

For $V_I' = V_{IQ}' + v_i'$, the Taylor's series expansion of the output of the amplifier, V_O' is given by

$$V_O' = T(V_I') = V_{OQ}' + T'(Q)v_i' + \frac{1}{2} T''(Q)v_i'^2 + \dots \quad (28)$$

$$M = \frac{R(V_{IQ} - V_{TON} - V_{OQ}) \frac{4kT}{K'} (f_2 - f_1) + \{ V_{IQ} - V_{TON} - V_{OQ} - \gamma (\sqrt{\phi + V_{OQ}} - \sqrt{\phi}) \} \frac{8kT}{3K'} (f_2 - f_1)}{\left[R(V_{IQ} - V_{TON} - V_{OQ}) + \{ V_{IQ} - V_{TON} - V_{OQ} - \gamma (\sqrt{\phi + V_{OQ}} - \sqrt{\phi}) \} \left(1 + \frac{\gamma}{2\sqrt{\phi + V_{OQ}}} \right) \right]^2}, \quad (24)$$

$$N = \frac{R \left(V_{IQ} - V_{TON} - \frac{V_{OQ}}{2} \right) V_{OQ} \frac{2K_f}{C_{OX}} \ln f_2}{\left[R(V_{IQ} - V_{TON} - V_{OQ}) + \{ V_{IQ} - V_{TON} - V_{OQ} - \gamma (\sqrt{\phi + V_{OQ}} - \sqrt{\phi}) \} \left(1 + \frac{\gamma}{2\sqrt{\phi + V_{OQ}}} \right) \right]^2}. \quad (25)$$

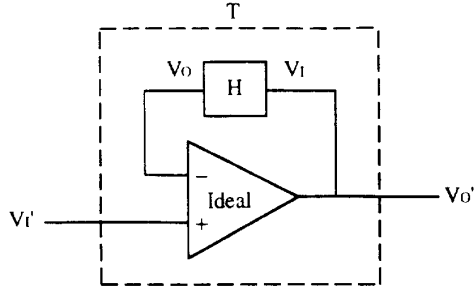


Fig. 4. An amplifier consisting of an Op-amp and the active attenuator in the feedback loop.

where $V_{OQ}' = T(V_{IQ}') = V_{IQ}$,

$$T'(Q) = \left(\frac{dV_{OQ}'}{dV_I'} \right)_{Q=g} = \frac{1}{\alpha} \quad (29)$$

and $T''(Q)$ is given by Eq. (30) (see bottom of page). Note that the small signal gain of the amplifier, g , defined by Eq. (29) and (9) is just the reciprocal of the attenuation factor of the attenuator, α , in the feedback loop. If $v_i' = A' \sin \omega t$, then, taking only the first three terms in Eq. (28),

$$V_{OQ}' \approx t_0 + t_1 \sin \omega t + t_2 \cos 2\omega t \quad (31)$$

where

$$t_0 = V_{OQ}' + \frac{1}{4} T''(Q) A'^2 \quad (32)$$

$$t_1 = T'(Q) A = g A' \quad (33)$$

and

$$t_2 = -\frac{1}{4} T''(Q) A'^2 \quad (34)$$

In these expressions, t_0 is the total dc, t_1 is the ac signal, and t_2 is the 2nd harmonic component of the output of the amplifier, respectively. Again, note that the 2nd-order distortion introduces additional dc offset as shown in Eq. (32) which will generally be very small. Using Eq. (5), (9), (26), and (29), the small signal gain of the amplifier, g , and the output quiescent voltage, V_{OQ}' , for given R and V_{IQ}' or the necessary R and the output quiescent voltage, V_{OQ}' for given g and V_{IQ}' can be calculated. Then, using Eq. (30), and (33-34), the signal output, t_1 , and the 2nd harmonic output, t_2 , can be calculated for a given input signal amplitude, A' .

Since the Op-amp is assumed ideal, and since the transfer function of the amplifier is the inverse of the transfer function of the attenuator, the output noise voltage of the amplifier is the input referred noise voltage of the attenuator which is simply given by $V_{NO}' = g V_{NO}$ where V_{NO} is given by Eq. (23-25).

Table 1. The calculated results for $\alpha=0.1$ ($g=10$), (a) input operating point, (b) corresponding output operating point, (c) corresponding R , (d) H'' , (e) signal to 2nd harmonic distortion ratio of the output of the attenuator at $A=100\text{mV}$, (f) T'' , (g) signal to 2nd harmonic distortion ratio of the output of the amplifier at $A'=10\text{mV}$.

(a)	(b)	(c)	(d)	(e)	(f)	(g)
V_o [V]	V_{oQ} [V]	R	H'' [1/V]	$ h_1/h_2 $ [dB]	T'' [1/V]	t_1/t_2 [dB]
1	0.02229	3.9529	0.005019	58.0	-0.5912	76.6
1.5	0.07218	3.9649	0.004388	59.2	-0.4414	79.1
2	0.1220	3.9744	0.003970	60.1	-0.4219	79.5
2.5	0.1717	3.9847	0.003565	61.0	-0.3525	81.1
3	0.2214	3.9923	0.003264	61.8	-0.3366	81.5
3.5	0.2710	4.0005	0.002982	62.6	-0.2997	82.5
4	0.3206	4.0072	0.002750	63.3	-0.2803	83.1
4.5	0.3701	4.0144	0.002535	64.0	-0.2514	84.0
5	0.4196	4.0207	0.002351	64.6	-0.2309	84.8

IV. DESIGN AND PERFORMANCE

The design of attenuators for a given attenuation factor, α , is considered in this section. The operating point, area, power dissipation, 2nd harmonic distortion, output noise, and high frequency performance are considered in the design. The performances of the designed attenuator and the amplifier shown in Fig. 4 are calculated and discussed in terms of the 2nd harmonic distortion and output noise.

For a given α , from Eq. (5) and (9), the required value of R and the resultant V_{OQ} are calculated as a function of the input operating point, V_{IQ} . For $\alpha=0.1$, the calculated results are shown in column (c) and (b) in Table 1. The H'' is calculated from Eq. (10) and given in column (d) in Table 1. Note that, for a given α and operating point, H'' is fixed. Likewise, the T'' is calculated from Eq. (30) and shown in column (f) in Table 1. Remember that $V_{IQ}' = V_{OQ}$, $V_{OQ}' = V_{IQ}$, and $g=1/\alpha$. Also, T'' is fixed for a given g and operating point. From Eq. (13-14), and (33-34), the signal output to 2nd harmonic output ratio for the attenuator, h_1/h_2 , and for the amplifier, t_1/t_2 , are respectively given by

$$\frac{h_1}{h_2} = \frac{4\alpha}{H'' A} \quad (35)$$

and

$$\frac{t_1}{t_2} = \frac{4g}{T'' A'} \quad (36)$$

Note that the output signal to 2nd harmonic distortion ratios are inversely proportional to the amplitude of the input signal. The calculated ratios for the attenuator when $A=100\text{mV}$, and for the amplifier when $A'=10\text{mV}$ are shown in column (e), and (g).

$$T''(Q) = \left(\frac{d^2 V_{OQ}'}{dV_I'^2} \right)_Q = \frac{R(2g-1) \left\{ g-1 - \frac{\gamma}{2\sqrt{\phi+V_{IQ}'}} \right\}^2 \left\{ V_{OQ}' V_{TON} - V_{IQ}' \gamma \left(\sqrt{\phi+V_{IQ}'} - \sqrt{\phi} \right) \right\}}{-R V_{IQ}' \left\{ V_{OQ}' V_{TON} - V_{IQ}' \gamma \left(\sqrt{\phi+V_{IQ}'} - \sqrt{\phi} \right) \right\}} \frac{\gamma}{4\sqrt{\phi+V_{IQ}'}} \quad (30)$$

respectively. It is seen that the signal to 2nd harmonic distortion ratio is 61.8dB for the attenuator and 81.5dB for the amplifier at $V_{IQ}=V_{OQ}'=3V$, and that these improve further as the quiescent voltage increases in both the attenuator and the amplifier.

Once $R=W_1L_2/L_1W_2$ is fixed for a given α and operating point, the respective $W_1, L_1, W_2,$ and L_2 values can be determined for minimum power dissipation, and less output noise or better high frequency performance within a given range of L and W . The total power dissipation, P_d , of the attenuator is given by $V_{DD}I_D$ where V_{DD} is assumed to be given and I_D is given by Eq. (3) or (4). Thus, for minimum power dissipation, the ratios W_1/L_1 and W_2/L_2 should be minimum. For a given range of L and W , first W_2/L_2 is set to minimum, W_{min}/L_{max} , since $W_1/L_1=(W_2/L_2)XR$ is larger than W_2/L_2 in practical cases ($R>1$). For W_1 and L_1 , there are two different possible choices within the given range of W and L , and for a given value of R ; Choice I is to set $W_1=W_{min}R$ and $L_1=L_{max}$; Choice II is to set $W_1=W_{min}$ and $L_1=L_{max}/R$. The former choice gives less output noise since L_1 is larger in Eq. (23) and better matched performance when actually fabricated. On the other hand, the latter choice gives smaller area and better high frequency performance. For $\alpha=0.1$, and several ranges of L and W , the output noise voltage, V_{NO} , and the power dissipation, P_d , of the attenuators designed as described above are calculated as a function of input quiescent voltage, V_{IQ} , using Eq. (23-25) and (3), and shown in Table 2. In the calculation, $V_{DD}=5V, T=298^{\circ}K, f_1=100Hz, f_2=1MHz, K'=5.663 \times 10^{-5}A/V^2, C_{ox}=8.125 \times 10^{-4}F/m^2$ and $K_f=3 \times 10^{-24}V^2F$ are used which are standard for a 2μ p-well CMOS process. From Table 2, it is seen that the output noise slightly decreases but the power dissipation increases as the operating voltage increases, and that the output noise increases but the power dissipation decreases as the maximum size of the transistors increases.

For a given operating point, the dynamic range defined by

$$DR = \frac{\text{output signal at 1\% THD}}{\text{in-band output noise}} \quad (37)$$

can be calculated from the results in Table 1 and 2. If we choose $V_{IQ}=V_{OQ}'=3V$ for maximum signal swing, and select Choice I and $2\mu m < L, W < 10\mu m$, then $H''=0.003264V^{-1}$ $V_{NO}=1.54 \times 10^{-5}V(\text{rms})$ and $P_d=106\mu W$ for the attenuator, and $T''=-0.3366V^{-1}$ and $V_{NO}'=gV_{NO}=1.54 \times 10^{-4}V(\text{rms})$ for the amplifier. Thus, From Eq. (35-36), $|h_2/h_1|=1\%$ at $A=1.23V$, and $t_2/t_1=1\%$ at $A'=1.189V$. Thus, using Eq. (13) and (37), we obtain $DR=75.0\text{dB}$ for the attenuator. $A'=1.189V$ will saturate the output of the amplifier. The maximum input amplitude applicable to the amplifier is $A' \approx 0.2V$ which results in 0.168% THD. From Eq. (33), at 0.168% THD, the dynamic range with a more stringent THD in Eq. (37) is $DR=79.3\text{dB}$.

Although the dynamic range as defined by Eq. (37) is widely used to characterize linear circuits, it gives little insight into the relationship between desired signal energy and unwanted energy at the output. An alternative criteria proposed here for characterizing the performance is the maximum of the ratio of the signal output to the total non-signal output defined

Table 2. The calculated results for the output noise voltage, V_{NO} , and the power dissipation, P_d , of the designed attenuators.

$\alpha=0.1, W_{min}=L_{min}=2\mu m$, and the corresponding V_{OQ} and R to each V_{IQ} are given in Table 1.

Choice I : $W_1=W_{min}R, L_1=L_{max}; W_2=W_{min}$, and $L_2=L_{max}$.

Choice II : $W_1=W_{min}, L_1=L_{max}/R; W_2=W_{min}$, and $L_2=L_{max}$.

Lmax Wmin(μm), Choice	V _{IQ} (V)	2		3		4	
		V _{NO} (V _{rms})	P _d (μW)	V _{NO} (V _{rms})	P _d (μW)	V _{NO} (V _{rms})	P _d (μW)
10	I	1.84E-5	31.9	1.54E-5	106	1.42E-5	223
	II	3.45E-5		3.32E-5		3.27E-5	
100	I	4.73E-5	3.19	3.52E-5	10.6	2.93E-5	22.3
	II	4.82E-5		3.64E-5		3.08E-5	
1000	I	1.49E-4	0.319	1.11E-4	1.06	9.21E-5	2.23
	II	1.49E-4		1.11E-4		9.21E-5	
10000	I	4.71E-4	0.0319	3.50E-4	0.106	2.91E-4	0.223
	II	4.71E-4		3.50E-4		2.91E-4	

by

$$STNR = \frac{\text{signal output}}{\text{non-signal output}_{\max}} = \frac{h_1}{\sqrt{h_2^2 + 2V_{NO}^2}_{\max}} \quad \text{or} \quad \frac{t_1}{\sqrt{t_2^2 + 2V_{NO}^2}_{\max}} \quad (38)$$

For the same operating point and conditions as used above, $STNR=54.5\text{dB}$ at $A=163\text{mV}$ for the attenuator, and $STNR=64.4\text{dB}$ at $A'=50.9\text{mV}$ for the amplifier.

V. CONCLUSION

The harmonic distortion and noise analyses of an active attenuator are investigated. A design scheme of the attenuator for minimum power dissipation and low noise within a given range for the size of the transistors was presented. Quantitative calculation of the performance at given sets of conditions was discussed. An amplifier employing the attenuator in the feedback loop was investigated as well. The results show that a useful monolithic attenuator with good performance as evidenced by its low power consumption, low THD, and low noise characteristics can be built simply with two transistors.

The promising performance of the attenuator demands experimental verification of the operation and performance of the attenuator. The fabrication of the attenuator is in progress. For more general applications of the attenuator, research on adjustment of the offset is also under investigation.

REFERENCES

- [1] S. C. Qin and R. L. Geiger, "A Linear Monolithic Active Attenuator with Multiple Output Taps", Proc. 30th Midwest Symposium on Circuits and Systems, pp765-768, Syracuse, 1987
- [2] K. H. Loh and R. L. Geiger, "Dynamic Range Performance of a MOS Active Attenuator", Proc. IEEE Int. Symp. on Circuits and Systems, pp1733-1736, June 1991
- [3] M. Van Horn and R. L. Geiger, "A CMOS OTA for Voltage-Controlled Analog Signal Processing", Proc. 28th Midwest Symposium on Circuits and Systems, pp596-599, Kentucky, 1985