

# An Automatic Offset Compensation Scheme with Ping-Pong Control for CMOS Operational Amplifiers

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**Abstract**—An automatic offset compensation scheme for CMOS operational amplifiers is presented. Offset is reduced by digitally adjusting the bias voltage of a programmable current mirror which is used as the load of the differential input stage. A 100% operating duty cycle is obtained by using a ping-pong structure. The offset compensation scheme is inherently time and temperature stable since the offset compensation is periodically performed with the ping-pong control. The proposed circuit has been fabricated using a 1.0  $\mu\text{m}$  *n* well CMOS process. The measured offset voltages of the test circuits are less than 400  $\mu\text{V}$  in magnitude.

## I. INTRODUCTION

IN many op-amp applications, offset cancellation or reduction is critical because an amplifier input offset voltage limits the capability of the system. An offset voltage of 10 mV to 30 mV is typical for CMOS amplifiers. This cannot be tolerated in many applications. For continuous-time integrated applications, a number of offset cancellation schemes have been reported [1]–[11]. Classical approaches to build low-offset MOS op-amps through device optimization are inefficient and have performance limitations. To obtain low offset, special circuit techniques are additionally required. Commonly used auto-zero techniques use analog switches and capacitors to implement low-offset amplifiers. The offset cancellation of these techniques is degraded by the charge injection due to the autozero switches. The schemes have 50% duty cycles making them unsuitable for continuous-time applications.

In this paper a digital correction technique is presented to keep the noise of the offset compensation circuit small. The objective is to compensate for inherent matching-induced offsets to achieve an op-amp with an offset voltage of less than 500  $\mu\text{V}$ . The proposed architecture is available to achieve even much lower offsets. A ping-pong architecture is employed to obtain a 100% duty cycle. With the ping-pong control the op-amp is capable of continuous-time operation, yet the offset is periodically adjusted making the offset compensation scheme insensitive to time and temperature drift. The scheme also requires no off-chip components and no adjustments during manufacturing. This compensation is obtained at the expense of modest extra chip area for the digital correction circuit.

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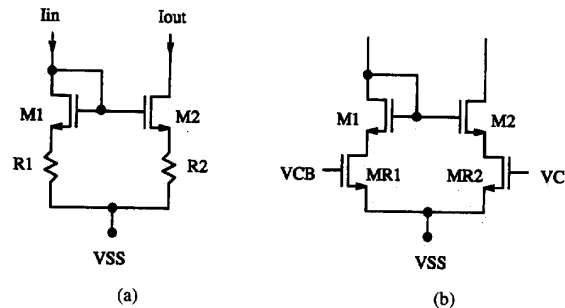


Fig. 1. Programmable current mirror biased with (a) resistors and (b) transistors.

The scheme is most practical, from an area viewpoint, for large chips where many low offset op-amps are required. In these applications the digital correction circuit can be used in common, thus the area required for the digital correction circuit comprises a small fraction of the total die area.

## II. OFFSET TUNING STRATEGY

To adjust offset the programmable current mirror shown in Fig. 1 is used as the load of the differential input stage. The current mirror gain of the programmable current mirror in Fig. 1(a) is given by:

$$A_i = \frac{I_{out}}{I_{in}} \approx \frac{g_{m2}}{g_{m1}} \left( \frac{1 + g_{m1}R_1}{1 + g_{m2}R_2} \right). \quad (1)$$

The current mirror gain can thus be adjusted or programmed by changing the resistor values. A variable resistor can be implemented with a MOS transistor which is biased to operate in a linear region as shown in Fig. 1(b). For the case of  $V_{DS} \ll V_{GS} - V_T$ , MR1 and MR2 behave as linear resistors of value:

$$1/R \approx \mu C_{OX} \left( \frac{W}{L} \right) (V_{GS} - V_T). \quad (2)$$

By changing the bias voltages VCB and VC, the resistor values and thus the current mirror gain can be adjusted.

The adjustable range of the current mirror gain varies with the device sizes of MR1 and MR2 as shown in Fig. 2. A small  $W/L$  increases the resistor value and thus increases the adjustable range of the current mirror gain which is directly related to the offset adjustable range of the op-amp. Therefore, the sizes of MR1 and MR2 should be selected according

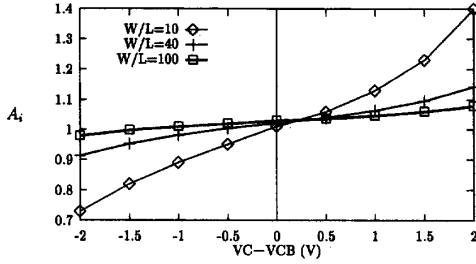


Fig. 2. Simulated current mirror gain adjustable range of the programmable current mirror in Fig. 1(b).

to the expected offset voltage range of the op-amp to be compensated.

These kinds of adjustable current mirrors have been used for auto-zero offset compensation [3], [4], where the op-amp output is fed back to a control port (e.g., VC) of a programmable current mirror during auto-zero periods, and the compensation voltage is stored on a capacitor to be utilized during signal processing periods. This analog scheme is very simple and requires a small area, but its performance is limited by two factors. First, the compensation voltage is actually the op-amp output offset which is small but cannot become zero. Secondly, the compensation voltage is contaminated by the charge injection of analog switches. Thus, there exists a limit of compensation at given supply voltages although it can be optimized by carefully selecting the op-amp gain and/or the gain from the control voltage to the op-amp output. The limit can be further reduced by using a compensation voltage generated from a digital correction circuit instead of one directly from the op-amp output. The digital scheme does not suffer from the charge injection problem. The performance of digital compensation is limited mainly by the resolution of the control voltages, and thus much smaller offset voltages are obtainable at the expense of more chip area.

Fig. 3 shows an offset adjustable two-stage CMOS op-amp with a programmable current mirror as the load of the input stage. The op-amp has been designed for high-speed and high-precision applications in a 1.0  $\mu\text{m}$  CMOS technology. Since the first stage has the dominant effect on the offset, the input referred offset voltage of the op-amp can be expressed as:

$$V_{OS,in} = V_{OSi} + V_{OSl} + V_{OSr} + V_{OS,sys} \quad (3)$$

where,  $V_{OSi}$ ,  $V_{OSl}$ , and  $V_{OSr}$  are the input referred random offset voltages due to the mismatches of the pairs (M1, M2), (M3, M4), and (MR1, MR2), respectively, and  $V_{OS,sys}$  is the systematic offset voltage. If  $VC = VCB$ , the systematic offset is usually small and can be reduced to a very small value by careful design. Clearly,  $V_{OS,sys}$  is a function of the bias voltage VC if VCB is fixed. For appropriate device sizes, there exists a certain value VC such that the total offset voltage  $V_{OS,in}$  is zero. The random offset voltage can thus be compensated by intentionally introducing an offsetting systematic offset voltage that is dependent upon VC.

Assuming  $VC = VCB$ , the random offset voltages  $V_{OSi}$ ,  $V_{OSl}$ , and  $V_{OSr}$  can be obtained as in [12]. The standard

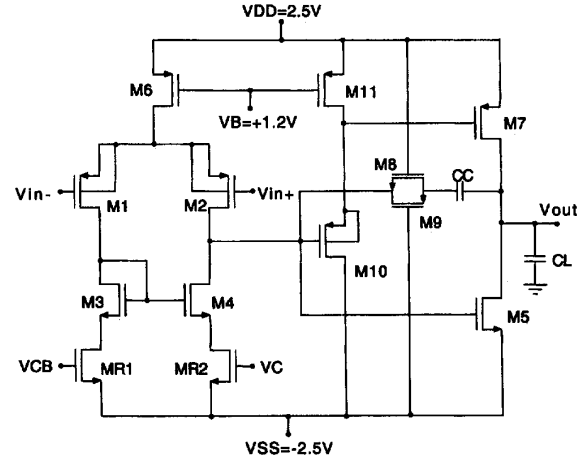


Fig. 3. Offset adjustable two-stage CMOS op-amp with a programmable current mirror.

deviation of the sum of  $V_{OSi}$ ,  $V_{OSl}$ , and  $V_{OSr}$  is given by:

$$\begin{aligned} \sigma_{V_{OS,in}} = & \frac{|V_{GSi} - V_{Ti}|}{\sqrt{2}} \left[ \sigma_L^2 \left( \frac{1}{L_i^2} + \frac{1}{L_l^2} + \frac{1}{L_r^2} \right) \right. \\ & + \sigma_W^2 \left( \frac{1}{W_i^2} + \frac{1}{W_l^2} + \frac{1}{W_r^2} \right) + \frac{4\sigma_{V_{Ti}}^2}{(V_{GSi} - V_{Ti})^2} \\ & \left. + \frac{4\sigma_{V_{Tl}}^2}{(V_{GSi} - V_{Tl})^2} + \frac{\sigma_{V_{Tr}}^2}{(V_{GSr} - V_{Tr})^2} \right]^{\frac{1}{2}}, \end{aligned} \quad (4)$$

where, the subscript  $i$  denotes the input transistors M1 and M2, the subscript  $l$  denotes the load transistors M3 and M4, and the subscript  $r$  denotes the transistors MR1 and MR2 used as resistors. The standard deviation of the input offset voltage of the op-amp in Fig. 3 can be calculated based on (4). In this calculation,

$$\sigma_L = \sigma_W = 0.014 \mu\text{m} \quad (5)$$

$$\sigma_{V_{Tr}} = \frac{0.0236}{\sqrt{LW}} \quad (6)$$

were used as in [12]. The designed transistor sizes,  $L_i = L_l = L_r = 1 \mu\text{m}$ ,  $W_i = 240 \mu\text{m}$ ,  $W_l = 86 \mu\text{m}$ , and  $W_r = 16 \mu\text{m}$ , and the simulated excess voltages,  $V_{GSi} - V_{Ti} = -0.626 \text{ V}$ ,  $V_{GSi} - V_{Tl} = 0.427 \text{ V}$ , and  $V_{GSr} - V_{Tr} = 3.753 \text{ V}$  were used for the calculation.

The calculated  $\sigma_{V_{OS}}$  is 12.2 mV. This is somewhat high due to the short channel lengths of the input-stage transistors. The minimum sizes of the channel lengths were selected to obtain the fast settling characteristics of the op-amp.

To obtain a 99.7% offset yield, the sizes of MR1 and MR2 will be determined such that the offset voltage of  $\pm 3\sigma_{V_{OS}}$  can be covered by adjusting VC. For the present design the ratio of (16/1) was selected to be more conservative for the achievable offset resolution. With this selection the offset adjustable range of the op-amp was simulated using a unity gain configuration. The results are shown in Fig. 4. An offset adjustable range

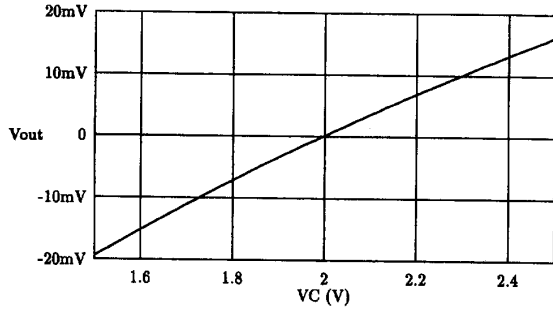


Fig. 4. Simulated offset adjustable range of the op-amp in Fig. 3. VCB is fixed to 2 V.

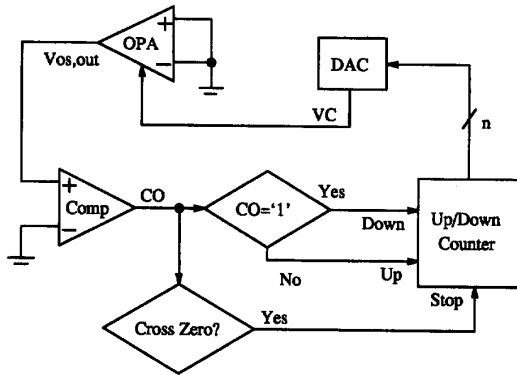


Fig. 5. Concept of the offset tuning scheme.

from  $-16.2$  mV to  $+19.6$  mV can be obtained by changing the bias voltage VC from 1.5 V to 2.5 V with VCB fixed to 2 V. This offset adjustable range which is equivalent to  $-1.33\sigma_{V_{OS}}$  to  $+1.61\sigma_{V_{OS}}$  leads to a 85.5% offset yield, provided the mean of the offset voltages is 0. The lower and upper limits of the bias voltage are determined by the reference voltages of the D/A converter (DAC) which will be discussed later. A wider adjustable range can be obtained by changing the DAC reference voltages, but the linearity will be degraded due to the nonlinearity of the NMOS resistors. The resolution will also be degraded by increasing the range of the DAC reference voltages at a fixed number of bits.

A simple way to find VC such that the total input offset voltage  $V_{OS,in}$  becomes zero is as follows:

1. The output voltage of the op-amp is compared to zero when both the input terminals are grounded.
2. The bias voltage VC of the transistor MR2 is adjusted in the direction of reducing the output offset voltage.
3. The procedure is repeated until the op-amp output voltage crosses zero.

This offset tuning strategy is depicted in Fig. 5. The up/down counter is initially set to half of full scale such that the DAC output VC is equal to the fixed bias voltage VCB. The performance of the offset reduction depends upon the resolution of the bias voltage VC and the offset of the comparator.

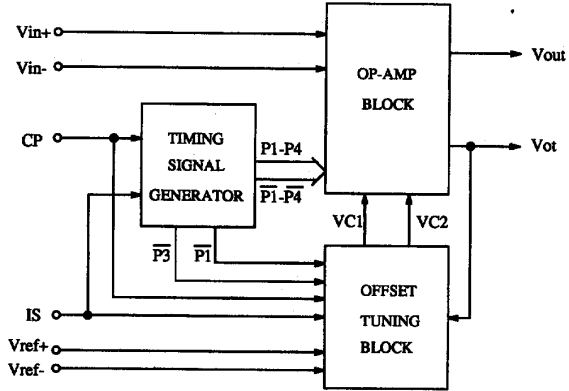


Fig. 6. Block diagram of the digitally offset compensated op-amp.

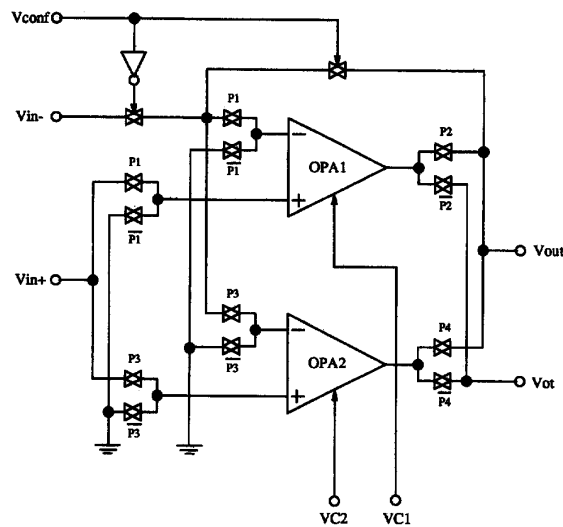


Fig. 7. Op-amp block diagram (ping-pong structure).

Fig. 6 shows a simplified block diagram of the entire offset compensated op-amp. It consists of three blocks: an op-amp block, a timing signal generator, and an offset tuning block. The op-amp block consists of two identical op-amps and several analog switches for ping-pong operation. The timing signal generator produces signals, P1-P4, to control the ping-pong structure. The offset tuning block will reduce the offset voltages of the op-amps by adjusting the bias voltages VC1 and VC2. Circuit details and functions of the blocks are presented in the following sections.

### III. OP-AMP BLOCK WITH A PING-PONG STRUCTURE

The op-amp block diagram is shown in Fig. 7. The block consists of two identically designed op-amps of Fig. 3 and several switches which are used for implementing a ping-pong structure. VC1 and VC2 are the bias voltages of the transistor MR2 of OPA1 and OPA2, respectively. One of the op-amps will be in a normal mode at any one time while the

TABLE I  
SIMULATED PERFORMANCE OF THE OP-AMP BLOCK OF FIG. 7.

Specification	Performance
Settling Time (-1 V to 1 V Step Input)	21.6 ns
0.2% Error Limit, $C_L = 1PF$	
Input Systematic Offset Voltage	160 $\mu V$
Open Loop Voltage Gain	700 (56.9 dB)
Unity Gain Frequency	113 MHz
Phase Margin	61°
Input Common Mode Range	$\pm 2.0$ V
Output Voltage Swing	$\pm 1.9$ V
Power Dissipation	45.9 mW
CMMR	56 dB

other is in an offset tuning mode. A 100% duty cycle can be obtained by interchanging their roles. The signal  $V_{conf}$  is used to configure the op-amps either in an open-loop or in a closed-loop with unity gain. The other switches are controlled by the timing signals, P1–P4, generated by the timing signal generator to achieve the ping-pong operation. A similar operation was introduced in [13], [14], where two identical resistors which are implemented with NMOS transistors biased in the ohmic region and capacitors are alternatively tuned to obtain accurate RC products for continuous-time filters. Simulated performance of the uncompensated op-amp block is shown in Table I. The SPICE simulation was performed with the circuit extracted from its layout.

Fig. 8(a) shows the timing diagrams of P1–P4. During the first phase, OPA1 processes the input signal while OPA2 is in the offset tuning mode. A phase is defined here as the time duration from the moment that two op-amps interchange their roles to the next interchanging moment. Each phase consists of  $2^{n-1}$  (128 for  $n = 8$ ) clock (CP) periods. The offset tuning block uses  $V_{ot}$  which is the output offset voltage of OPA2 at this time to generate an offset control signal VC2. When the op-amps interchange their roles, P3 first goes to high at the 128th CP falling edge, such that the signal input is also connected to OPA2. After that, other three timing signals, P1, P2, and P4 change their states after one CP period. At this time the transient in OPA1 is used for tuning does not affect the tuning process because updating the bias voltage VC1 is made after one clock period, and the one clock period is made long enough for the op-amp to finish its transient.

An expected offset voltage waveform is shown in Fig. 8(b). During the reset (when the signal "IS" is "0") the states of the four timing signals are (P1, P2, P3, P4) = (1, 0, 1, 1), and thus, the output of the op-amp block  $V_{out}$  will be the initial uncompensated output offset voltage of OPA2 if the inputs are grounded. Of course, the magnitude of the offset voltage depends on the configuration of the op-amp. During the first phase, i.e., (P1, P2, P3, P4) = (1, 1, 0, 0),  $V_{out}$  will be the uncompensated output offset voltage of OPA1, and the offset of OPA2 is compensated by the offset tuning circuit. Therefore, during the second phase (P1, P2, P3, P4) = (0, 0, 1, 1), the compensated offset voltage of OPA2 will appear at the output while the offset of OPA1 is being adjusted. The compensated offset voltage of OPA1 can be thus found during the third phase. In the following phases only the changes of the offset due to the temperature and time drift will be compensated.

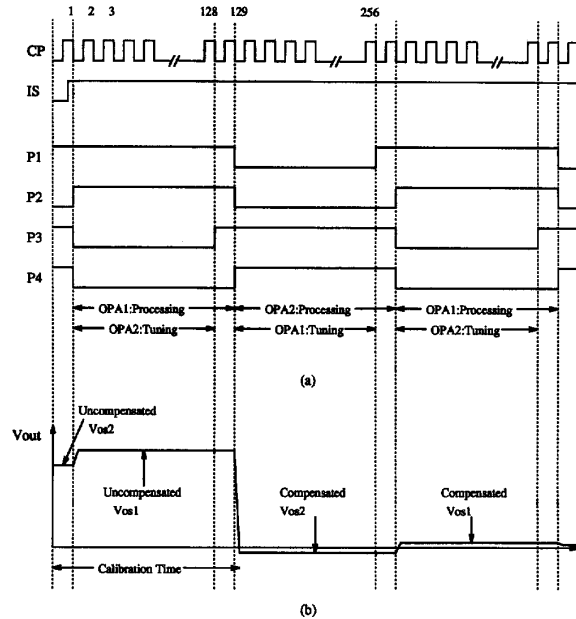


Fig. 8. (a) Timing diagram of the ping-pong structure. (b) An expected offset voltage waveform of the op-amp block.

The compensated offset voltages of the two op-amps can be different from each other, so the equivalent offset voltage of the op-amp block after calibration can be defined by:

$$V_{OSeq} = \max\{|V_{OS1}|, |V_{OS2}|\}. \quad (7)$$

The ping-pong operation makes it possible that the op-amp can operate in a continuous-time mode while the offset voltages are kept small after the calibration time that corresponds to 128 CP periods. The temperature drift of the offset voltages can be also compensated by the ping-pong operation.

Fig. 9 shows the simulated output delay of the op-amp block when VC is changed. The initial output voltage of the open-loop op-amp block was assumed to be 0.114 V which is due to the systematic input offset voltage. The random offset was not considered. To reduce the offset, VC was decreased from 2 V to 1.996 V at  $t = 1 \mu s$ . The step, about 4 mV, corresponds to the resolution of the DAC, i.e., 1LSB of eight-bit. The VC change causes the reduction of the output voltage, and thus, the input offset voltage. The delay time of the op-amp block with respect to the VC change is about 5  $\mu s$ . Thus, one CP period must be longer than the delay time to correctly update the bias voltage VC.

#### IV. OFFSET TUNING BLOCK

The block diagram of the offset tuning block is shown in Fig. 10. It consists of a comparator, a zero crossing detector (ZCD), two eight-bit up/down counters (UDC block), and two small eight-bit D/A converters (DAC). This block detects the output voltage  $V_{ot}$  of the op-amp to be tuned and then provides an updated bias voltage VC1 for OPA1 and VC2 for OPA2 such that the offset voltages are reduced. The timing signals,  $\overline{P1}$  and  $\overline{P3}$ , generated from the timing signal generator

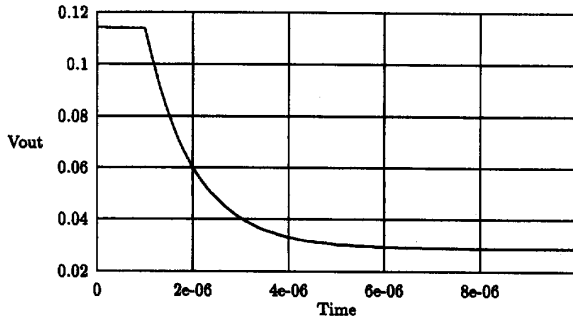


Fig. 9. Output delay of the op-amp block with respect to VC change.

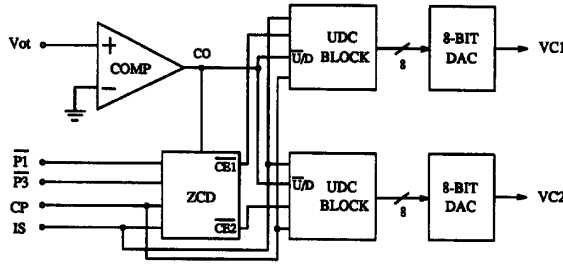


Fig. 10. Block diagram of the offset tuning block.

determine which op-amp will be tuned, so only one of the two up/down counters is enabled to count. The counters are initially set through the signal  $IS$  to half of full scale. This is done to accommodate for the inherent bipolarity of the offset voltages.

If the comparator output is high, indicating that the offset is greater than zero, then the down signal of the up/down counter is set to "1," so that the counter counts down to decrease the bias voltage  $VC$ . The current mirror gain of the programmable current mirror is then decreased, and the op-amp output voltage is also decreased, i.e., the offset voltage is reduced. As long as the comparator output does not change, this procedure is repeated until  $\overline{P1}$  or  $\overline{P3}$  is changed. If the comparator output goes to "0" before the phase is changed, then the zero crossing detector detects this change and sets the count enable signal  $CE$  to "0" to prevent the op-amp output from oscillating. A change of the comparator output means that the op-amp output crosses zero, and the minimum offset is achieved. Thus, no further update of the bias voltage is required.

A. Digital-to-Analog Converter

A simple  $R$  and  $2R$  resistor ladder network shown in Fig. 11 is used for an eight-bit DAC. The resistor ladder is implemented by PMOS transistors with the  $W/L$  ratios of  $2/5$  for  $R$  and  $2/10$  for  $2R$ . The ratio of the PMOS transistors used for the decoding switches is  $10/1$ . The binary signals  $D0$ – $D7$  are the outputs of the up/down counter. One advantage of this simple structure is that the area is very small compared to other structures and increases only linearly with the number of bits. For the proposed offset compensation scheme the DAC does not require excellent linearity because some degree of nonlinearity can be tolerated unless the resolution is significantly

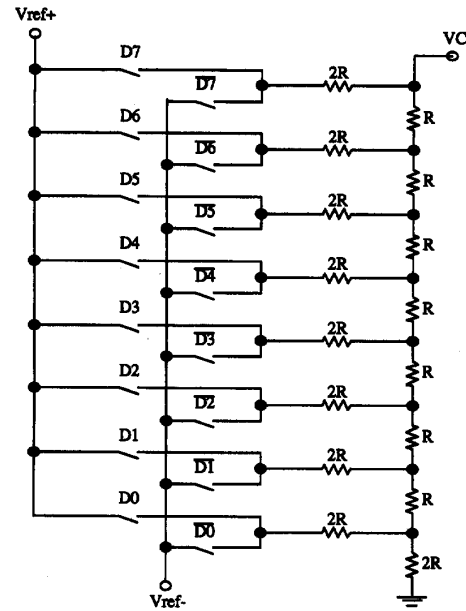


Fig. 11.  $R$  and  $2R$  resistor ladder eight-bit D/A converter.

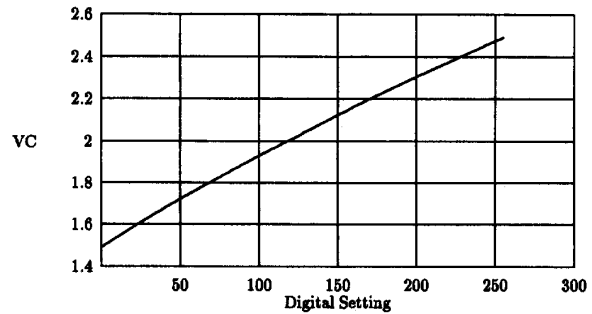


Fig. 12. Simulated DAC output voltages at 256 digital settings ( $V_{ref+} = 2.5$  V and  $V_{ref-} = 1.5$  V).

degraded. Even nonmonotonicity in the DAC can be tolerated. Nonlinearity and nonmonotonicity result in minor degradation of the resolution without affecting the correct operation of the offset compensation. The simple structure has been chosen to keep the area small.

The simulated output voltages of the designed DAC at different digital settings are shown in Fig. 12, where  $V_{ref+} = 2.5$  V and  $V_{ref-} = 1.5$  V. The simulated result shows that the DAC has the expected nominal nonlinear characteristics. The DAC output voltage at digital setting 128 is 2.04 V instead of 2.0 V due to the nonlinearity. Fig. 4 shows that the op-amp output also exhibits a modest nonlinear relationship between the bias voltage of the programmable current mirror and the offset voltage. Due to the nonlinearity of both the DAC and the programmable current mirror the simulated worst-case resolution is 0.22 mV when the offset adjustable range is  $-16.2$  mV to  $+19.6$  mV, which is degraded from the theoretical resolution of 0.14 mV ( $=35.8$  mV/256) but satisfies the targeted resolution of  $500 \mu V$ .

The resolution can be readily improved by increasing the number of bits of the DAC and the up/down counters at the cost of a small increase in die area. If a ten-bit DAC is used, then a theoretical resolution of  $35 \mu\text{V}$  ( $=35.8 \text{ mV}/1024$ ) can be obtained at the cost of two more flip-flops for a counter and eight more PMOS transistors for a DAC. Another way to improve the resolution is to reduce the range of the DAC reference voltages. This will, however, reduce the offset adjustable range.

### B. Comparator

A simple two-stage comparator with the output buffered is employed to compare the op-amp output offset voltage to zero. The designed device sizes are  $W_i/L_i = 28/2$  and  $W_l/L_l = 9/4$ . The standard deviation of the random offset voltage of the designed comparator was calculated based on (4), resulting in  $\sigma_{V_{OS}} = 6.5 \text{ mV}$ . This comparator offset voltage can be tolerated because the op-amp in an offset tuning phase is in an open-loop configuration (see Fig. 7), and thus, the output offset voltage preserved at the input of the comparator is 700 (the open-loop gain) times greater than the input offset voltage of the op-amp. Since eight-bit DAC's are used for the present design, and the simulated resolution of the offset adjustment is 0.22 mV, the minimum output voltage of the op-amp which must be resolved by the comparator is 154 mV ( $0.22 \text{ mV} \times 700$ ) which is much greater than the comparator offset voltage. Thus, only a small fraction of the comparator input offset which is the comparator input offset voltage divided by the open-loop gain of the op-amp will contribute to degradation in the achievable offset resolution.

## V. EXPERIMENTAL RESULTS

The test circuit was fabricated in a  $1.0 \mu\text{m}$   $n$  well CMOS process. The chip photomicrograph is shown in Fig. 13. The total circuit area excluding pads is  $0.99 \text{ mm}^2$ . The op-amp block occupies 14.7% of the total area, and the comparator and the two DAC's occupy 0.84% and 2.12%, respectively. The remaining 82.3% is for the digital control circuits and connections. The extra large area of the digital section can be compensated somewhat by using it in common for several op-amps. One simple example is to use time sharing operation. For the case of using two op-amp blocks, only one up/down counter can be used along with four DAC's by including latches before DAC's, and other blocks can remain unchanged. With additional multiplexing circuits and connections for time sharing operation, one digital tuning circuit can serve for two op-amp blocks such that two among four op-amps are always available for signal processing while one of the remaining two op-amps is in an offset tuning mode. This scheme can be extendable for circuits including more op-amp blocks.

The CP frequency is set to 46.9 kHz ( $T_{CP} = 21.3 \mu\text{s}$ ). The period of one phase is thus,

$$T_p = 128T_{CP} = 2.73 \text{ ms}.$$

A closed-loop configuration with a gain of 100 is used to characterize the offset voltage waveform of the op-amp block. The closed loop configuration is obtained by connecting two

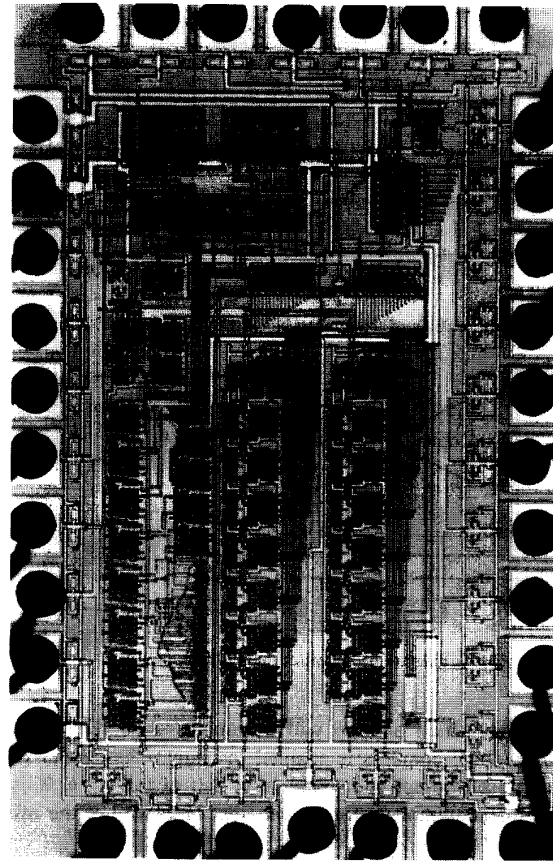
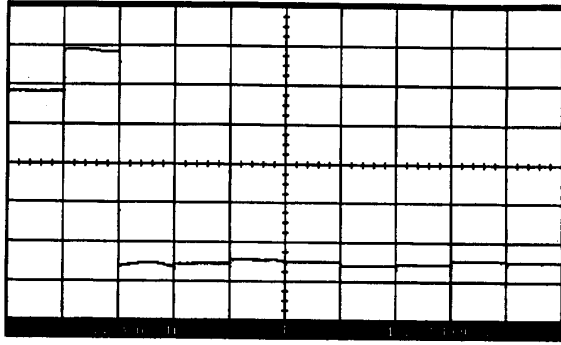


Fig. 13. Chip photomicrograph.

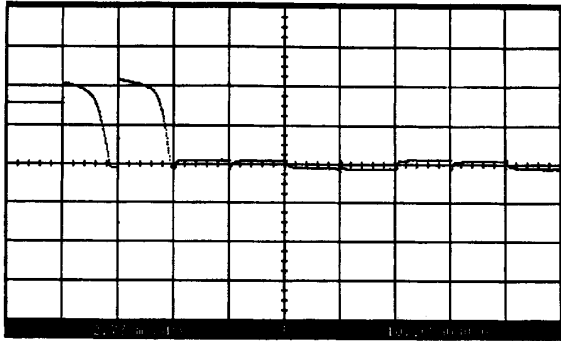
resistors ( $R1 = 1 \text{ K}\Omega$  and  $R2 = 100 \text{ K}\Omega$ ) around the inverting input terminal, when the signal " $V_{conf}$ " in Fig. 7 is set to "0." With the inputs grounded 100 times the input offset voltage will appear at the output terminal  $V_{out}$ . In this case a periodic square waveform that is generated from a function generator is used for the reset ("IS") signal, and this serves as a triggering signal to help an oscilloscope catch the nonperiodic offset voltage waveforms more easily.

### A. Measured Offset Waveforms

A typical output offset waveform measured from one of the test chips is shown in Fig. 14(a). The waveform was obtained from the closed-loop feedback amplifier in the gain of 100 configuration. The reset signal is changed from "0" to "1" at  $t = 2.73 \text{ ms}$  when  $t = 0$  is referenced to the left edge of the trace. The horizontal scale is 2.73 ms/div which is the period of one phase  $T_p$ . The vertical scale is 200 mV/div, and the vertical axis offset is 500 mV. It can be seen that the measured offset waveform is very similar to the expected waveform shown in Fig. 8(b). The first two high states are due to the uncompensated offset voltages of OPA2 and OPA1, respectively. The following low states are the compensated offset voltages. The initially uncompensated



(a)



(b)

Fig. 14. (a) Output offset waveform measured at  $V_{out}$  with the op-amp having a closed-loop gain of 100 (VS: 200 mV/div, offset: 500 mV). (b) Output offset waveform measured at  $V_{ot}$  which is the output offset voltage of the open-loop op-amp being adjusted (VS: 1 V/div, offset: 0 V).

input offset voltages and the compensated offset voltages can be obtained from the plots by dividing the output voltages by the closed-loop gain of 100.

By connecting  $V_{ot}$  (see Fig. 7) instead of  $V_{out}$  to the oscilloscope input, the offset compensation process can be observed more clearly because  $V_{ot}$  is the output offset voltage of the open-loop op-amp being tuned, and this signal is compared with zero by the comparator and finally reduced by the offset tuning circuit. The measured  $V_{ot}$  is shown in Fig. 14(b). From the plot it can be seen that the initial uncompensated large offset voltages of OPA2 and OPA1 are reduced significantly during the first and second phases, respectively. It can be also seen that because of the large uncompensated input offset voltages and the large open-loop gains of the op-amps, the outputs of the open-loop op-amps initially saturate.

During the first phase the initial offset voltage of OPA2 is continuously decreased, and the offset compensation is stopped when the offset crosses the zero line. Thus the offset sits at a small negative level. In the next OPA2 tuning phase, i.e., the third phase, the tuning circuit detects the negative polarity of the offset and starts to adjust the offset toward the positive direction. After the initial tuning, a single one-

step adjustment (1LSB change of the DAC) is usually enough to make the offset cross the zero line. The zero crossing detector then makes the adjustment stop. This process is repeated in the following tuning phases. Therefore, each op-amp will have two compensated offset levels, i.e., one is positive and the other is negative as shown in Fig. 14(b). Thus, the compensated op-amp will have bipolar offset voltages. Unipolar offset compensation and correspondingly an overall decrease in offset voltages can be readily obtained by slightly modifying the control logic (the zero crossing detector block) such that compensated offset voltages approach the zero crossing from the same direction during each phase. Doing this, the compensated offset variation will be substantially reduced, and the corresponding offset voltages are reduced by a factor of two.

### B. Offset Compensation Results

The compensated offset voltages are measured from  $V_{ot}$  by expanding the vertical scale and dividing the values by the measured open-loop gain. This will be more accurate for small offset voltages than measurements from a feedback amplifier at  $V_{out}$  because of the large open-loop gain. The measured open-loop gains are between 400 and 700. The initial large offset voltages were, however, measured from  $V_{out}$  using closed-loop configurations with proper closed-loop gains which were selected low enough to guarantee that the op-amp outputs do not saturate.

Of 13 chips tested, three showed initial offset voltages outside the compensatable range. This can be expected because of the low designed offset yield as mentioned in Section II. The measured initial offset voltages and the compensated final offset voltages are shown in Table II. Since each op-amp has two compensated offset levels as mentioned above, the greater one in magnitude is reported in the table. The table shows that most op-amp initial offset voltages are biased in the positive direction. This suggests a small wafer-level and/or die-level systematic offset.

All compensated offset voltages are less than  $400 \mu\text{V}$  in magnitude which met our design specification of  $500 \mu\text{V}$ . These offsets are, however, somewhat degraded from the simulated resolution of  $220 \mu\text{V}$ . The degradation is attributable, in part, to the systematic offset which causes the final steps of the offset control voltage VC to be placed around the lower left corner of the curve in Fig. 4 where the resolution is degraded. The nonlinearity of the fabricated circuit may be more severe than the simulated one. The comparator offset also partially contributes to the degradation in offset voltages.

Although the resolution can be improved by a more careful layout, the systematic offset can be reduced, and the variations of the random offset voltages can be reduced by using a more linear portion of the plot in Fig. 4, an easier way to improve the resolution without reducing the offset adjustable range is to increase the number of bits of the DAC. In this case the comparator offset will ultimately become the dominant factor limiting resolution. Further improvement with higher-bit DAC's can be achieved by compensating the comparator offset.

TABLE II  
MEASURED INITIAL AND COMPENSATED OFFSET VOLTAGES.

#		Initial $V_{OS}$	Final $ V_{OS} $	#	Initial $V_{OS}$	Final $ V_{OS} $	
1	OPA1	9.9 mV	157 $\mu$ V	2	OPA1	15.0 mV	150 $\mu$ V
	OPA2	8.9 mV	191 $\mu$ V		OPA2	11.2 mV	309 $\mu$ V
3	OPA1	-6.3 mV	219 $\mu$ V	4	OPA1	9.5 mV	395 $\mu$ V
	OPA2	2.4 mV	97 $\mu$ V		OPA2	11.6 mV	318 $\mu$ V
5	OPA1	8.0 mV	72 $\mu$ V	6	OPA1	5.0 mV	245 $\mu$ V
	OPA2	6.3 mV	158 $\mu$ V		OPA2	2.3 mV	57 $\mu$ V
7	OPA1	-370 $\mu$ V	172 $\mu$ V	8	OPA1	8.4 mV	102 $\mu$ V
	OPA2	8.5 mV	261 $\mu$ V		OPA2	7.4 mV	185 $\mu$ V
9	OPA1	13.8 mV	313 $\mu$ V	10	OPA1	590 $\mu$ V	299 $\mu$ V
	OPA2	12.6 mV	163 $\mu$ V		OPA2	1.5 mV	269 $\mu$ V

TABLE III  
EFFECTS OF OFFSET COMPENSATION ON THE CMRR AND PSRR'S.

	$(L_1 - L_2) / (L_3 - L_4)$	$VC$	$V_{OS}$	CMRR (dB) at 1 MHz	PSRR + (dB) at 1 MHz	PSRR- (dB) at 1 MHz
Case	0/0	2 V	39 $\mu$ V	55.4	33.4	32.4
1	0.01/(0.01)	2 V	-7.3 mV	54.6	33.4	32.5
Case	0.01/(-0.01)	2.22 V	84 $\mu$ V	58.1	33.2	33.6
1	(0.01)/0.01	2 V	7.7 mV	56.4	33.3	32.3
Case	(0.01)/0.01	1.795 V	91 $\mu$ V	53.4	33.6	31.2

### C. Effects on CMRR and PSRR

The effects of offset compensation on the CMRR and PSRR's have been simulated. The simulated results are shown in Table III. The process variation of matched devices were simulated by using different device sizes. These mismatch components resulted in offset voltages of  $-7.3$  mV for Case 1 and  $7.7$  mV for Case 2 while the systematic offset is  $39$   $\mu$ V. The mismatch components also affect the CMRR, but their effects on the PSRR's are negligible. It can be seen that the CMRR can be improved or degraded by compensating the offset voltages due to the device mismatch. It is also seen that the CMRR variation due to the offset compensation process is not significant, and the PSRR variation is negligible.

### D. Transient Characteristics

In many applications there are brief periods of time where the amplifier need not be operational, and in such applications the transient responses associated with switching the op-amp from the compensation state into the application state are not of concern since this switching can occur during these brief periods. Furthermore, the re-compensation rate can be very small ranging from minutes to days on even weeks in many environments. The effects of this switching transient even in true continuous operation are, however, very small.

The measured transient characteristics due to the ping-pong operation are shown in Fig. 15. The upper waveform of Fig. 15 (a) and (b) was used as the triggering signal which will be denoted as  $S_T$ , where

$$S_T = \overline{P1} \cdot P3.$$

Therefore, as can be seen in Fig. 8(a), the period of  $S_T$  is  $128T_{CP}$ , and the duration of  $S_T = '0'$  is  $T_{CP}$ . At time A the

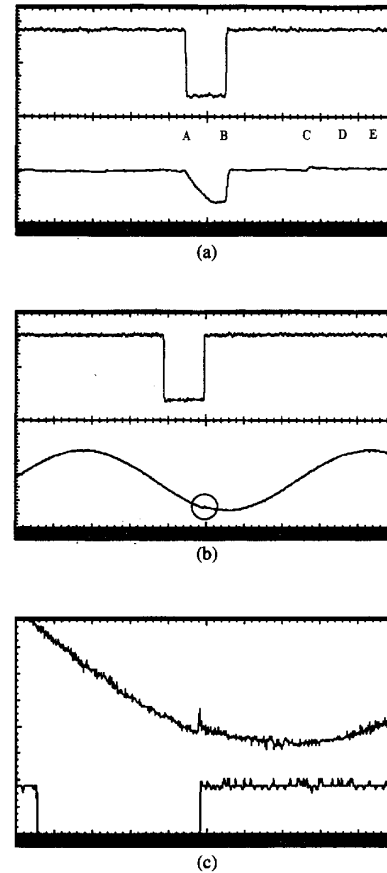


Fig. 15. Measured transient characteristics. (a) Output offset voltage measured at  $V_{ot}$  (lower trace,  $VS: 500$  mV/div). (b) Output signal measured at  $V_{out}$  when the op-amp is in a closed-loop configuration with a gain of 33 (lower trace,  $VS: 500$  mV/div). (c) Magnified plot of (b) (upper trace,  $VS: 200$  mV/div, offset:  $-1.24$  V). The triggering signal  $S_T$  is the upper trace of (a) and (b) and the lower trace of (c) ( $VS: 1$  V/div).

inputs of the op-amp which have been connected to ground for offset tuning are switched to the input signal. After one CP period the two op-amps interchange their roles completely at time B.

The lower waveform of Fig. 15(a) is  $V_{ot}$  which is the output of the op-amp in an offset tuning mode. The waveform  $V_{ot}$  exhibits the compensated output offset voltage of one op-amp until time A and shows the output offset of the other op-amp after time B. It can be seen that since the compensation of the op-amp which is in a new tuning phase is started after one CP period as mentioned in Section III, the offset adjustment can be observed at time C which is two CP periods after time B. It can be also seen that no further offset adjustment is observed at the following CP falling edges such as time D and E since the offset crossed the zero line at time C, and after calibration a single one-step adjustment is usually enough to make the offset cross the zero line.

The lower waveform of Fig. 15(b) was measured at  $V_{out}$  when the op-amp block was in a closed-loop configuration with a gain of 33 and a sinusoidal input was applied. The high-gain configuration was used to examine the transient



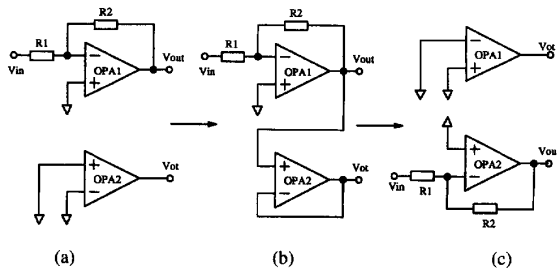


Fig. 16. An example switching process to reduce the transient effects due to the ping-pong operation. (a) OPA1: signal processing, OPA2: offset tuning. (b) OPA2 tracks the output signal of OPA1 during  $S_T = "0."$  (c) OPA1: offset tuning, OPA2: signal processing.

characteristics more clearly. With low-gain configurations the transients were hardly observed. The output transients can be observed inside the circle on Fig. 15(b). Fig. 15(c) is a magnified plot of the circle on Fig. 15(b). The displacement of the output signal is due to the difference between the offset voltages of two op-amps. This displacement can be greatly reduced by using the unipolar offset compensation scheme as mentioned before.

From the experimental results it can be seen that the transient energy in the output due to the ping-pong operation is not significant. The transient energy can be further reduced if the following schemes are incorporated with the current structure:

1. Modifying the switching process such that the output of the op-amp to be used for signal processing follows the output of the op-amp which is currently being used. This can be done by connecting the output  $V_{out}$  with the input of the op-amp in a unity-gain configuration as shown in Fig. 16. This tracking process can be done during  $S_T = "0."$
2. Reducing the CP frequency greatly after the first two tuning phases. This can be readily obtained by modifying the control logic.
3. Disabling the ping-pong operation after the initial power-up calibration and enabling only on demand. This will also reduce the digital noise associated with the clock pulse CP.

Using these schemes, the transients will be almost negligible, and continuous-time operation can be achieved without any significant dynamic range loss.

## VI. CONCLUSION

An automatic digital offset correction method for continuous operation CMOS op-amps has been presented. A programmable current mirror is used to adjust the offset voltage. A ping-pong structure is employed to obtain a 100% duty cycle while the offset voltage is constantly kept small. The proposed offset compensation is not sensitive to time and temperature drift. Experimental results show that the designed op-amps can be digitally adjusted to have input offset voltages of less than  $400 \mu\text{V}$  in magnitude. The resolution can be substantially improved by increasing the number of bits of

the DAC, doing layout more carefully, using a unipolar offset compensation scheme, and employing an offset compensated comparator. Experimentally measured transients due to the ping-pong operation are not significant. Several schemes have been proposed to further reduce the transient effects.

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