

# An Accurate and Matching-Free Threshold Voltage Extraction Scheme for MOS Transistors

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## Abstract

An accurate threshold voltage extraction scheme for MOS transistors is presented. The scheme differs from alternative methods recently reported in the literature in that it does not require matched replica of the transistor under test and thus can be applied more effectively and accurately to real-time on-chip applications where threshold voltage measurements are required for many transistors with various geometries and bias conditions. The proposed scheme is accurately implemented in a matching-free way using a ratio-independent switched-capacitor subtracting amplifier and a dynamic current mirror. Nonideal effects associated with these circuits are investigated.

## Introduction

Numerous numerical techniques exist for accurately extracting device model parameters from measured data [1],[2]. One example of such a technique is the MOS transistor threshold voltage ( $V_T$ ) extraction using a linear regression on measurements of  $I_{DS}$  at many  $V_{GS}$  values. Some applications require real-time on-chip parameter extraction for implementing useful circuit functions. The numerical techniques discussed above are computationally intense and not well-suited for real-time on-chip applications.

Recently, several real-time  $V_T$  extraction methods based on circuit implementations have been proposed for overcoming the above disadvantages [3]-[6]. These methods are very fast and have ample applications although the accuracy is degraded compared to that attainable by the numerical methods. Most methods [3]-[5] require matched devices to extract  $V_T$  for one test device of a fixed geometry. Their accuracy thus depends on the matching between the devices under test. These methods are inefficient when extraction of  $V_T$  is required for many transistors with various geometries including small sizes since the matching of small-size transistors is poorer than that of large transistors. These methods also require other component matching in their extraction circuits such as current mirror transistors and resistors. Their mismatches will also degrade the accuracy of the extracted  $V_T$  values. Moreover, the methods [3],[4] are not applicable for transistors with different bias conditions, i.e., nonzero substrate-to-source voltages ( $V_{BS} \neq 0$ ) since they need a cascode configuration of matched test-transistors or transistor arrays. The method discussed in [6] uses only one test device and thus does not require device matching. The method is very simple but produces relatively large errors (about 100mV) due to the uncertainty of choosing the proper threshold current which is used to measure  $V_T$ .

In this paper an accurate matching-free  $V_T$  extraction scheme is presented which does not require any replica of the device under test and applicable for transistors with different geometries and different substrate bias conditions. The features of the proposed scheme is comparatively summarized in Table 1 with other extraction schemes mentioned above.

## Principle of the Matching-Free $V_T$ Extractor

### Basic Scheme

A conceptual schematic of the proposed  $V_T$  extraction scheme is depicted in Fig.1. Applying the outputs of a current mirror  $I_{D1}$  (with S1 closed and S2 open) and  $I_{D2}$  (with S1 open and S2 closed) to a test transistor which operates in the saturation region and assuming that the transistor has square-law characteristics, we obtain respectively

$$K(V_{GS1} - V_T)^2 = I_{D1} \quad (1)$$

$$K(V_{GS2} - V_T)^2 = I_{D2} \quad (2)$$

where

$$K = \frac{\mu C_{OX}}{2} \frac{W}{L}, \quad I_{D2} = nI_{D1}$$

Equation (1) and (2) have the same  $K$  and  $V_T$  because only one test transistor is used as contrasted with other extraction schemes. Solving these equations we readily obtain the threshold voltage  $V_T$

$$V_T = \frac{1}{\sqrt{n} - 1} (\sqrt{n}V_{GS1} - V_{GS2}) \quad (3)$$

Assume S1 and S2 are driven by a complimentary nonoverlapping clock. When S1 is closed,  $V_{GS1}$  is sampled and multiplied by  $p$ . When S2 is closed,  $V_{GS2}$  is sampled and subtracted from  $pV_{GS1}$ . The result is then multiplied by  $q$ . The output voltage  $V_{out}$  of Fig.1 is then

$$V_{out} = q(pV_{GS1} - V_{GS2}) \quad (4)$$

Comparing (3) with (4), it can be seen that the output voltage will be

$$V_{out} = mV_T$$

if  $p$  and  $q$  are given by

$$p = \sqrt{n}, \quad q = m/(\sqrt{n} - 1)$$

Thus, an integer multiple of  $V_T$  can be readily obtained by choosing an integer  $m$ . The easiest way to obtain  $V_T$  is to choose  $n = 4$  and  $m = 1$  resulting in  $p = 2$  and  $q = 1$  and thus,

$$V_{out} = 2V_{GS1} - V_{GS2} = V_T$$

where  $V_{GS1}$  and  $V_{GS2}$  are the gate-to-source voltages of the test-transistor when the drain currents are  $I_D$  and  $4I_D$ , respectively.

Most common implementations of the current mirror and the switched-capacitor amplifier require device and capacitor matching respectively although matching with the device under test is not required. Since both the current mirror gain and the amplifier gain are small and integral, both blocks can be dynamically implemented without requiring any matching of devices or capacitors. The implementation of the blocks will be discussed.

### Model Error Consideration

As are most other methods [3]-[5], the proposed  $V_T$  extraction scheme is also based on the assumption that MOS transistors operating in the saturation region obey the square-law. The characteristics of real MOS transistors, however, deviate from the square-law due to the nonideal effects such as channel-length modulation and mobility degradation, resulting in a discrepancy between the extracted  $V_T$  and a real  $V_T$ . Including the nonideal effects, the drain current can be described by

$$I_{DS} = \left[ \frac{\mu_o}{1 + \theta(V_{GS} - V_T)} \right] \left[ \frac{1}{L(1 - \lambda V_{DS})} \right] \frac{C_{OX}W}{2} (V_{GS} - V_T)^2 \quad (5)$$

where  $\lambda$  is the channel-length modulation parameter,  $\theta$  is the mobility degradation parameter, and  $\mu_o$  is the zero-field mobility of carriers.

The error voltage due to the  $\lambda$  and  $\theta$  effects can be readily derived using equation (5) and neglecting the second order effects, resulting in

$$V_{T_{err}} = \frac{1}{2}(\lambda - \theta)V_{ex1}V_{ex2} = \frac{1}{4}(\lambda - \theta)V_{ex2}^2 \quad (6)$$

where  $V_{exi}$  for  $i = 1, 2$  is the excess voltage  $V_{GSi} - V_T$ . Small excess voltages will help reducing the error voltage, which is an expected result because the  $\lambda$  and  $\theta$  effects increase with  $V_{DS}$  and  $V_{GS}$ , respectively, and the test device in our extractor is diode-connected to guarantee its saturation-region operation, resulting in  $V_{DS} = V_{GS}$ . It is interesting to note that the two parameters

in (6) are in a relation of canceling each other, and fortunately, both parameters are inversely proportional to the channel length. Therefore, the variance of  $\lambda - \theta$  and thus the error voltage will not increase substantially with the channel length reduction. For example, if the maximum difference value of the two parameters is  $0.1V^{-1}$ ,  $V_T = 0.8V$ , and  $V_{ex2} = 0.4V$ , then the error voltage will be less than 0.5%.

The proposed scheme has been simulated for two test devices which have different geometries using SPICE with level 2 MOS models ( $V_{TO}=0.924V$ ). In this simulation, no error associated with the current mirror and the analog arithmetic block was assumed to examine the pure model error. With assumption that the  $V_{TH}$  computed by SPICE is the actual threshold voltage, the error voltage  $V_{T_{err}}$  ( $V_{T_{ex1}} - V_{TH}$ ) is plotted in Fig.2 as a function of the excess voltage  $V_{ex2}$  ( $V_{GS2} - V_{TH}$ ). As expected, the error voltages increase with  $V_{ex2}$ , and the error for the long-channel device ( $W/L=200\mu m/40\mu m$ ) is smaller than that for the short-channel device ( $W/L=20\mu m/4\mu m$ ). The figure exhibits that the error variance of the proposed scheme to the excess voltage  $V_{ex2}$  is comparable with the variance to the device size. It can be also seen that the slope of the curves changes substantially at a small  $V_{ex2}$  that corresponds to the transition point between the strong inversion region and the weak inversion region. Therefore, the bias current  $I_D$  should be selected carefully such that the excess voltages  $V_{ex1}$  and  $V_{ex2}$  are greater than the transition point but not too big for small model error. It can be seen in Fig.2 that if  $V_{ex2} \leq 0.4V$  than the error voltage due to the model error will be less than 5mV even with the short-channel device ( $L=4\mu m$ ).

The proposed scheme has also been compared with the linear regression (LR) method [2] in Table 2. In the LR method,  $I_{DS}$  values are collected at 20  $V_{GS}$  values using SPICE, so no measurement error is assumed. For consistency in excess voltages, the  $V_{GS}$  values are selected such that the highest sample value  $V_{GS_h}$  is  $V_{GS2}$ , and the lowest sample value  $V_{GS_l}$  is  $V_{GS1}$ . Since threshold voltages are functions of device terminal voltages, and their variance increases as the device size decreases, the actual threshold voltage  $V_{TH}$  of the short-channel device ( $L=4\mu m$ ) computed by SPICE varies with  $V_{GS}$  or  $V_{DS}$  as shown in the table. At  $V_{GS} = 1.066V$ ,  $V_{TH} = 0.889V$ , while at  $V_{GS} = 1.525V$ ,  $V_{TH} = 0.887V$ . Thus, the  $V_{TH}$  variation is about 2mV when the  $V_{GS}$  change is 0.46V. This variation will be significant for shorter-channel devices. The  $V_{TH}$  variation of the long-channel device ( $L=40\mu m$ ) is almost negligible. In the proposed scheme the variation is due to the two different  $V_{GS}$  values,  $V_{GS1}$  and  $V_{GS2}$ , and in the LR method the variation is also due to the different  $V_{GS}$  values used to grab the  $I_D$  data. Thus, the average values

$$V_{TH_{av}} = \begin{cases} (V_{TH}(V_{GS1}) + V_{TH}(V_{GS2}))/2 & \text{for the proposed} \\ (V_{TH}(V_{GS1}) + V_{TH}(V_{GS_h}))/2 & \text{for the LR method} \end{cases}$$

were used to calculate the error of extracted threshold voltages. It can be seen from the table that the accuracy of the LR method is similar to that of the proposed scheme, and the LR method also gives large error when the samples are taken from large  $V_{GS}$  values.

### Ratio-Independent SC Subtracting Amplifier

The simple arithmetic ( $2V_{GS1} - V_{GS2}$ ) needed in our  $V_T$  extractor is realized using a SC circuit. Many circuit techniques and strategies [7]-[9] have been proposed to overcome the nonideal effects limiting the performance of SC circuits such as parasitic capacitances, nonzero offset voltage of op-amps, finite dc gain of op-amps, capacitor mismatches, and charge injection of MOS switches. To implement the SC circuit in a matching-free way and to relax the op-amp gain requirement, Lee's ratio-independent concept [8] and Nagaraj's gain-insensitive technique [9] are employed in our SC subtracting amplifier.

The schematic of the proposed ratio-independent SC subtracting amplifier is shown in Fig.3. The circuit performs the analog arithmetic ( $2V_{GS1} - V_{GS2}$ ) and operates in six nonoverlapping clock phases  $\phi_1$  to  $\phi_6$ . Since a single test device is used,  $V_{GS1}$  and  $V_{GS2}$  can not be available at the same time. Thus, the input of the SC circuit,  $V_G$  is

$$V_G = \begin{cases} V_{GS1} & \text{for } \phi_1 \text{ and } \phi_4 \\ V_{GS2} & \text{for } \phi_2 \text{ and } \phi_3 \end{cases}$$

Of course, the current mirror in Fig.1 is dynamically implemented such that it can supply the test device with  $I_D$  during  $\phi_1$  and

$\phi_4$  and with  $4I_D$  during  $\phi_2$  and  $\phi_3$ . The capacitors C1 and C2 are used for main operations, and C3 and C4 are the corresponding auxiliary capacitors for the preliminary operations required for compensation of the finite op-amp gain. C3 and C4 are chosen such that  $C3/C4=C1/C2$ . Capacitor Cc is used to store the finite gain error voltage.

### Sensitivity to nonideal effects

The error voltage associated with the finite op-amp gain, parasitic capacitances at internal nodes, capacitor ratio mismatches, and op-amp offset are analytically derived. To reduce complexity only two parasitic capacitances  $C_{p1}$  and  $C_{p2}$  at two critical nodes (1) and (2) are considered. The derived output voltage during  $\phi_6$  is

$$V_{out}(6) = (2V_{GS1} - V_{GS2}) - V_{err},$$

and the error voltage  $V_{err}$  is

$$V_{err} = \epsilon_{gain} + \epsilon_{mis} + \epsilon_{off}$$

where

$$\begin{aligned} \epsilon_{gain} &\simeq \frac{1}{A^2} \{ \{ y'(x-1) + x(y-z) \} (V_{GS1} - V_{GS2}) \\ &\quad + x'y'(2V_{GS1} - V_{GS2}) \} \\ \sigma_{\epsilon_{mis}} &\simeq \frac{1}{A} |z-y| (V_{GS1} - V_{GS2}) \frac{2\sigma_c}{C} \\ \epsilon_{off} &\simeq \frac{1}{A} \left[ y' \left( 2 + \frac{C4}{C3} \right) + (y-z) \left( 1 + \frac{C2}{C1} \right) \frac{C2}{C1} \right] V_{OS} \end{aligned}$$

where  $x, y, z, x',$  and  $y'$  are functions of the circuit capacitances, C1, C2, C3, C4, Cc, and the parasitic capacitances,  $C_{p1}, C_{p2}$ .

As expected, the error due to finite op-amp gain,  $\epsilon_{gain}$ , is inversely proportional to  $A^2$  where A is the op-amp dc gain. The effects of parasitic capacitances  $C_{p1}$  and  $C_{p2}$  are also divided by  $A^2$ . The standard deviation of the error term due to capacitor ratio mismatches,  $\sigma_{\epsilon_{mis}}$ , which has been derived using the similar procedure as in [10], is also small because the mismatch component is divided by the op-amp gain A. It can be seen that the circuit is also relatively insensitive to the op-amp offset voltage since in the offset error term,  $\epsilon_{offset}$ , the op-amp offset  $V_{OS}$  is divided by A. The derived equations were verified in step-by-step through SWITCAP simulations. The proposed SC subtracting amplifier has been simulated with SWITCAP. The simulated output error at different op-amp gains with  $V_{OS}$  as a parameter is shown in Fig.4. It is seen that with op-amp gains greater than 500, the error becomes less than 0.05% even with  $V_{OS} = -20mV$ . In this simulation parasitic capacitances (10% as before) associated with all other internal nodes are also considered.

### Charge Injection Reduction Schemes

The SC amplifier has been simulated with SPICE using a charge controlled MOS model (XQC=0.5), where charge conservation is guaranteed by the method of computing terminal currents. The simulated error voltage due to charge injection effects is around 10mV. This is somewhat large and thus, should also be compensated to keep the accuracy high. Although many charge injection compensation schemes have been reported, there does not exist any single scheme that can provide full compensation and can be applicable for all situations. Thus, it may be desirable to use a combination of several schemes. For the proposed circuit, several schemes are incorporated to obtain a charge injection error voltage less than 1mV.

Since the operating speed is not critical in our circuit, small-sized switches ( $W/L=4\mu m/2\mu m$ ) are used to reduce the amount of charge to be taken care of. The capacitor values have been selected such that  $C1=C2=C3=C4=4pF$  and  $Cc=8pF$ . The scheme using half-sized dummy switches can be generally applied for any types of SC circuits if equipartition of channel charge is possible. Thus, half-sized dummy switches are used in our circuit along with a fast falling gate clock which ensures almost equipartition of channel charge such that the dummy switches can compensate it. The gate voltage falling rate should be selected carefully. If the falling rate is too fast, the charge pumping effects will be significant. If the falling rate is slow, then the deviation from the equipartition will increase. A gate clock falling rate of 5V/5nsec has been selected because no significant charge pumping effects was experimentally observed down to 5nsec in [11], and SPICE simulations showed that with the switch-off fall time of 5nsec the deviation from 1:1

partition is less than 5% for most practical conditions such as node impedances. By using this the overall error voltage due to charge injection is expected to be greatly reduced although no perfect equipartition of the channel charge is possible, and the mismatches between the main and the dummy switches degrade the compensation accuracy.

The simulated overall output error voltage is 0.6mV which is a greatly reduced value compared with 10mV obtained without compensation. This accuracy well satisfies our targeted accuracy of 1mV. The simulated output waveform is shown in Fig.5 where a 30mV offset voltage source is inserted at the noninverting input terminal of the op-amp. In the figure the preliminary operations which are erroneous due to the offset voltage and the finite op-amp gain, and the compensated main operations can be easily distinguished. The accuracy can be degraded by the nonideal factors associated the dummy switch compensation such as mismatches between the main and dummy switches and clock skews. However, it has been shown from SPICE simulations that these effects are not significant.

### Dynamic Current Mirror

The current mirror block shown in Fig.1 is implemented dynamically to supply accurate currents  $I_D$  and  $4I_D$  to test devices. To reduce the finite output conductance effects of the current mirror, the self-biased stacked mirror concept proposed by Wegmann and Vittoz [12] is used in our circuit. The schematic of the dynamic current mirror and the required clock phases are shown in Fig.6.

The dynamic current mirror is composed of six current copier cells. Each cell consists of a sampling switch  $S_{i_a}$ , ( $i = 1, 2, \dots$  or 6), a storage capacitor  $C_i$ , and a PMOS transistor. Switches  $S_{i_b}$  and  $S_{i_c}$  for  $i = 1, 2, \dots, 6$ , are used to periodically connect the cells with the input  $I_D$  for refreshing the stored information and with the output for supplying the mirrored currents. The stacked common-gate transistors which are employed to increase the output impedance are connected such that one cell is always connected with node (1) to deliver current  $I_1$  (ideally  $I_D$ ), four cells are always connected with node (2) to deliver current  $I_2$  (ideally  $4I_D$ ), and remaining one cell is connected to the input bias current  $I_D$  for refreshing.

When switches  $S_{i_a}$  and  $S_{i_b}$  are closed to memorize the input current  $I_D$ , the sampling switch  $S_{i_a}$  must be opened first as shown in the clock phase diagram in Fig.6 in order not to contaminate the stored information. Once  $S_{i_a}$  is open, the gate voltage is kept constant if leakage current in the sampling switch is ignored such that the drain current remains equal to  $I_D$ . When  $S_{i_b}$  is opened, and  $S_{i_c}$  or  $S_{1_d}$  is closed, the memorized current is available at the output. The transients occurred when  $S_{i_b}$  and  $S_{i_c}$  are switched can be a significant error source for continuous-time applications as investigated in [12]. In our circuit the transient effects is not important because the currents are required for only specific time intervals, which indicates that the dynamic current is suitable for our  $V_T$  extractor.

The charge injection problem from the sampling switches is also compensated by the same strategy as used in the SC subtracting amplifier. The dynamic current mirror was simulated when node (1) and (2) were connected with a NMOS transistor ( $W/L=20\mu\text{m}/4\mu\text{m}$ ). The simulated output currents  $I_1$  and  $I_2$  are depicted in Fig.7. The initial behaviors of the current copier cells to produce output currents of ratio 1:4 can be observed until  $t = 30\mu\text{sec}$ . After the initial cycle, the current mirror can supply the currents  $I_1$  and  $I_2$  of which the ratio is ideally 1:4 to the test device. The output current ratio accuracy is shown in Fig.8 as a function of the input bias current  $I_D$ . Since the ratio error for one  $I_D$  value varies slightly at different clock phases, the maximum values are selected and shown on the figure. The ratio errors in the  $I_D$  range in interest are less than 700 ppm which produces approximately 0.5mV error in the arithmetic operation of  $2V_{GS1} - V_{GS2}$ . Therefore, along with the SC subtracting amplifier discussed in the previous sections the dynamic current mirror can perform the proposed  $V_T$  extraction scheme accurately.

### Conclusions

An accurate real-time  $V_T$  extraction scheme which does not need matched replica of the device under test has been proposed. A ratio-independent and finite gain insensitive switched-capacitor subtracting amplifier and a dynamic current mirror have been designed to perform the proposed scheme accurately in a matching-free way. Model error associated with the proposed scheme has

been investigated and compared with the linear regression method. Taking into account unexpected process variations, the total error voltages associated with the designed circuit are in a few millivolt range. This error is smaller compared with the model error. To make the  $V_T$  extractor be applicable for various transistors which has different geometries and different bias conditions and to achieve a high accuracy, the model error should be always kept small. The scheme is applicable to various applications where many  $V_T$  measurements are required. For example, the scheme can be well applied for implementation of low-voltage floating-gate MOSFET circuits where  $V_T$  measurement of many floating-gate MOSFETs with different geometries are essential for  $V_T$  tuning [13].

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Table 1: Feature comparison of  $V_T$  extraction schemes

Schemes	Required # of matched test-ns	Required matched component	Applicability at different geometries	Applicability at different substrate bias conditions	Comments
Numerical [2]	None	None	Efficient	Yes	Accurate but not suitable for real time
Wang [3]	9	Current mirror trs	Inefficient	No	Using a transistor array
Tsividis [4]	3	Current mirror trs	Inefficient	No	Using a transistor string
Alini [5]	2	Resistor & Current mirror trs	Inefficient	Yes	BICMOS implementation
Lee [6]	None	None	Efficient	Yes	Simple but Poor accuracy
Proposed	None	None	Efficient	Yes	Dynamic implementation

Table 2: Comparison between the proposed and the LR method

	That device size (W/L)	Number of samples	$V_{out} / V_{TH}$		Extracted $V_{TH}$	Error $V_{TH} - V_{TH_{true}}$
			$V_{out} / V_{TH}$	$V_{out} / V_{TH}$		
Linear Regression Method [2]	20nm 4nm	20	1.066V/0.888V	1.241V/0.888V	0.8919V	3.43mV
			1.211V/0.888V	1.525V/0.887V	0.8971V	3.58mV
	200nm 40nm	20	1.116V/0.921V	1.309V/0.921V	0.9230V	2.08mV
			1.275V/0.921V	1.625V/0.921V	0.9281V	7.09mV
The Proposed Scheme	20nm 4nm	3uA	1.066V/0.888V	1.241V/0.888V	0.8921V	3.61mV
			1.211V/0.888V	1.525V/0.887V	0.8941V	8.58mV
	200nm 40nm	10uA	1.116V/0.921V	1.309V/0.921V	0.9233V	2.36mV
			1.275V/0.921V	1.625V/0.921V	0.9275V	6.47mV

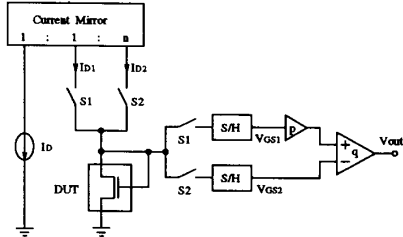


Fig.1: Conceptual schematic of the  $V_T$  extraction scheme

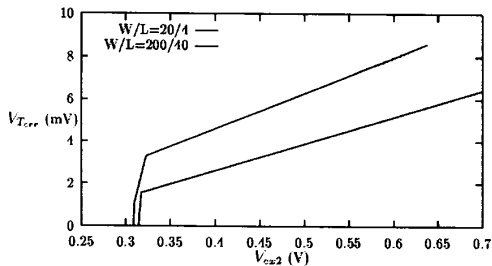


Fig.2: Difference between  $V_{T_{ext}}$  and  $V_{T_H}$

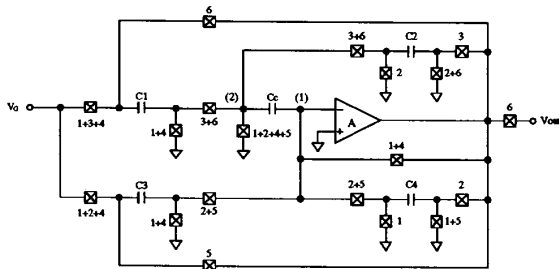


Fig.3: Schematic of the proposed SC amplifier

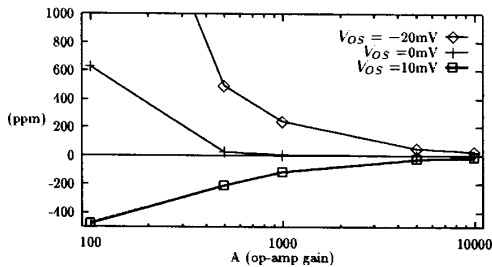


Fig.4: SWITCAP simulated output error voltage  $V_{err}$

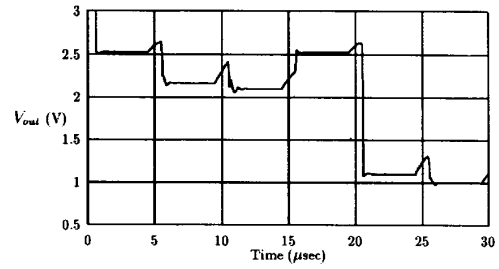


Fig.5: Simulated  $V_{out}$  ( $V_{GS1}=1.4V$ ,  $V_{GS2}=1.8V$ ,  $A=800$ )

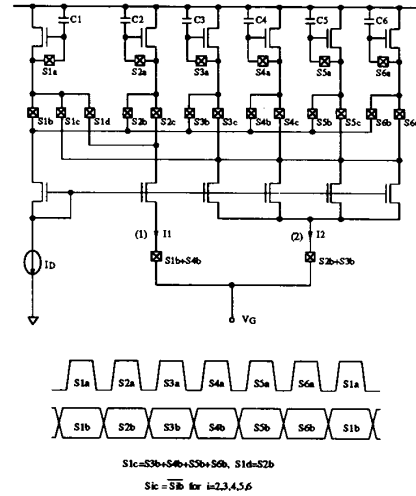


Fig.6: Schematic of the dynamic current mirror

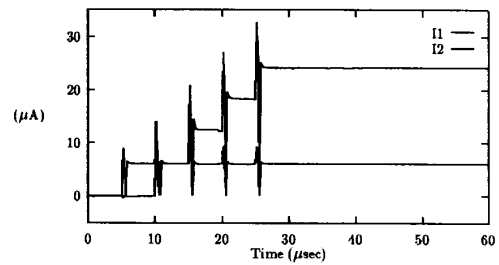


Fig.7: Simulated output currents  $I_1$  and  $I_2$

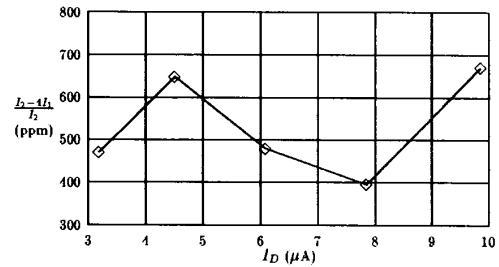


Fig.8: Simulated current ratio error