MOS Active Attenuators for Analog ICs And Their Applications to Finite Gain Amplifiers

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ABSTRACT

A MOS active summing voltage attenuator along with the voltage attenuator proposed before [5] form a set of attenuators particularly useful in analog monolithic applications. The performance of a finite gain amplifier employing the MOS active attenuator is discussed. Large signal and small signal multiple input monolithic finite gain summing and subtracting amplifiers employing the attenuators are presented.

INTRODUCTION

Voltage attenuators have applications in circuits such as feedback amplifiers, data converters, and input stages of transconductance amplifiers. In discrete circuits, the resistor voltage divider is widely used as an attenuator. However, in integrated circuits, the resistor voltage divider is not attractive because of its large area, high power dissipation, and large parasitic capacitances. Alternatively, simple MOS active voltage attenuators suitable for monolithic applications have been proposed [1-5]. In this paper, a MOS active summing attenuator consisting of two cascaded MOS active attenuators will be presented. Finite gain amplifiers employing the attenuator and finite gain summing and subtracting amplifiers employing the attenuator and the summing attenuator will be introduced.

SUMMING ATTENUATOR

The n-channel MOS active attenuator [5] and a new summing attenuator are shown in Fig. 1. The summing attenuator consists of two attenuators cascaded. For the summing attenuator, V_{BB} is used to control the output operating voltage and input signals are designated as V_1 and V_2. As for the inverting attenuator [5], the summing attenuator works when all the four transistors are in the saturation region. Thus, the dc transfer characteristic can be obtained by equating the drain currents in the saturation region for each attenuator. Assuming that the zero bias threshold voltages of the four MOSFETs are matched at V_{TON}, the four transistors are in the saturation region provided

$$2V_{TON} + \gamma\left(\sqrt{\phi + V_{TON}} - \sqrt{\phi}\right) < V_{BB} < V_{DD} + V_{T4}, \quad (1)$$

$$V_{TON} < V_1 < V_O + V_{TON}, \quad (2)$$

and

$$V_{TON} < V_2 < V_B + V_{TON}. \quad (3)$$

Using the Sah's model for the drain currents, the dc transfer characteristic is obtained as

$$R_1 V_1 - V_B = (R_1 - 1)V_{TON} - V_O - \gamma\left(\sqrt{\phi + V_O} - \sqrt{\phi}\right) \quad (4)$$

$$R_2 V_2 - V_{BB} = (R_2 - 1)V_{TON} - V_B - \gamma\left(\sqrt{\phi + V_B} - \sqrt{\phi}\right) \quad (5)$$

where

$$R_1 = \sqrt{W_1 L_2 / L_1 W_2} \quad (6)$$

and

$$R_2 = \sqrt{W_3 L_4 / L_3 W_4}. \quad (7)$$

Linearity

If $\gamma=0$ in (4) and (5), the equations become linear. This is attainable if each transistor is fabricated in a separate substrate and the substrate of each transistor is connected to its source. In this case, the attenuation factors are given by $\alpha=-R_1$, $\alpha_1=-R_1$, and $\alpha_2=-R_2$. Even when $\gamma \neq 0$, which is the case where the substrates are common, the transfer characteristics between V_1 and V_O and between V_2 and V_O

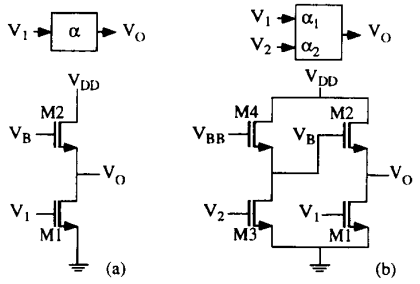

Fig. 1. The circuit diagram of the n-channel (a) attenuator and (b) summing attenuator.

are very nearly linear as shown in Fig. 2 for practical γ. It is these facts that make the circuit useful as a voltage attenuator in both cases. In the calculation for Fig. 2, γ=0.5255V$^{1/2}$, ϕ=0.6V and V_{TON}=0.777V were used which are standard for 2μ CMOS process and R_1=0.1149 and R_2=0.1290 were set such that the small signal attenuation factors for v_1 and v_2 are both -0.1 The operating points were set by V_{BB}=5.712V such that V_{OQ}=2.5V (V_{BQ}=3.993V) when $V_{1Q}=V_{2Q}$=2.5V.

To mathematically characterize the nonlinearity, the harmonic distortion for each input can be obtained if the dc transfer characteristics of (4) and (5) are expanded into a Taylor's series. For $V_1 = V_{1Q} + v_1$ and $V_B = V_{BQ} + v_B$, the output voltage, V_O, is expanded as

$$V_O = V_{OQ} + v_O = H_1(V_1, V_B) \tag{8}$$

$$\cong H_1(V_{1Q}, V_{BQ}) + \left.\frac{\partial H_1}{\partial V_1}\right|_Q v_1 + \left.\frac{\partial H_1}{\partial V_B}\right|_Q v_B + \frac{1}{2}\left.\frac{\partial^2 H_1}{\partial V_1^2}\right|_Q v_1^2 + \frac{1}{2}\left.\frac{\partial^2 H_1}{\partial V_B^2}\right|_Q v_B^2 + \left.\frac{\partial^2 H_1}{\partial V_1 \partial V_B}\right|_Q v_1 v_B$$

where $V_O = H_1(V_1, V_B)$ is the dc transfer characteristic given by (4). Similarly, for $V_{BB}=V_{BBQ}$ and $V_2=V_{2Q}+v_2$,

$$V_B = V_{BQ} + v_B = H_2(V_2, V_{BB})$$
$$\cong H_2(V_{2Q}, V_{BBQ}) + \left.\frac{\partial H_2}{\partial V_2}\right|_Q v_2 + \frac{1}{2}\left.\frac{\partial^2 H_2}{\partial V_2^2}\right|_Q v_2^2 \tag{9}$$

where $V_B = H_2(V_2, V_{BB})$ is the dc transfer function given by (5). Substituting $v_2=B\sin\omega t$, we obain

$$V_B = \left(H_2(V_{2Q}, V_{BBQ}) + \frac{1}{4}\left.\frac{\partial^2 H_2}{\partial V_2^2}\right|_Q B^2\right) + \left(\left.\frac{\partial H_2}{\partial V_2}\right|_Q B\sin\omega t - \frac{1}{4}\left.\frac{\partial^2 H_2}{\partial V_2^2}\right|_Q B^2\cos 2\omega t\right). \tag{10}$$

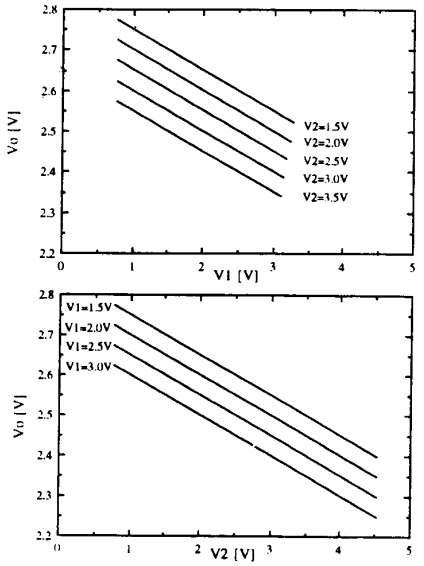

Fig. 2. dc transfer characteristics of the summing attenuator

Substituting $v_1 = A\sin\omega t$ and v_B obtained as the second term in (10) into (8), the output of the summing attenuator, V_O, is given by

$$V_O = H(V_1, V_2, V_{BB})$$
$$\cong \left\{H_1(V_{1Q}, V_{BQ}) + \frac{1}{4}\left.\frac{\partial^2 H_1}{\partial V_1^2}\right|_Q A^2 + \frac{1}{4}\left.\frac{\partial^2 H_1}{\partial V_B^2}\right|_Q \left.\frac{\partial H_2}{\partial V_2}\right|_Q^2 B^2 + \frac{1}{2}\left.\frac{\partial^2 H_1}{\partial V_1 \partial V_B}\right|_Q \left.\frac{\partial H_2}{\partial V_2}\right|_Q AB\right\}$$
$$+\left\{\left.\frac{\partial H_1}{\partial V_1}\right|_Q A + \left.\frac{\partial H_1}{\partial V_B}\right|_Q \left.\frac{\partial H_2}{\partial V_2}\right|_Q B\right\}\sin\omega t \tag{11}$$
$$-\left\{\frac{1}{4}\left.\frac{\partial^2 H_1}{\partial V_1^2}\right|_Q A^2 + \frac{1}{4}\left(\left.\frac{\partial H_1}{\partial V_B}\right|_Q \left.\frac{\partial^2 H_2}{\partial V_2^2}\right|_Q + \left.\frac{\partial^2 H_1}{\partial V_B^2}\right|_Q \left.\frac{\partial H_2}{\partial V_2}\right|_Q^2\right)B^2 + \frac{1}{2}\left.\frac{\partial^2 H_1}{\partial V_1 \partial V_B}\right|_Q \left.\frac{\partial H_2}{\partial V_2}\right|_Q AB\right\}\cos 2\omega t.$$

The first term in (11) is the total dc component, the second term the desired signal, and the third term is the second harmonic component of the output, respectively. From the second term, the small signal attenuation factor for v_1 is $\left.\frac{\partial H_1}{\partial V_1}\right|_Q$ and that for v_2 is $\left.\frac{\partial H_1}{\partial V_B}\right|_Q \left.\frac{\partial H_2}{\partial V_2}\right|_Q$. At the same condition used earlier to calculate the dc transfer characteristic, the signal to THD ratio is calculated to be 78.3dB when both the input signal amplitudes are 100mV.

Noise Analysis of the Summing Attenuator

Fig. 3 shows a noise equivalent circuit of the summing attenuator based on noiseless transistors and output referred noise current sources and its simplified equivalent circuit. From Fig. 3, the output noise voltage (rms), V_{NO}, of the summing attenuator is given by

$$V_{NO} = \frac{I_N}{g_O} = \frac{\sqrt{I_{N1}^2 + I_{N2}^2 + \left(g_{m2}V_{NO}'\right)^2}}{g_O} = \frac{\sqrt{I_{N1}^2 + I_{N2}^2 + \left(\frac{g_{m2}}{g_{m4}+g_{mb4}}\right)^2\left(I_{N3}^2 + I_{N4}^2\right)}}{g_{m2}+g_{mb2}}$$
$$= \frac{\sqrt{\int_{f_1}^{f_2} S_{I1} + S_{I2}df + \left(\frac{g_{m2}}{g_{m4}+g_{mb4}}\right)^2 \int_{f_1}^{f_2} S_{I3} + S_{I4}df}}{g_{m2}+g_{mb2}} \tag{12}$$

where

$$S_{Ii} = \frac{8}{3}kTg_{mi} + \frac{2K_fK'I_{DQi}}{C_{OX}L_i^2 f} \text{ for } i=1,\ 2,\ 3,\ \text{and } 4 \tag{13}$$

and where the subscripted variable I_{XX}, g_{XX} and S_{XX}, denote drain current, transconductance and noise current spectral

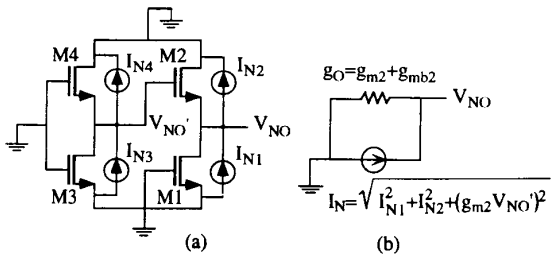

Fig. 3. (a) A noise equivalent circuit of the summing attenuator and (b) its simplified equivalent circuit

density respectively.

For given attenuation factors, R_1 and R_2 are determined. Then, the sizes (W and L) of each transistor in the attenuator can be optimized for minimum output noise using the same scheme presented in [5]. Consider the $\gamma=0$ case for the calculation of the output noise, $R_1=R_2=0.1$ for attenuation factors of -0.1 and $V_{BB}=4.398$V ($V_{BQ}=3.449$V) for the same input and output operating voltages at 2.5V. The other process dependent parameters are the same we used earlier. When the allowable range for the transistor sizes is 2-100μm, the optimized sizes for minimum noise are $W_1=W_3=15.59\mu m$, $L_1=L_3=W_2=W_4=100\mu m$ and $L_2=L_4=6.415\mu m$. The summing attenuator consisting of these transistors has output noise, V_{NO}, of 1.7864×10^{-5}V(rms) and power dissipation, P_d, of 131μW. Thus, when both the input amplitudes are 0.7V which is maximum for v_1, the dynamic range, DR, which is signal to random noise ratio is 74.9dB.

AN AMPLIFIER EMPLOYING THE ATTENUATOR

Fig. 4. shows an finite gain amplifier consisting of an ideal op-amp and the active attenuator shown in Fig. 1 (a) in the feedback loop. If the op-amp is assumed ideal,

$$V_1' = V_O = H_1(V_1) = H_1(V_O'), \tag{14}$$

or

$$V_O' \equiv T_1(V_1') = H_1^{-1}(V_1'). \tag{15}$$

For $V_1' = V_{1Q}' + v_1' = V_{1Q}' + A' \sin\omega t$, the Taylor's series expansion of the output of the amplifier, V_O', is given by

$$V_O' = T_1(V_1') \cong T_1(V_{1Q}') + \left.\frac{\partial T_1}{\partial V_1'}\right|_Q v_1' + \frac{1}{2}\left.\frac{\partial^2 T_1}{\partial V_1'^2}\right|_Q v_1'^2 \tag{16}$$

$$= \left(T_1(V_{1Q}') + \frac{1}{4}\left.\frac{\partial^2 T_1}{\partial V_1'^2}\right|_Q A'^2 \right) + \left.\frac{\partial T_1}{\partial V_1'}\right|_Q A' \sin\omega t - \frac{1}{4}\left.\frac{\partial^2 T_1}{\partial V_1'^2}\right|_Q A'^2 \cos 2\omega t.$$

For an amplifier of a gain of -10, the attenuator in the feed-feedback loop should have an attenuation factor of -0.1. At the same condition used earlier in the calculation for Fig. 2, the signal to THD ratio of the output is 85.6dB for 10mV input amplitude. If the op-amp is assumed ideal, the output noise voltage of the amplifier is the input referred noise voltage of the attenuator which is simply given by (gain of the amplifier)× V_{NO} where V_{NO} is the output noise voltage of the attenuator. From [5], when the transistor sizes are optimized for minimum noise within 2-100μm range, $V_{NO}=9.61\times 10^{-6}$V(rms) at the same condition used earlier. The maximum applicable input amplitude to the amplifier is about 70mV. At this input amplitude, the dynamic range of the amplifier is 74.2dB at a signal to THD ratio of 0.037% (68.7dB).

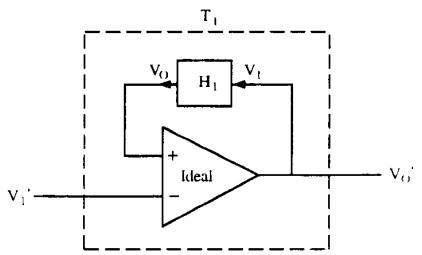

Fig. 4. An amplifier consisting of an op-amp and the attenuator

SUMMING AND SUBTRACTING AMPLIFIERS

Some new summing and subtracting amplifier structures using the inverting attenuator and the inverting summing attenuator are shown in Fig. 5. The circuits (a) and (b) in Fig. 5 function as summing amplifiers and the circuit (c) functions as an subtracting amplifier, with controllable weights. Assuming ideal op-amps and attenuators, we obtain for the circuit (a) in Fig. 5,

$$V_O = \frac{\alpha_1}{\alpha} V_1 + \frac{\alpha_2}{\alpha} V_2 + \left(V_{OQ} - \frac{\alpha_1}{\alpha} V_{1Q} - \frac{\alpha_2}{\alpha} V_{2Q} \right), \tag{17}$$

where V_{OQ} is a function of V_{1Q}, V_{2Q}, V_{BB} of the summing attenuator and V_B of the attenuator. From (17), it trivially follows that

$$v_O = \frac{\alpha_1}{\alpha} v_1 + \frac{\alpha_2}{\alpha} v_2. \tag{18}$$

If

$$V_{OQ} - \frac{\alpha_1}{\alpha} V_{1Q} - \frac{\alpha_2}{\alpha} V_{2Q} = 0, \tag{19}$$

which can be met by controlling V_{BB} and V_B,

$$V_O = \frac{\alpha_1}{\alpha} V_1 + \frac{\alpha_2}{\alpha} V_2. \tag{20}$$

Thus, the circuit in Fig. 5 (a) can be a either small signal or large signal summer with arbitrary controllable weights for each input.

For the circuit in Fig. 5 (b) which uses only one summing

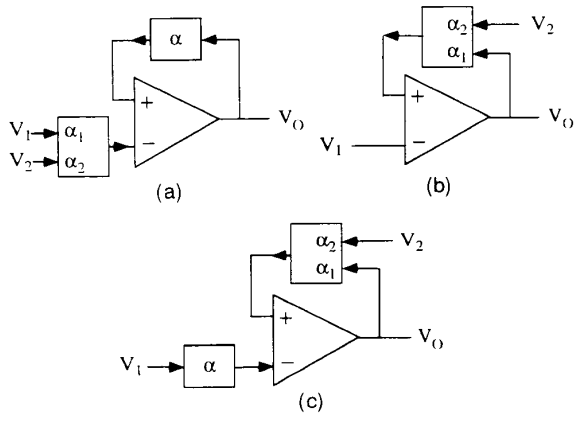

Fig. 5. (a) and (b) summing amplifiers, (c) subtracting amplifier

attenuator along with an op-amp, we obtain

$$V_O = \frac{1}{\alpha_1} V_1 - \frac{\alpha_2}{\alpha_1} V_2 + \left(V_{OQ} - \frac{1}{\alpha_1} V_{1Q} + \frac{\alpha_2}{\alpha_1} V_{2Q} \right). \quad (21)$$

From (21), it follows trivially that

$$v_O = \frac{1}{\alpha_1} v_1 - \frac{\alpha_2}{\alpha_1} v_2. \quad (22)$$

If

$$V_{OQ} - \frac{1}{\alpha_1} V_{1Q} + \frac{\alpha_2}{\alpha_1} V_{2Q} = 0, \quad (23)$$

$$V_O = \frac{1}{\alpha_1} V_1 - \frac{\alpha_2}{\alpha_1} V_2. \quad (24)$$

The circuit (b) in Fig. 5 can be used as an inverting small signal or large signal summer with different gains for each input.

For the circuit shown in Fig. 5 (c),

$$V_O = \frac{\alpha}{\alpha_1} V_1 - \frac{\alpha_2}{\alpha_1} V_2 + \left(V_{OQ} - \frac{\alpha}{\alpha_1} V_{1Q} + \frac{\alpha_2}{\alpha_1} V_{2Q} \right), \quad (25)$$

or

$$v_O = \frac{\alpha}{\alpha_1} v_1 - \frac{\alpha_2}{\alpha_1} v_2. \quad (26)$$

If

$$V_{OQ} - \frac{\alpha}{\alpha_1} V_{1Q} + \frac{\alpha_2}{\alpha_1} V_{2Q} = 0, \quad (27)$$

from (25),

$$V_O = \frac{\alpha}{\alpha_1} V_1 - \frac{\alpha_2}{\alpha_1} V_2. \quad (28)$$

The circuit in Fig. 5 (c) can be a either small signal or large signal subtractor.

It is also possible to construct multiple (more than two) input summing and subtracting amplifiers. Sample three input and four input summing amplifiers using the two input summing amplifier shown in Fig. 5 (a) as a basic building block are shown in Fig. 6. For the three input summing amplifier shown in Fig. 6 (a),

$$v_O = \frac{\alpha_{11}\alpha_{21}}{\alpha_{f1}\alpha_{f2}} v_1 + \frac{\alpha_{12}\alpha_{21}}{\alpha_{f1}\alpha_{f2}} v_2 + \frac{\alpha_{22}}{\alpha_{f2}} v_3. \quad (29)$$

For the four input summing amplifier shown in Fig. 6 (b),

$$v_O = \frac{\alpha_{11}\alpha_{31}}{\alpha_{f1}\alpha_{f3}} v_1 + \frac{\alpha_{12}\alpha_{31}}{\alpha_{f1}\alpha_{f3}} v_2 + \frac{\alpha_{21}\alpha_{32}}{\alpha_{f2}\alpha_{f3}} v_3 + \frac{\alpha_{22}\alpha_{32}}{\alpha_{f2}\alpha_{f3}} v_4. \quad (30)$$

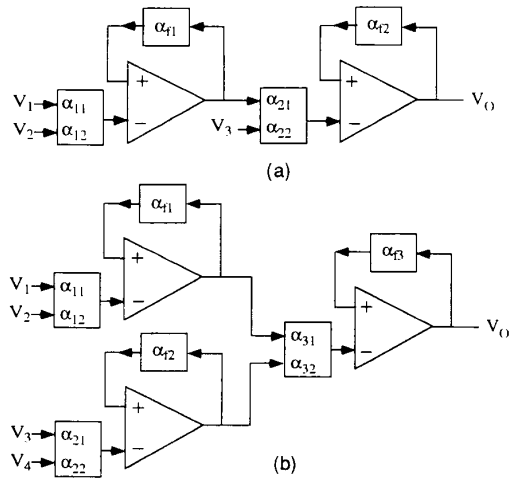

Fig. 6. Examples of multiple input summing amplifiers

CONCLUSION

A MOS active summing attenuator suitable for monolithic applications has been presented. Its performance in terms of harmonic distortion and random noise was investigated. An amplifier employing the attenuator in the feedback loop has been presented. Small signal and large signal, summing and subtracting amplifiers employing the summing attenuator and the attenuator with an op-amp was presented as were multiple (more than two) input summing amplifier structures employing the attenuators.

The active summing attenuators and the active attenuator have many attractive characteristics such as small size, nearly infinite input impedance, precisely controllable attenuation ratio, low power consumption, good linearity, low noise and offset adjustability independent of attenuation ratio. It is believed that the attenuators with these merits and the versatile finite gain amplifiers realized with the attenuators and op-amps should find applications in analog integrated circuits.

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