At the input stage of the drive circuitry, a standard TTL rising-edge trigger pulse is buffered by transistor Q1 to form the negative trigger signal 'A'. This turns on the pulsed bias output FET Q3, which produces a negative pulse at the output of T1, forcing the step-recovery diode into forward bias and so inducing a saturation charge density across its junction. By applying a pulsed bias to the step-recovery diode rather than a conventional DC bias, a larger charge density can be achieved without exceeding the average power dissipation rating of the diode. Application of the bias through T1 also avoids the need to attach components directly to the diode, which can contribute to spurious reflections.

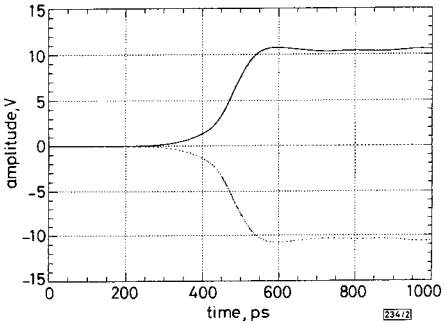

Fig. 2 *Output of balanced subnanosecond pulse generator into a 50Ω coaxial line, for both connection polarities*

——— positive output
····· negative output

The pulse at 'A' continues through the inverting delay stage Q2 to produce the positive trigger signal 'B', turning on transistor Q4 which is operated in avalanche mode for high speed. This causes a high-current positive pulse with 6ns risetime to appear at the output of T1, which starts to remove the stored charge from the step-recovery diode. Although the risetime of this pulse is relatively slow compared to those normally applied to step-recovery diodes, there will be at least enough residual charge on the diode induced by the preceding pulsed bias to last until the drive signal has reached its ultimate amplitude. When charge removal is completed, the diode abruptly snaps into a nonconducting state within 100ps, and the result is the output waveforms of Fig. 2, produced when the SRD is connected across a single 50Ω unbalanced transmission line with opposite polarity connection in the two cases. Measured by a sampling oscilloscope with 25ps risetime, the circuit produces an 11V step with a 20–80% risetime of 80ps. The transformer T1 has an isolating effect due to the limited bandwidth of the ferrite core, and prevents the high-speed step from coupling back to the driving circuit. Reflections from the driver circuit are therefore eliminated and the result is a clean output waveform which is free of spurious ringing.

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Characterisation of linear MOS active attenuator and amplifier

J.-Y. Kim and R.L. Geiger

Indexing terms: MOS integrated circuits, Active networks, Amplifiers, Attenuators

The experimental performance of a linear monolithic MOS active voltage attenuator and a linear finite gain amplifier employing the attenuator in the feedback loop is discussed. Measured DC transfer characteristics, and the signal to harmonic distortion ratios as functions of signal amplitudes, are presented.

Introduction: In discrete circuits, high performance finite gain amplifiers using an operational amplifier with a voltage divider consisting of two resistors in the feedback path are widely used. In monolithic applications, the resistive voltage attenuator is impractical because it requires large area, has a low input impedance, consumes considerable power, and has large parasitic capacitances. A precise and practical monolithic attenuator suitable for making finite gain amplifiers has eluded designers for many years.

MOS active attenuators, simple in structure but with performance suitable for monolithic applications, have been proposed [1 – 6]. In this Letter, the experimental performance of an attenuator and a finite gain amplifier [1] consisting of an operational amplifier and the attenuator in the feedback path is reported.

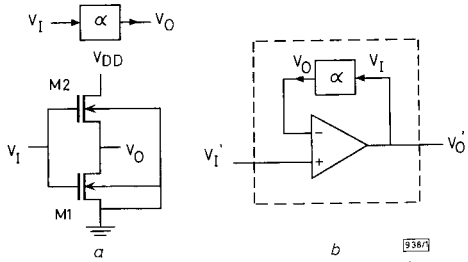

Fig. 1 *Circuit and block diagram of attenuator consisting of two n-channel MOSFETs, and block diagram of amplifier consisting of an opamp and attenuator*

a Attenuator
b Amplifier

Attenuator and amplifier: Fig. 1 shows the attenuator consisting of two *n*-channel MOSFETs and the amplifier employing the attenuator [1]. The circuit shown in Fig. 1*a* operates as a voltage attenuator when M1 is in the ohmic region and M2 is in the saturation region. Thus, provided

$$V_{T1} < V_I < V_{DD} + V_{T2} \quad (1)$$

it follows from the simple square law model with $\gamma = 0$ that

$$V_O = \alpha(V_I - V_{TON}) \quad (2)$$

where the attenuation factor α is given by

$$\alpha = 1 - \sqrt{\frac{\frac{W_1}{L_1}}{\frac{W_1}{L_1} + \frac{W_2}{L_2}}} \quad (3)$$

an attenuation that is precisely determined by width/length ratios. If $\gamma \neq 0$, the relationship between the input and output is still

nearly linear, linearity that is somewhat obscured by the explicit relationship between V_O and V_I:

$$2\frac{\frac{W_1}{L_1}}{\frac{W_2}{L_2}}\left(V_I - V_{TON1} - \frac{V_O}{2}\right)V_O = \left\{V_I - V_{TON2} - V_O - \gamma\left(\sqrt{\phi + V_O} - \sqrt{\phi}\right)\right\}^2 \quad (4)$$

Assuming an ideal opamp, the DC transfer function of the amplifier shown in Fig. 1*b* is the inverse of the DC transfer function of the attenuator in the feedback loop. Thus, the input V'_I and output V'_O relationship of the amplifier is given by eqn. 2 when V_O is replaced by V'_I and V_I by V'_O.

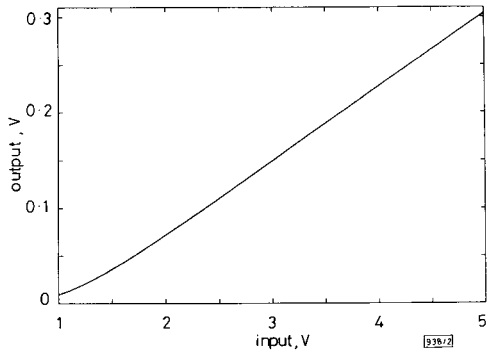

Fig. 2 *DC transfer characteristic of attenuator*

Experimental results: The attenuators were fabricated using a standard 2μm CMOS process. Fig. 2 shows the measured DC transfer characteristic of the attenuator consisting of M1 (12 × 10μm²) and M2 (3 × 10μm²) when the substrate is common ($\gamma \neq 0$). V_{DD} was 5V in the measurement. The DC transfer characteristic exhibits a high degree of linearity for the input range 2–5V. The small signal attenuation factor which is the slope of the DC transfer characteristic is 0.07824 at an input quiescent voltage of 3.5V. To further investigate the linearity of the attenuator, a sinusoidal input was applied at the 3.5V input quiescent point and the spectrum of the output was measured at different input amplitudes.

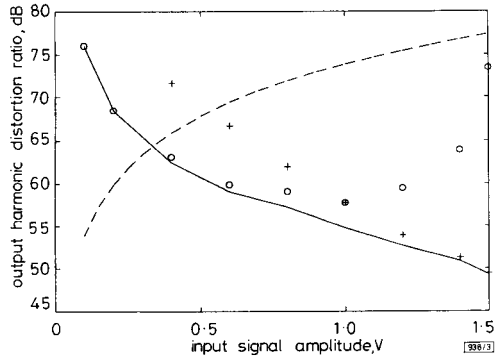

Fig. 3 *Signal to harmonic distortion ratios of output of attenuator against input amplitude*

——— signal to THD ratio
O signal to 2ndHD ratio
\+ signal to 3rdHD ratio
– – – – signal to noise ratio

Results are shown in Fig. 3. The signal to THD ratio was 76.0dB at 100mV input signal amplitude and gradually decreased as the signal amplitude increased. The output noise voltage was calculated to be 1.1228×1^{-5}V RMS for the noise band of 100Hz to 1MHz, using the noise model in [1], the 2μm process parameters, the dimensions of the MOSFETs, and the operating point voltages. The output signal to noise ratio is also shown in Fig. 3 as a function of input signal amplitude. From Fig. 3, the maximum of the signal output to the total non-signal output ratio, STNR [1], is 61.2dB at an input signal amplitude of 330mV. The power consumption at the input quiescent voltage of 3.5V was measured to be 185μW.

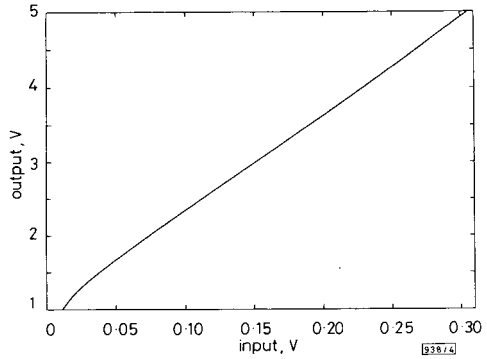

Fig. 4 *DC transfer characteristic of amplifier*

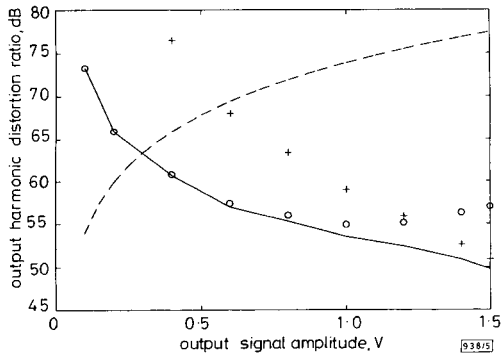

Fig. 5 *Signal to harmonic distortion ratios of output of amplifier against output amplitude*

——— signal to THD ratio
O signal to 2ndHD ratio
\+ signal to 3rdHD ratio
– – – – signal to noise ratio

The amplifier shown in Fig. 1*b* was formed with the same attenuator and an LF351 opamp. The DC transfer characteristic of the amplifier is shown in Fig. 4. The signal to THD ratio of the output is shown in Fig. 5 as a function of the output amplitude. The small signal gain at the 3.5V output quiescent point was measured to be 12.72. The signal to THD ratio of the output of the amplifier was 73.3dB at the output signal amplitude of 100mV with the output quiescent voltage at 3.5V. Neglecting the noise from the opamp, the output noise voltage of the amplifier is the gain of the amplifier multiplied by the output noise voltage of the attenuator, that is, 1.4282×10^{-4}V RMS. The signal to noise ratio of the output of the amplifier is also shown in Fig. 5 as a function of the output amplitude. The STNR is 60.2dB when the output signal amplitude is 290mV.

Conclusion: Experimental results showed a monolithic attenuator with signal to THD ratio of 76.0dB at 100mV input signal amplitude and STNR of 61.2dB at 330mV input signal amplitude. An amplifier employing the attenuator has a signal to THD ratio of 73.3dB at 100mV output signal amplitude and STNR of 60.2dB at 290mV output signal amplitude. The monolithic attenuator and amplifier should find applications in mixed-signal integrated circuits.

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Feedforward pulse-width modulator for boost DC-DC power converters

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Indexing terms: Power convertors, Pulse width modulation

The authors describe a novel pulse-width modulator with feedforward compensation of input voltage disturbances in boost DC-DC switched mode power converters. The modulator transforms an open-loop boost converter into a linear DC voltage amplifier. It is suitable for simple integrated-circuit implementation using the same building blocks as existing PWM controllers for switched mode power supplies.

Introduction: A usual requirement for high-quality power supplies is a low audio susceptibility over a wide frequency range. At DC, without an outer feedback loop, the audio susceptibility $|\hat{v}_o/\hat{v}_g|$ of a switched mode DC-DC power converter is equal to the DC conversion ratio $|V_o/V_g|$, where V_o is the output DC voltage, V_g is the input DC voltage, and $\hat{v}_o$, $\hat{v}_g$ denote small-signal perturbations.

In conventional pulse-width modulators used in switched mode power supplies, the output pulsating waveform $c(t)$ is obtained by comparing a slowly-varying modulating input v_m with a periodic sawtooth waveform $v_r(t)$. As a result, the PWM output duty ratio D is proportional to the modulating input, $D = v_m/V_M$, where V_M is the peak of the sawtooth waveform. The ideal DC conversion ratio of the boost converter is

$$\frac{V_o}{V_g} = \frac{1}{1-D} \qquad 0 \le D < 1 \tag{1}$$

Because the boost converter steps up the input voltage, the open-loop audio susceptibility is greater than 0dB at DC.

Feedforward compensation can be used to reduce the effects of input voltage disturbances on the converter output voltage. This technique is well known and frequently applied with buck (step-down) and buck-derived converters, where the slope of the sawtooth waveform in the pulse-width modulator is varied in proportion to the input voltage V_g. [1] showed how feedforward PWM can be used in other switched mode converters, but the method was found unsuitable for the boost converter where it results in zero control-to-output gain.

This Letter describes a novel pulse-width modulator that allows effective feedforward compensation in the boost converter.

Description of feedforward PWM: Fig. 1 shows the boost converter with the new feedforward pulse-width modulator (FF-PWM). A sawtooth waveform $v_r(t)$ is obtained using an integrator with reset. A clock signal resets the integrator periodically with

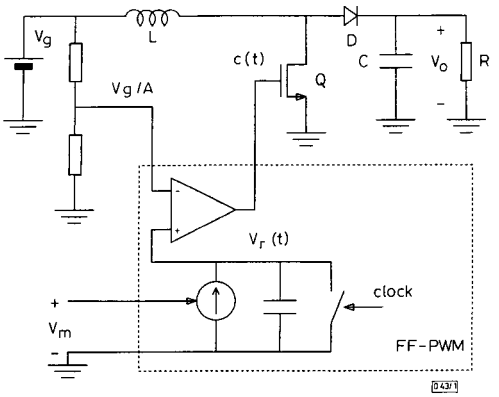

Fig. 1 *Boost converter with feedforward pulse-width modulator*

Experimental parameters are: L = 718μH, C = 10μF, Q = MTP8N50, D = MUR810, R = 250Ω, v_m = 5V = const, A = 10

period T_s. The capacitor charging current in the integrator is proportional to the slowly-varying modulating input v_m. Assuming that v_m is constant, the periodic sawtooth waveform $v_r(t)$ is given by

$$v_r(t) = v_m \frac{t}{T_s} \quad 0 \le t < T_s \quad v_r(t + kT_s) = v_r(t) \tag{2}$$

A voltage comparator compares $v_r(t)$ with scaled input voltage V_g/A. The output of the comparator is the pulsating signal $c(t)$ that controls the switching transistor Q in the boost converter. Gate-drive circuitry is shown in Fig. 1. Fig. 2 shows typical waveforms in the FF-PWM. The resulting duty ratio D is a nonlinear function of the modulating input v_m:

$$D = 1 - \frac{V_g}{Av_m} \qquad Av_m \ge V_g \tag{3}$$

Steady-state and dynamic characteristics: From eqns. 1 and 3, we have that $V_o = Av_m$, which means that the converter becomes a linear DC voltage amplifier with gain A independent of operating conditions.

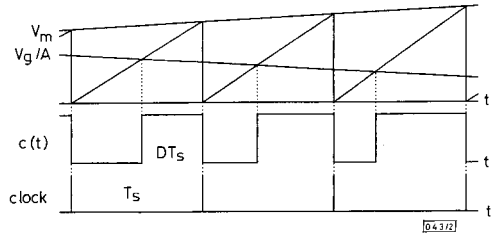

Fig. 2 *Typical waveforms in feedforward pulse-width modulator*

The effects of the FF-PWM on the small-signal dynamics can be obtained by perturbing and linearising eqn. 3 around a steady-state operating point. Duty ratio perturbation $\hat{d}$ is given by

$$\hat{d} = -\frac{(1-D)}{V_g}\hat{v}_g + A\frac{(1-D)^2}{V_g}\hat{v}_m \tag{4}$$

Eqn. 4 can be combined with the converter state-space averaged small-signal dynamic model [2] to obtain all transfer functions of interest. The audio susceptibility with FF-PWM is given by

$$H_{af}(s) = \frac{\hat{v}_o}{\hat{v}_g} = \frac{V_o}{V_g}\frac{s/w_z}{1 + \frac{1}{Q}(s/w_o) + (s/w_o)^2} = H_a(s)\frac{s}{w_z} \tag{5}$$

where

$$w_z = \frac{R(1-D)^2}{L} \quad w_o = \frac{1-D}{\sqrt{LC}} \quad Q = R\sqrt{\frac{C}{L}} \tag{6}$$

and $H_a(s)$ is the audio susceptibility without feedforward compensation. Note that $|H_{af}(jw)|$ is ideally zero at DC and reduced in a