A Charge Conserving Macromodel for MOSFET's

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ABSTRACT

A charge conserving macromodel suitable for the simulation of the charge injection behavior of MOSFET switches is presented. Simulation results using the macromodel are compared with the experimental data in the literature. The performance of the macromodel at high switching speed is demonstrated.

INTRODUCTION

In analog circuits, MOSFET's are widely used as switches. A major limitation of the MOS switch is that it disturbs the adjacent node voltages when it is turned off. This is due to injection of channel charge when the MOS switch is turned off and coupling through the gate-drain/source overlap capacitances. This non-ideal behavior of the MOS switch and the techniques used to minimize the disturbance have been investigated [1]-[6]. Models for MOSFET's which can simulate the charge injection behavior have been developed [7]-[15]. The analytic or numerical models are difficult to use if the circuit involving MOS switches is not simple. In actual circuits with MOS switches, the fraction of channel charge injected to the drain or source nodes depends on the conditions at the nodes, signal level and impedance, and on the time-varying conductance of the switch itself during the turn-off transient. The gate-channel capacitance is geometrically distributed. Existing charge conserving models require preset input for the partitioning of the injected charge or divide the gate-channel capacitance and lump it at the drain and source nodes. Thus, it is difficult to accurately simulate the charge injection behavior of MOS switches or to simulate the effectiveness of compensation schemes.

As high precision high speed circuits such as high precision high speed sample-and-hold circuits, high resolution high speed ADC's, and many other high precision high speed switched-capacitor or switched-current circuits are demanded, a model and simulator which can accurately simulate the capacitive behavior as well as the conductive behavior of MOS switches is required.

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CHARGE CONSERVING MACROMODEL FOR MOSFET's

In SPICE, the conductance of MOSFET's is quite well modeled [13]-[15], [7], but the capacitive characteristics of MOSFET models have limitations because the charge conserving Level 2 model requires a preset input for the partitioning. Fig. 1 shows the parasitic capacitances in MOSFET's when the distributed bulk-channel capacitance is depicted by the capacitor C_{BC}. Fig. 2 shows the energy band diagram of an n-channel MOSFET inside the semiconductor exhibiting the junction capacitances between bulk and source/drain and the bulk-channel junction-like depletion capacitance. Based on the nature of the capacitances and utilizing the conductance models in SPICE, the macromodel shown for n-channel MOSFET's in Fig. 3 is proposed. This macromodel can accurately simulate the characteristics of MOSFET's when it is implemented in SPICE.

The $(n+1)$ MOSFET's in the model shown in Fig. 3 are used to model the channel conductance. Because all the parasitic capacitances are accounted for with external capacitors and diodes which obey the charge conservation principle, the MOSFET's in the macromodel should be modeled to be parasitic capacitance free. If the channel area of the transistor to be modeled is WxL with lateral diffusion of LD, the channel area of each of the MOSFET's, M_1, M_2, ... , M_n, M_{n+1}, in the macromodel should be Wx{$(L-2LD)/(n+1)$} with zero lateral diffusion such that the series connection of the $(n+1)$ MOSFET's can model the conductance of the WxL MOSFET with lateral diffusion

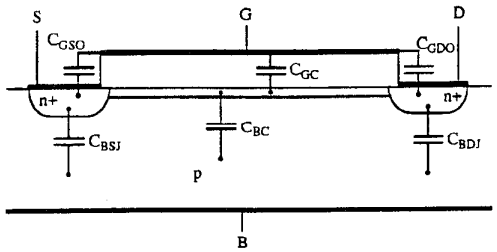

Fig. 1. Parasitic capacitances in MOSFET's, shown for an n-channel device

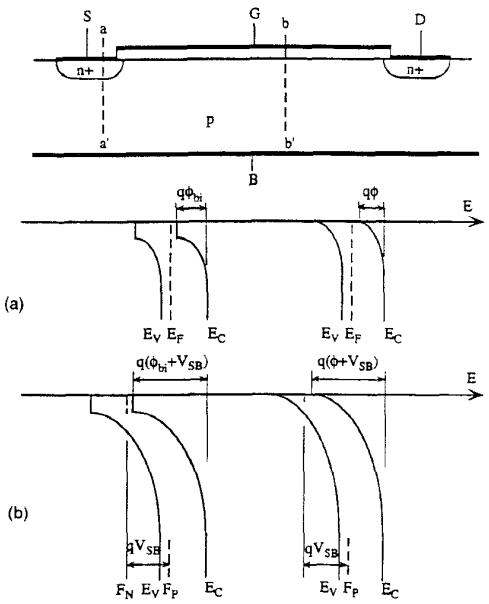

Fig. 2. Energy band diagrams of an n-channel MOSFET inside the semiconductor along line a-a' and along line b-b': (a) When V_{SB}=0, (b)When V_{SB}>0

of *LD*. When the MOSFET is modeled with divided MOSFET's connected in series, the impedances seen from a point in the channel in both lateral directions by the charge at that point in the channel is accounted for in the macromodel. Also, when the MOSFET is modeled with divided MOSFET's connected in series, the overall conductance of a MOSFET is modeled better because the varying threshold conditions along the channel are modeled better as well.

The capacitors C_{GSO} and C_{GDO} model the overlap capacitances between gate and source and between gate and drain, respectively.

The n capacitors, C_{OXi}, i=1,...,n, model the parasitic gate-channel capacitance. The capacitance of each of the n capacitors should be the same and should be the total gate oxide capacitance of the actual MOSFET divided by n.

The diodes D_{BSJb} and D_{BSJs} are to model the bulk-source junction of the actual MOSFET's for both the junction capacitance and the leakage current. D_{BSJb} is for the bottom junction and D_{BSJs} is for the sidewall junction between the bulk and source. Similarly, D_{BDJb} and D_{BDJs} are to model the bottom and the sidewall junction between the bulk and drain.

The diodes, D_{BCi}, i=1,...,n, model the depletion capacitance between the bulk and channel and the leakage current between the channel and bulk (including possible charge pumping into the bulk at high speed switching). In order for the total capacitance of the n D_{BC}'s to be the same as the bulk-channel capacitance of the actual MOSFET, the capacitance of each of the n diodes should be one nth of the bulk-channel capacitance of the actual MOSFET. From Fig. 2, the junctions of the diodes should be one-sided and abrupt with built-in potential of ϕ which is the surface potential at the onset of inversion of the actual MOSFET. The DC zero bias junction capacitance, C_{BCiJ0}, of the D_{BCi} is related to the C_{OXi} by

$$C_{BCiJ0} = \frac{\gamma}{\sqrt{\phi}} C_{OXi} . \tag{1}$$

In order to compare the MOS structure and the capacitor-diode structure shown in Fig. 4, let us first consider the voltage at the node G in the MOS structure when the voltage between node C_i and node B is V_{CBi} and the charge at node C_i is $-Q_{Ci}$. Assuming zero flat band voltage,

$$V_{GCi} = V_{Th} + \frac{Q_{Ci}}{C_{GCi}} = \phi + \gamma\sqrt{\phi + V_{CBi}} + \frac{Q_{Ci}}{C_{GCi}} \tag{2}$$

and

$$V_{GB} = V_{CBi} + \phi + \gamma\sqrt{\phi + V_{CBi}} + \frac{Q_{Ci}}{C_{GCi}} \tag{3}$$

where C_{GCi} is the oxide capacitance of the MOS structure. On the other hand, in the capacitor-diode structure, when the voltage between node C_i and node B is V_{CBi} and the net charge at node C_i is $-Q_{Ci}$,

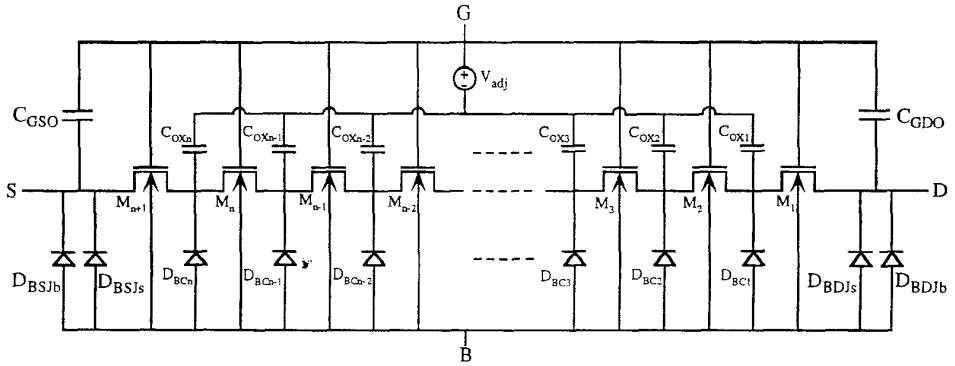

Fig. 3. A charge conserving macromodel, shown for an n-channel MOSFET

V_{adj}=V_{FB}+ϕ

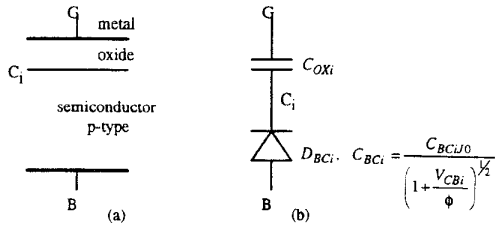

Fig. 4. (a) MOS structure, and (b) capacitor-diode structure

$$-Q_{Ci} = -C_{OXi}V_{GCi} + (V_{CBi} + \phi)\frac{C_{BCiJ0}}{\left(1+\frac{V_{CBi}}{\phi}\right)^{1/2}} \qquad (4)$$

where the built-in potential of the diode is same as the surface potential of the MOS structure. Using Eq. (1) and (4),

$$V_{GCi} = \gamma\sqrt{\phi + V_{CBi}} + \frac{Q_{Ci}}{C_{OXi}} \qquad (5)$$

and

$$V_{GB} = V_{CBi} + \gamma\sqrt{\phi + V_{CBi}} + \frac{Q_{Ci}}{C_{OXi}} \ . \qquad (6)$$

When C_{GCi}=C_{OXi}, it is noted, from Eq. (3) and (6), that the voltage at node G in the capacitor diode structure is ϕ less than the voltage at node G in the MOS structure at the same charge condition and V_{CBi}.

In practical MOSFET's, even at zero bias between the gate and the bulk, the energy band in the semiconductor exhibits some bending. The two main causes are the work function difference of the materials forming the gate and the bulk, and the fixed interfacial charge at the semiconductor-oxide interface. The flat band voltage, V_{FB}, is defined to be the gate-bulk voltage required to flatten the energy band in the bulk of practical MOSFET's and obtained from

$$V_{FB} = V_{T0,practical} - \phi - \gamma\sqrt{\phi} \ . \qquad (7)$$

In the capacitor-diode structure, this non-ideality does not exist. In the macromodel, the voltage at the top of the oxide capacitors should be $V_{adj} = \phi + V_{FB}$ less than the gate voltage of the MOSFET's to simulate the conductance characteristic and the capacitive characteristic simultaneously. This voltage difference is taken care of by the voltage source of $V_{adj} = \phi + V_{FB}$ in the macromodel.

In this macromodel, the conductance along the channel is modeled with the SPICE MOSFET models and the distributed charge along the channel is modeled by the distributed capacitors and diodes along the channel. The non-linear junction capacitances and the depletion capacitance between the bulk and channel are modeled by the capacitance of junction diodes. Because of the distributed nature, the macromodel is expected to simulate the charge injection behavior of MOSFET's even at very high turn-off speed. It should also be able to simulate the charge pumping behavior which is significant at high switching speed. Because all the capacitances shown in Fig. 1 are effectively modeled, it should be accurate. The macromodel is easy to use because it is easily implementable in SPICE.

SIMULATION AND COMPARISON WITH EXPERIMENTAL DATA

To verify the accuracy of the macromodel for MOSFET's, simulation results are compared with the experimental data of Eichenberger and Guggenbuhl [8]. The simple sample-and-hold circuit shown in Fig. 5 was used. The simulation condition and the SPICE input parameters are given in [8] The gate voltage of the MOS switch is designated as V_G in Fig. 5. The SPICE Level 1 model was used for the MOSFET's in the macromodel because the process dependent input parameters necessary for higher level models are not known and the principles used in the development of the macromodel is consistent with the MOSFET model in SPICE level 1. The mobility degradation used by Eichenberger and Guggenbuhl was incorporated in the simulation with the macromodel utilizing the .PARAM statement in SPICE. The simulation measured the clock feedthrough error voltage induced by the switch MOSFET during the turn off period of the sample-and-hold circuit. The error voltage as a function of the signal level and the turn-off slope of the gate voltage was simulated and compared with the Eichenberger and Guggenbuhl's experimental and simulation date using their lumped numerical model in Fig. 6. The original data in [8] covered the 1~5V signal range, but here we concentrate on the more interesting 1V to 4V input range. It is noted that the macromodel gets more accurate at the higher switching speed than the Eichenberger and Guggenbuhl's lumped model. This is attributed to the distributed nature of the macromodel. In order to further investigate the performance of the macromodel at even higher switching speed, the simulation results of the macromodel and Eichenberger and Guggenbuhl's model are compared at 5V/1ns switching speed and shown in Fig. 7. It is noted that as the switching speed increases, the macro model and Eichenberger and Guggenbuhl's lumped model are more different. The intrinsic transit time is estimated to be of the order of 0.1ns assuming minimum MOS switch dimensions, a typical 3 μm process, and 5V switching [3]. Thus, as the

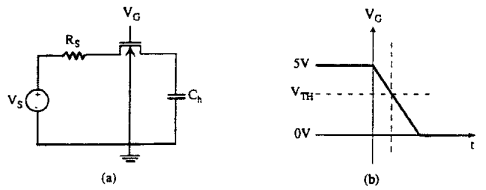

Fig. 5. (a) Simple sample-and-hold circuit, (b) gate voltage

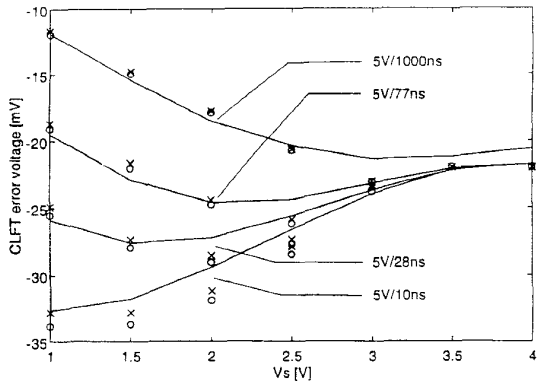

Fig. 6. Comparison of the simulation results using the macromodel (X) with Eichenberger and Guggenbuhl's experimental data (___) and Eichenberger and Guggenbuhl's simulation data (o)

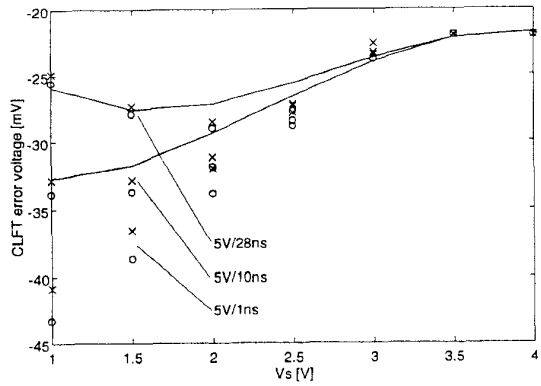

Fig. 7. Comparison at high switching speed: macromodel (X) with Eichenberger and Guggenbuhl's measurements (___) and Eichenberger and Guggenbuhl's model (o)

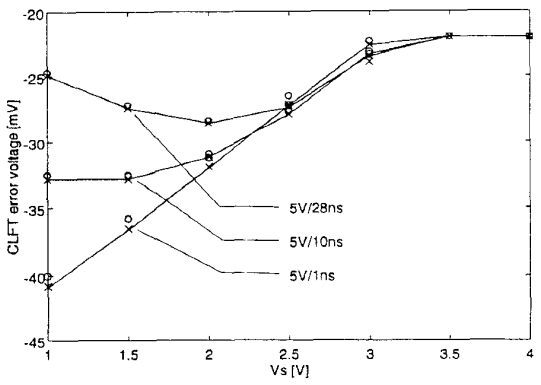

Fig. 8. Comparison of the simulation results with different numbers of MOSFETs in the macromodel: when n=10 (___), when n=5 (X), and when n=1 (o)

switching time gets close to 0.1ns, the lumped model does not accurately simulate the switch.

To determine the appropriate numbers of MOSFET's, capacitors, and diodes to be used in the macromodel, simulations were done with different n in the macromodel keeping the other conditions constant. Results are compared in Fig. 8. When 6 MOSFET's were used, the simulation result was very close to that when 11 MOSFET's were used down to 5V/1ns switching speed, but when 2 MOSFET's were used, the simulation result showed digression and the digression increased as the switching speed was increased to 5V/1ns.

CONCLUSION

A charge-conserving macromodel for MOSFET's suitable for the simulation of the MOS switch induced error has been presented. This macromodel can be used directly in standard circuit simulators such as SPICE. The results of the simulations using the macromodel in SPICE were compared with the experimental and simulation data of Eichenberger and Guggenbuhl to validate the macromodel. Because of the distributed nature, the macromodel should simulate the charge injection behavior of MOSFET's even at very high switching speed.

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