Experimental Test of a Charge Conserving Macromodel for MOSFETs

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ABSTRACT

A charge conserving macromodel convenient to use and effective for the simulation of the charge injection behavior of MOSFET switches has been presented [1, 2]. The macromodel is compared with the SPICE level 2 charge conserving model. The accuracy of the macromodel is tested by measuring the clock-feed-through error of a simple sample-and-hold circuit. The macromodel is accurate even at high switching speed because of its distributed nature and because of its ability to simulate the leakage current to the bulk.

INTRODUCTION

MOSFETs are widely used as switches in analog and mixed signal integrated circuits. Even if MOSFET switches are extensively used as transmission gates, its non-ideality related with clock-feed-through (CLFT) effect degrades the performance of the circuit involving the MOS switch. The CLFT effect of the MOS switch is that it disturbs the adjacent node voltages when it is turned off. The disturbance is due to injection of channel charge when the MOS switch is turned off and coupling through the gate-drain/source overlap capacitances. This behavior of the MOS switch and the techniques to compensate the disturbance have been investigated [3]-[6]. Models for MOSFETs which can be used to simulate the charge injection behavior have been developed [7]-[16].

The analytical or numerical models are difficult to use if the circuit involving MOS switches is not simple. This fact makes the macromodel which is easily implementable in standard simulators like SPICE attractive. The gate-channel capacitance is geometrically distributed. The share of channel charge injected to the drain (or source) node varies depending on the conditions at the nodes (signal level and impedance) and on the time-varying conductance of the switch itself during the turn-off transient. The existing models, which conserve charge at the device terminals, require a manual preset input for the partitioning of the charge injected or divide the gate-channel capacitance and lump it at the drain and source nodes. These models are not adequate to accurately simulate the charge injection behavior of MOSFET switches and simulate the effectiveness of compensation schemes.

CHARGE CONSERVING MACROMODEL FOR MOSFETs

In SPICE, the conductance of MOSFETs is quite well modeled [17]. A model in SPICE level 2 conserves charge, but it is a lumped model and requires an input for the parameter *XQC*, the coefficient of channel charge share attributed to the drain. Thus, the model is inadequate to accurately simulate the charge injection behavior of MOSFET switch at high switching speed. To provide an effective means for simulating the charge injection effect of MOS switches, the macromodel shown for n-channel MOSFETs in Fig. 1 has been proposed [1, 2]. It is based on the nature of the parasitic capacitances in MOSFETs and utilizes the good existing conductance models. This macromodel can be used directly in standard circuit simulators such as SPICE.

Because of the distributed nature, the macromodel should accurately simulate the charge injection behavior of MOSFETs even at very high switching speed. It should also be able to simulate the charge pumping behavior which is significant at high switching speed. The macromodel is easy to use even when the circuits involving MOS switches are complicated. A subroutine implementation of the macromodel directly usable in SPICE is shown in Fig. 2.

COMPARISON WITH SPICE MODELS

Simulations have been done to compare the macromodel with the SPICE level 2 charge conserving model. The output voltage across the holding capacitor, V_h, in the sample-and-hold circuit shown in Fig. 3 was simulated as a

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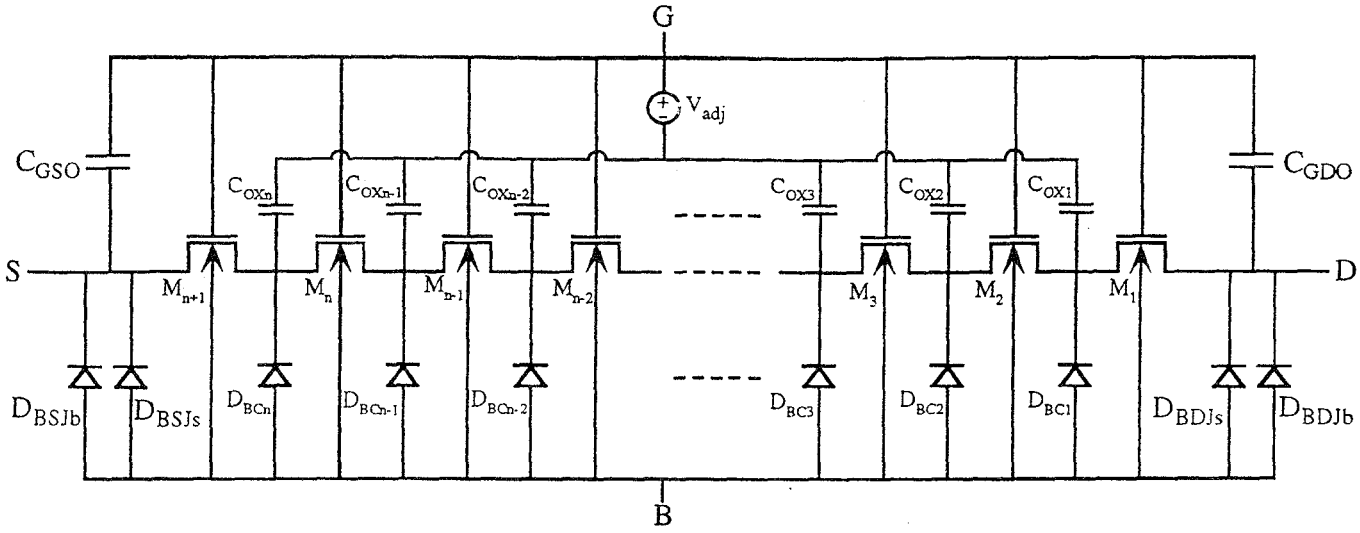

Fig. 1. Charge conserving macromodel, shown for n-channel MOSFET

$V_{adj}=V_{FB}+\phi$

function of time. In the simulation, n=10 was used for the division of the MOSFET, C_h was 2pF, V_S, was 2.5V, and the input resistance, R_S, was 50Ω. A set of standard 1μm CMOS process parameters shown in TABLE 1 was used. The dimension of the switch MOSFET was W=22μm and L=1.086μm such that the settling error in 20ns of the sample-and-hold circuit was less than 16μV. The diffusion area of the drain and source was assumed to be Wx2μm. In Fig. 4, the simulated results using the macromodel and the SPICE level 2 charge conserving model were compared when the ramping rate of the gate voltage is 5V/3ns and when the ramping rate is 5V/1μs.

Using the SPICE level 2 model with *XQC* values less than or equal to 4.999 (*XQC* values less than or equal to 4.999 activate the charge conserving model) were different for different values of *XQC* as shown in Fig. 3. On the other hand, depending on the input signal level and the gate voltage ramping rate, the adequate input value for *XQC* is different. These facts seriously weaken the capability of the charge conserving MOSFET model in SPICE level 2 for the simula tion of the charge injection effect of MOSFETs over a range of signal level and over a range of gate voltage ramping rate.

```
.subckt  Macro 1 2 3 100 (ol ow)
.param   p1      dl=ol/6 darea=ol/5*ow jarea=2e-6*ow
+                jperi=4e-6+2*ow
Dbdjb    100 1           Djb
Dbdjs    100 1           Djs
Cgdo     1 2             Cov
X1       1 2 4 100 202   submac (p1.dl ow)
X1       4 2 5 100 202   submac (p1.dl ow)
X1       5 2 6 100 202   submac (p1.dl ow)
X1       6 2 7 100 202   submac (p1.dl ow)
X1       7 2 8 100 202   submac (p1.dl ow)
M6       8 2 3 100       nm l=p1.dl w=ow
Cgso     3 2             Cov
Dbsjs    100 3           Djs
Dbsjb    100 3           Djb
Vadj     2 202   dc      0.1982
         .subckt submac  1 2 3 100 202 (dl ow)
                 Msub    1 2 3 100   nm l=dl w=ow
                 Coxsub  3 202       Cox
                 Dbcsub  100 3       Dbc
         .ends
.model   nm nmos kp=p5.kpd vto=p3.vto gamma=p3.gamma
                 phi=p3.phi is=0
.model   Cov c   1.173e-10*ow
.model   Cox c   p3.cox*p1.darea
.model   Djb d   cjo=2.628e-4*p1.jarea m=0.5 vj=0.37
+                is=3.2e-14
.model   Djs d   cjo=3.781e-10*p1.jperi m=0.3 vj=0.37
+                is=1.2e-14
.model   Dbc d   cjo=0.5*p3.gamma*p3.cox/sqrt(p3.phi)*p1.darea
+                m=0.5 vj=p3.phi is=4.8e-15 fc=0.95
.ends

.param   p2      von=5 vs=2.5
.param   p3      kp=6.432e-5 vto=0.8667 gamma=0.8088
+                phi=0.6833 ucrit=1e5 uexp=0.2728
+                esi=1.036e-10 cox=1.380e-3
.param   p4      vt=p3.vto+p3.gamma*(sqrt(p2.vs+p3.phi)-
+                sqrt(p3.phi))
.param   p5      kpd=0.5*p3.kp*(1+(p3.ucrit*1e2*p3.esi/p3.cox/
+                (p2.von-p2.vs-p4.vt))**p3.uexp)
```

Fig. 2. SPICE implementation of macromodel

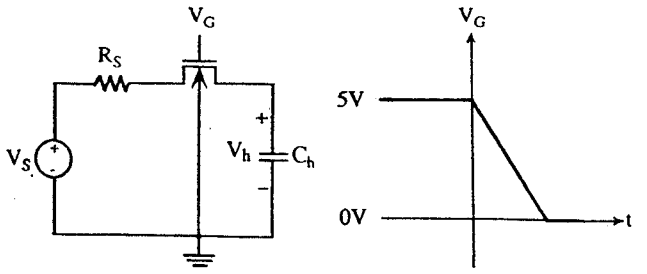

Fig. 3. Sample-and-hold circuit and gate voltage

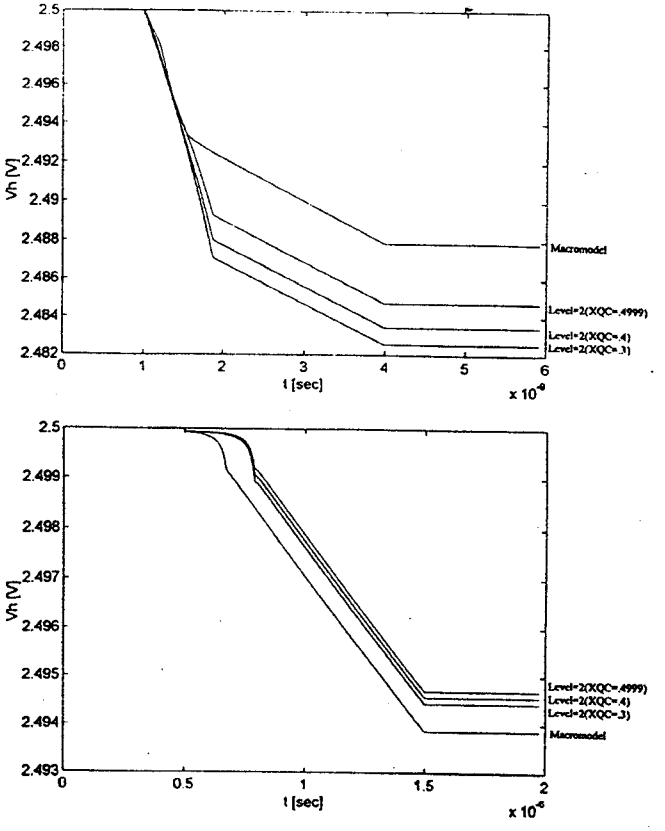

Fig. 4. Comparison of macromodel with SPICE level 2 model

EXPERIMENT AND COMPARISON

To verify the accuracy of the macromodel for MOSFETs, experiments have been done and compared with the simulation results using the macromodel. Fig. 5 shows the experimental setup. The simple sample-and-hold circuit followed by a source follower was fabricated in a standard 2μm CMOS process. The micrograph of the circuit is shown in Fig. 6. The dimension of the MOSFET switch was designed to be W=50.40μm and L=1.490μm such that the CLFT error of the sample-and-hold circuit is large enough to be accurately measured. The circuit parameters and the SPICE input parameters are given in TABLE 2.

The SPICE Level 1 model was used for the MOSFETs in the macromodel because the principles used in the development of the macromodel is consistent with the MOSFET model in SPICE level 1. The mobility degradation

TABLE 1. SPICE input parameters

parameter	value	parameter	value
K'	6.432×10^{-5} A/V^2	V_{max}	9.317×10^{4} m/s
V_{TO}	0.8667 V	T_{OX}	2.502×10^{-8} m
γ	0.8088 V$^{1/2}$	C_J	2.628×10^{-4} F/m^2
ϕ	0.6833 V	MJ	0.5
$UCRIT$	1×10^{5} V/cm	C_{JSW}	3.781×10^{-10} F/m
$UEXP$	0.2728	$MJSW$	0.3
N_{sub}	8×10^{15} /cm^3	ϕ_B	0.37 V
N_{fs}	2×10^{11} /cm^2	C_{ox}	1.380×10^{-3} F/m^2
X_J	3×10^{-7} m	C_{OV}	1.173×10^{-10} F/m
μ_0	7×10^{2} cm^2/(Vxs)	C_{gbo}	3.036×10^{-8} F/m

was incorporated in the simulation with the macromodel utilizing the .PARAM statement in SPICE, as shown in Fig. 2. The mobility degradation incorporated in the simulation modifies K', depending on Vs [7, 17] by

$$K'_{modified} = \frac{1}{2}K'\left\{1+\left[\frac{UCRIT\varepsilon_{Si}}{C_{OX}\left(V_{GON}-V_S-V_{TH}\right)}\right]^{UEXP}\right\} \quad (1)$$

where

$$V_{TH} = V_{T0}+\gamma\left(\sqrt{\phi+V_S}-\sqrt{\phi}\right). \quad (2)$$

The CLFT error voltage, defined by

$$\text{CLFT error}=V_{h,f}-V_S, \quad (3)$$

where $V_{h,f}$ is the voltage across the holding capacitor after the gate voltage become zero and V_S is the signal voltage, was simulated and measured as a function of the signal level and the turn-off slope of the gate voltage. The comparison is shown in Fig. 7 for five different turn-off ramping rate ranging from 5V/1μsec to 5V/5ns and for eight different signal voltages ranging from 0.5V to 4V.

The maximum difference between the simulated and measured CLFT errors is 2.48mV while the magnitude of the measured CLFT error is maximum 60mV. In the simulation, the applied ramp voltage is assumed to be linear but the observed waveforms were not quite linear, especially at higher ramping rate. This must have attributed to the larger discrepancy between the simulated and measured

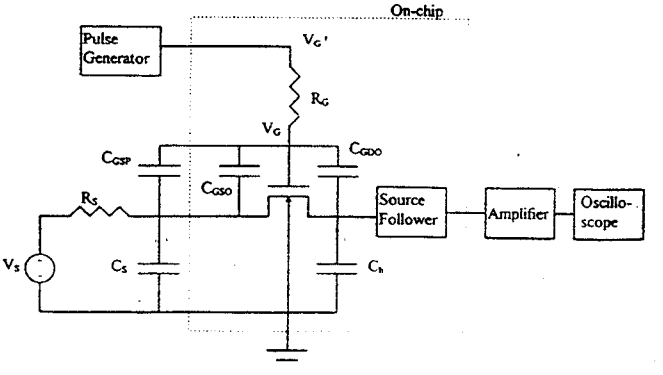

Fig. 5. Experimental setup

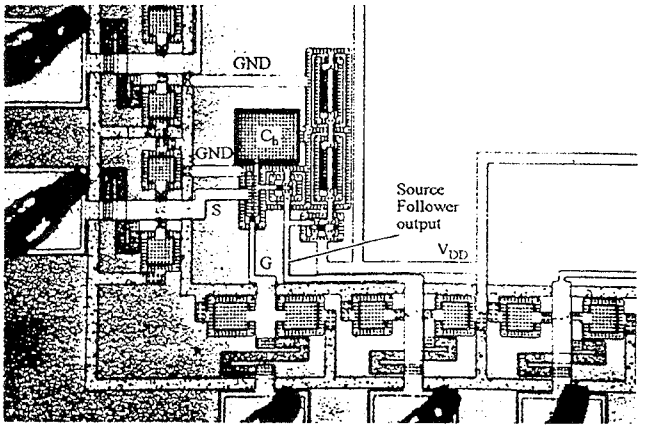

Fig. 6. Micrograph

TABLE 2. Circuit and SPICE input parameters

parameter	value	parameter	value
R_S	50 Ω	C_h	1.937 pF
R_G	425 Ω	C_S	1 nF
		$C_{GSP} + C_{GSO}$	9.3pF
K'	4.549×10^{-5} A/V^2	C_J	1.038×10^{-4} F/m^2
V_{TO}	0.8756 V	MJ	0.6604
γ	0.2200 V$^{1/2}$	C_{JSW}	2.169×10^{-10} F/m
ϕ	0.6 V	$MJSW$	0.1785
$UCRIT$	5.916×10^{4} V/cm	ϕ_B	0.8 V
$UEXP$	0.1592	C_{ox}	7.938×10^{-4} F/m^2
		C_{gdo}	2.833×10^{-10} F/m

results at the high ramping rate. The process parameter values used in the simulation were the lot average values or the values extracted from a selected wafer. During turn-off transient, the MOSFET switch in the sample-and-hold circuit remains either in cutoff region or in deep ohmic region (small V_{DS}). It is believed that the inaccurate process parameters for the specific test chip and for the region of operation also degraded the accuracy of the simulation results of the macromodel.

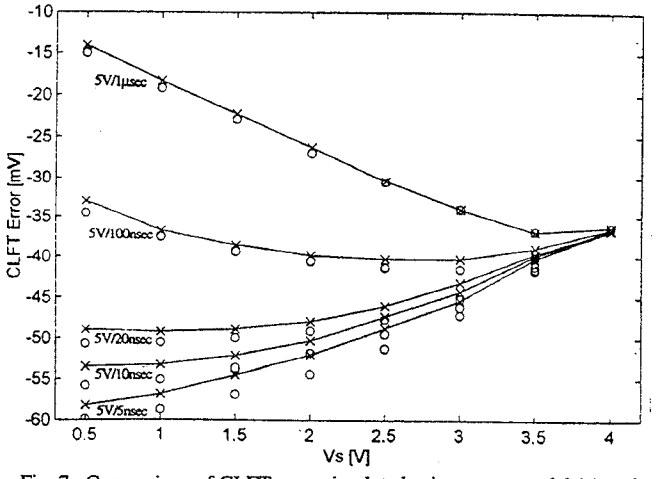

Fig. 7. Comparison of CLFT error simulated using macromodel (o) and experimental data (-x-)

CONCLUSION

A charge-conserving macromodel for MOSFETs suitable for the simulation of the MOSFET switch induced error was compared with a SPICE level 2 model and experimental results. This macromodel can be used directly in standard circuit simulators such as SPICE. Because of the distributed nature, the macromodel simulates the charge injection behavior of MOSFETs accurately even at very high switching speed.

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