Field Programmable Logic Gates Using GMR Devices

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I. INTRODUCTION

The usage of GMR devices so far has been limited to sensors, non-volatile memory and disk drive read heads. However, the fact that these devices exhibit a digital behavior lends them to the building of logic gates. Furthermore, due to the simplicity of changing the resistance setting (digital value) of a GMR device, this technology is suitable as field programmable logic devices (FPLDs).

The physical and magnetic descriptions of GMR memory devices can be found in [1] and [2]. For this purely digital application, a simple schematic symbol and model for the device are shown in Fig. 1. While the techniques presented here are applicable to many GMR bit configurations, for this figure, an asymmetrical GMR sandwich film ("pseudo spin-valve") has been assumed.

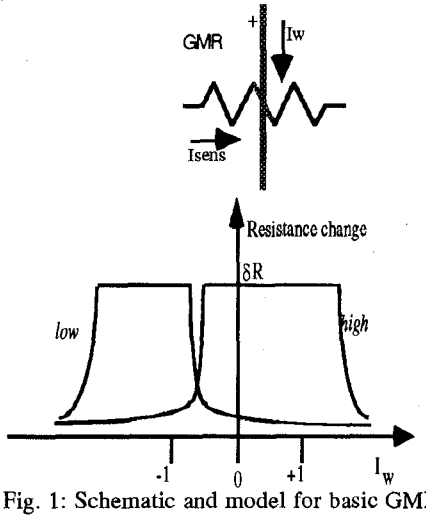

Fig. 1: Schematic and model for basic GMR element

The definitions for *high* and *low* logic values presented herein and used throughout this paper are arbitrary and are changeable to suit the particular GMR technology being used. Given zero word current (I_W=0) or a positive word current (I_W>0) in the range of 1-5 mA, the resistance of the device is approximately R+δR if it is programmed *high* (Fig. 2) and is approximately R if programmed *low* (Fig. 3). δR is defined as shown in Fig. 1. If a negative word current is applied, again in the range of 1-5 mA, then the resistance of a device programmed *high* (Fig. 2) is R and the resistance of a device programmed *low* (Fig. 3) is R+δR. Depending on the GMR technology, the resistance change at I_W=0 can be very close to the values when a positive I_W is applied. So by definition, a logic 0 input to this device is represented by $I_W \geq 0$, and a logic 1 input is represented by applying $I_W < 0$. TABLE I summarizes the operating points of the device.

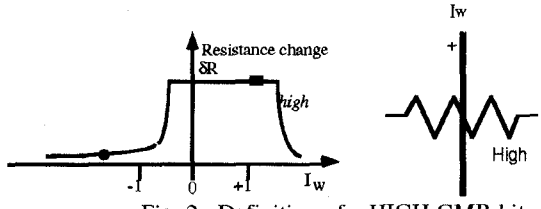

Fig. 2. Definition of a HIGH GMR bit

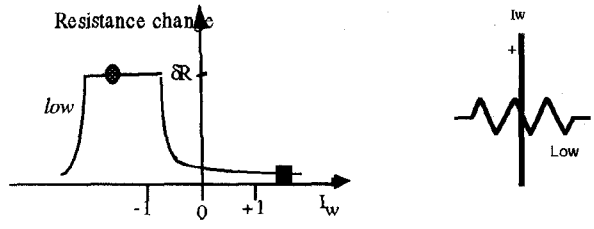

Fig. 3. Definition of a LOW GMR bit

TABLE I
RESISTANCE VALUES FOR A PROGRAMMED GMR BIT

Input Value ▶ / BIT Program ▼	logic 0 ($I_W \geq 0$)	logic 1 (I_W neg)
LOW	R ■	R + δR ●
HIGH	R + δR ■	R ●

A device is programmed *high* or *low* by simply applying a large negative or positive (approximately 25mA) word current, respectively (Fig. 4). This makes the device very easily programmable in the field. By increasing I_w beyond the evaluation level, the GMR bit will change its programmed state. For example, Fig. 4 depicts a change in a GMR bit program from HIGH to LOW by increasing I_w for a few nano-seconds.

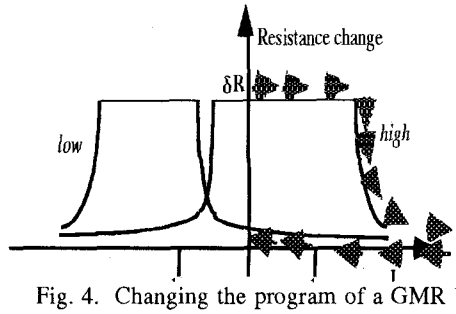

Fig. 4. Changing the program of a GMR bit

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II. BASIC FPLD STRUCTURE

A basic voltage sensing FPLD structure is shown in Fig. 5 and will be referred to as a gate, and each GMR device will be referred to as a bit. (Several sensing schemes are possible, e.g. tying the left end of the string to a voltage source and sensing the current. Due to the page limitation, only a voltage sensing scheme is presented.) For the sake of illustration, a 4-input gate is shown and will be analyzed. The bottom bit of each pair is the evaluation bit and the top bit is the reference bit. Programming the reference and evaluation bits *high* or *low* configures the logic function of the gate and enables the inclusion or exclusion of any particular input from the function. The maximum number of inputs a gate can have is dependent on the process and GMR device size. With existing auto-zero techniques applied in MRAM memories[3], gate configurations of up to 60 inputs appears possible.

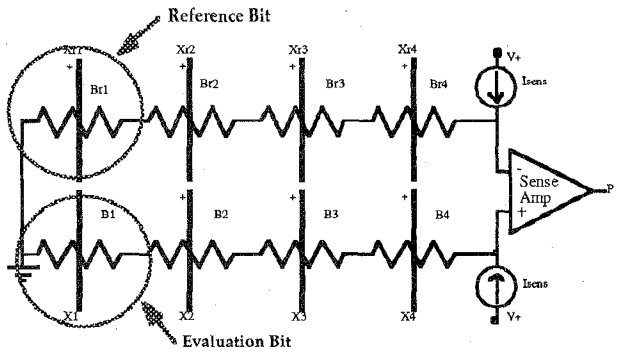

Fig. 5. Basic field programmable circuit

Using a mixture of a Boolean function (exclusive-or) with regular addition, subtraction and multiplication functions, the differential input of the amplifier for the above FPLD configuration can be written as

$$v_+ - v_- = \Big[\big(\{B_1 \oplus X_1\} + \{B_2 \oplus X_2\} + \{B_3 \oplus X_3\} + \{B_4 \oplus X_4\}\big) - \big(\{B_{r1} \oplus X_{r1}\} + \{B_{r2} \oplus X_{r2}\} + \{B_{r3} \oplus X_{r3}\} + \{B_{r4} \oplus X_{r4}\}\big)\Big] \delta RI_{sens} + V_{os} \quad (1)$$

where B_i and B_{ri} are the programmed values of the *ith* evaluation and reference bits, respectively, (1 or 0 for *high* or *low*), X_i and X_{ri} are the logic value on the inputs to the evaluation and reference bits, respectively (1 or 0) and V_{OS} is the input offset voltage on the sense amp. (Note that all the "+" operators in equations (1), (2) and (3) are addition operations). For example, the FPLD in Fig. 5 may be programmed as a 2-input through 4-input NOR gate by programming all the bits in the reference leg *high* and setting the X_{ri}'s to 0 (no current input needed as seen in Fig. 1). All the bits in the evaluation leg are also set to *high*. and the gate is evaluated by applying 1's and 0's to the X_i inputs. Fig. 6 shows the NOR configuration which reduces equation (1) to

$$v_+ - v_- = \left[\begin{pmatrix} \{B_1 \oplus X_1\} + \{B_2 \oplus X_2\} \\ + \{B_3 \oplus X_3\} + \{B_4 \oplus X_4\} \end{pmatrix} - 4\right] \delta RI_{sens} + V_{os} \quad (2)$$

and since all the *B's* are *high* equation (2) further reduces to

$$v_+ - v_- = \left[\left(\overline{X_1} + \overline{X_2} + \overline{X_3} + \overline{X_4}\right) - 4\right] \delta RI_{sens} + V_{os} \quad (3)$$

where $\overline{X}$ is the Boolean complement of X. The logic value of the gate thus becomes (the "+" here is an OR operator):

$$P = \overline{X_1 + X_2 + X_3 + X_4}. \quad (4)$$

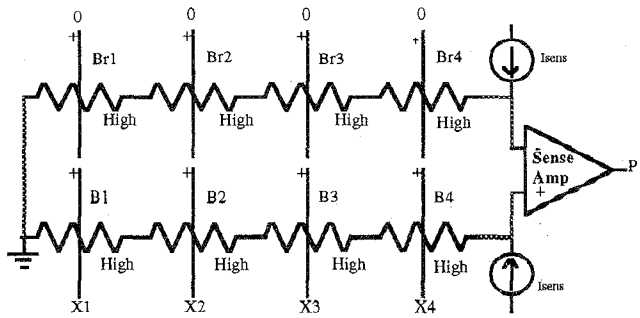

Fig. 6. NOR gate configuration.

An input is disabled (excluded from the evaluation) for this gate by shorting the X_i and the X_{ri} of that input together.

For the above NOR gate configuration, the offset voltage of the sense amplifier is assumed to be positive. Furthermore, the sense amplifier has to be designed such that:

$$\delta RI_{sens} > V_{os} \quad \text{and} \quad \delta RI_{sens} - |V_{os}| > |V_{noise}| \quad (5)$$

where $|V_{noise}|$ is the absolute maximum random noise value and δRI_{sens} is the minimum voltage change in the system and is referred to as an LSB.

In the case where Vos <0, one of the reference bits is programmed LOW to compensate for the negative offset. The conditions in equation (5) must still hold. Another method of compensating for the uncontrollability of V_{os} is to add a pair of trim bits to the end of each gate (one on the reference leg and one on the evaluation leg). These bits can then be programmed the same or opposite to generate the desired offset for the gate. A third solution is to add a 1/2 LSB to one of the legs in effect controlling the sign of the offset voltage.

III. OTHER CONFIGURATIONS

Assuming all X_{ri}'s are 0, other standard logic functions can be programmed as follows:

NAND (Fig. 7): B_i *high* and B_{ri} *low*; assuming $V_{os}<0$. If $V_{os}>0$ then one of the reference bits should be programmed high.

OR (Fig. 8): B_i *low* and B_{ri} *low* , assuming $V_{os}<0$. If $V_{os}>0$ then one of the reference bits should be programmed high.

AND (Fig. 9): B_i *low* and *Bri high*, assuming $V_{os}>0$. If $V_{os}<0$ then one of the reference bits should be programmed low.

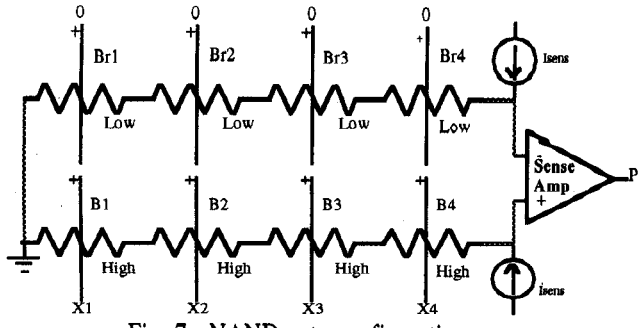

Fig. 7. NAND gate configuration.

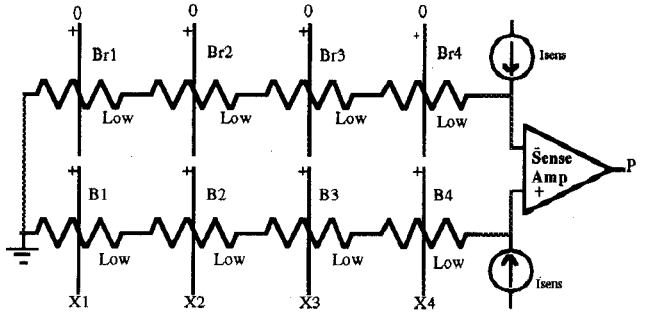

Fig. 8. OR gate configuration.

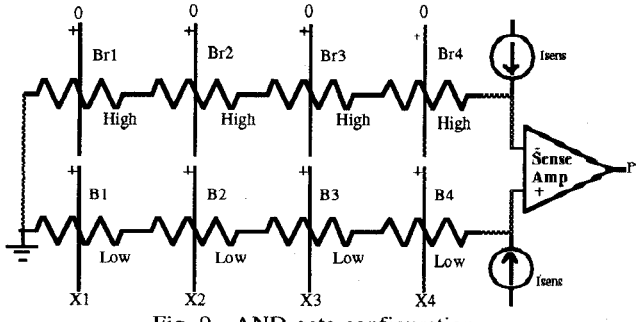

Fig. 9. AND gate configuration.

More complex logic functions can be programmed by mixing and matching the programmability and the connectivity of the inputs. An example of a more complex and very useful function is a majority function. Fig. 10 shows a majority gate that outputs a logic 1 when the number of 1's at the inputs is greater than or equal the number of 0's (assume $V_{OS}>0$). Note that the reference and evaluation inputs are shorted together.

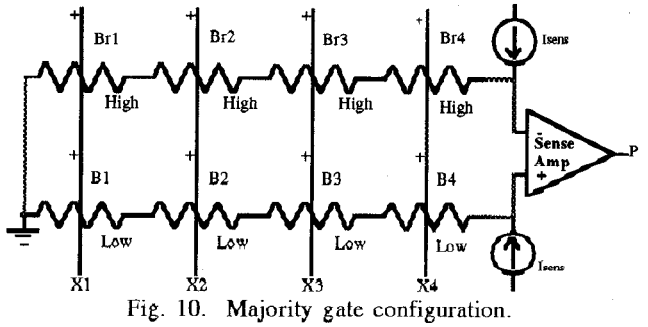

Fig. 10. Majority gate configuration.

For all of the above configurations, an input is eliminated from the gate by simply programming the corresponding reference and evaluation bits alike and shorting their inputs together.

IV. Logic Evaluation Schemes

As noted earlier, a specific input is evaluated by applying a current to it of magnitude 1 to 5 mA depending on the GMR technology (advances in GMR technology are continually bringing that number down). Assuming a 1mA current is needed, at first glance, a 4-input gate could require 4 mA to evaluate. This is not the case, the same current can be used to evaluate multiple bits across different gates. A particular scheme is shown in Fig. 11. The entire gate is evaluated using 1mA, in addition, this scheme allows for the cascading of the FPLDs. Another method for further reducing the evaluation and programming current requirements is the winding of the metal strip over the magnetic material as shown in Fig. 12. This bit configuration requires 80% less current than the bit in Fig. (1). The cost is an increase in the layout area of the bit and potentially a need for a permalloy "keeper" layer over the bit to smooth the magnetic field.

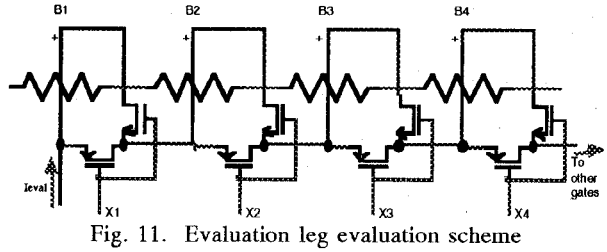

Fig. 11. Evaluation leg evaluation scheme

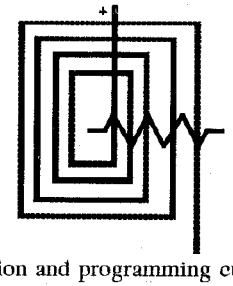

Fig. 12. Evaluation and programming current reduction

V. Conclusions

This paper summarizes the basic methodology for building field programmable logic functions using GMR devices. The size of the gates and the properties of the sense amplifier are a function of the particular GMR technology used, device matching and the magnitude of the sense current available. A test chip is currently in fabrication.

References

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