A SIMULATION ENVIRONMENT FOR PIPELINED ANALOG-TO-DIGITAL CONVERTERS[1]

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ABSTRACT

This paper describes a detailed functional simulator for the design and characterization of single and parallel pipelined analog-to-digital converters. It is a user-friendly program which allows the user to specify the A/D parameters and thus target a particular architecture. Since high resolution is achieved by error correction algorithms, digital self-calibration is also incorporated. Modular design allows the user to replace any component model with more complex modules as demanded by the application. The environment also has the capability to perform single and double tone testing to determine the spurious free dynamic range of the ADC being considered. Since simulation of architectures at the functional level is fast and easy as opposed to a generalized mathematical package, the design cycle time is reduced considerably.

1. INTRODUCTION

Most of the present day high speed/high resolution A/D converters are pipeline architectures [1]-[4]. In the past, there have been some functional simulators for mixed signal and analog sampled data systems like MIDAS [5], but there has not been any available simulator specifically targeted towards pipelined A/D converters. This work is an attempt at developing a specialized simulator for single and parallel pipeline A/D converters. The program also has the capability to perform single tone and double tone testing for pipelines and to perform FFT's to determine the spurious free dynamic range.

Fig. 1 shows a generalized view of a parallel pipeline A/D converter architecture. Each individual pipeline is composed of several pipelined cells. Many possible architectures and resolutions are possible for the construction of the individual cells. Common implementations of pipelined A/D converters have normally used a 1-bit resolution per cell. However, the simulator allows for a user-defined number of bits resolved per cell.

A flow chart of the program is shown in Fig. 2 and the individual parts are described in the following sections of this paper. Section 2 describes the conversion characteristics of a single cell, section 3 describes the models for the cell components used in the simulator, section 4 covers digital self-calibration techniques incorporated namely the bootstrapping algorithm [6],[7], section 5 describes the input and output formats, the program flow and the algorithms used in the conversion and calibration, section 6 presents some experimental results, section 7 describes the single and double tone testing for the SFDR and the FFT function which can be performed and finally, section 8 concludes the paper.

[1]This work was supported by a grant from Texas Instruments

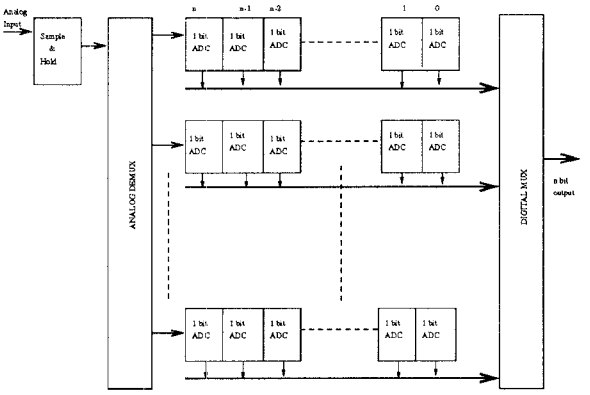

Figure 1. Time interleaved multiple pipeline architecture

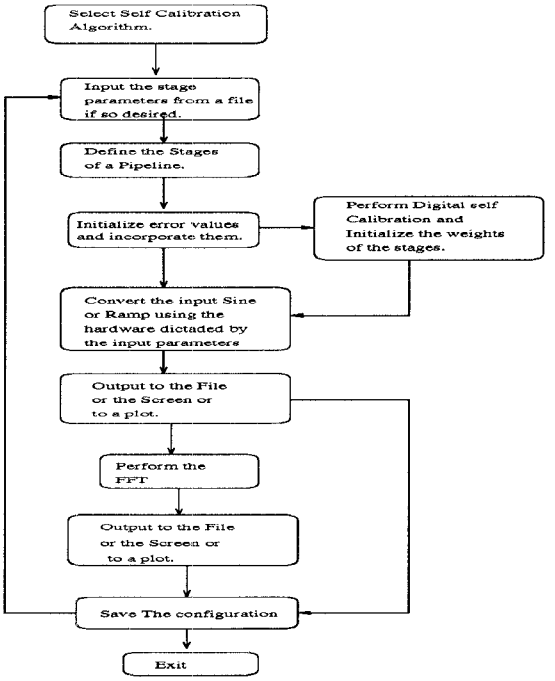

Figure 2. Flow chart of the program

2. SINGLE CELL ARCHITECTURE

In this section, a description of how a general pipeline converter works is given. The schematic of a single converter

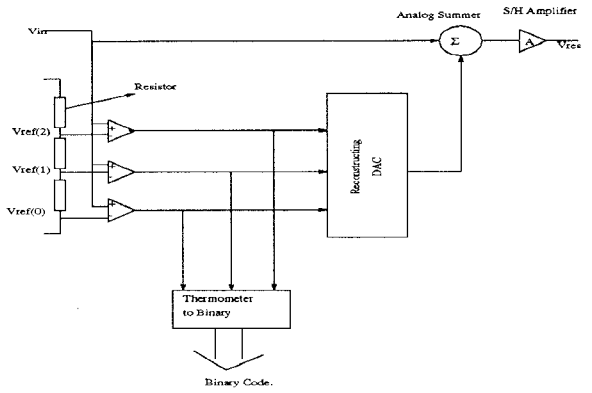

Figure 3. Example of a Single Converter Stage

stage is shown in Fig. 3. Let the total number of converters be L-1 and let l denote the lth converter. The incoming signal V_{in} is compared against a number of reference or ADC levels, using a flash converter. The comparator outputs provide a rough digital representation of the input voltage in thermometer format. If we call the digital output code c_l, and there are M comparators, the $M+1$ possible outputs are

$$\begin{aligned} c_l &= 0 \quad for \quad V_l^{in} < V_l^{ref}[0] \\ &\quad 1 \quad for \quad V_l^{ref}[0] \le V_l^{in} \le V_l^{ref}[1] \\ &\quad \ldots\ldots\ldots \\ &\quad M \quad for \quad V_l^{ref}[M-1] \le V_l^{in} \end{aligned} \tag{1}$$

Depending on the output code, one of these M + 1 possible voltages, V^{DAC} (DAC stands for Digital to Analog Converter), is subtracted from the input signal. The difference $V^{in} - V^{DAC}$ is then amplified by the sample/hold amplifier in order to restore the signal to a level compatible with the next stage. The resulting signal is called the residue. For any given c_l, a general equation can be written for the residue V_l^{res} as a function of V_l^{in}.

$$V_l^{res} = (V_l^{in} - V_l^{DAC}[c_l])A_l \tag{2}$$

$$Rearranging, \qquad V_l^{in} = V_l^{DAC}[c_l] + \frac{V_l^{res}}{A} \tag{3}$$

From the pipeline structure, we know that $V_{l-1}^{in} = V_l^{res}$. Therefore, the input voltage for that stage can be written as

$$V_l^{in} = V_l^{DAC}[c_l] + \frac{V_{l-1}^{DAC}[c_{l-1}]}{A_l} + \frac{V_{l-1}^{res}}{A_l A_{l-1}} \tag{4}$$

For an n stage pipeline the input voltage can be represented as

$$\begin{aligned} V^{in} &= V_{L-1}^{DAC}\frac{A^L}{A^L} + V_{L-2}^{DAC}\frac{A}{A_{L-1}}\frac{A^{L-1}}{A^L}\ldots \\ &+\ldots. + V_0^{DAC}\frac{A^{L-1}}{A_{L-1}\ldots A_1}\frac{A}{A^L} + \frac{V_0^{res}}{A_{L-1}\ldots A_0} \end{aligned} \tag{5}$$

3. MODEL OF A SINGLE STAGE

The model used for the single stage is very flexible. The number of stages, the number of redundant stages and the gain/stage are initialized. The structure of each stage is set

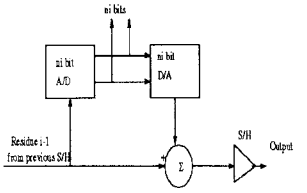

Figure 4. Model of the single stage

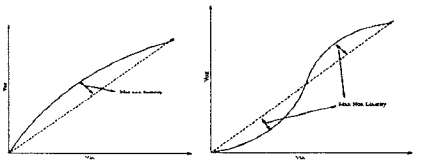

Figure 5. Single bow and double bow non linearity model

up as a module which targets a specific architecture. This can be replaced by the user to target the users own model. Three kinds of component errors are possible in Fig. 4. These are errors in the gain of the Sample/Hold amplifier (δA_l), errors in the flash ADC reference levels (δADC) and errors in the reconstructing DAC (δDAC). Depending on the user specification, the distribution of these errors is either uniform or extreme. The gain(A), the DAC level and the ADC levels of each stage l are stored as

$$A[l] = A + \delta A_l \tag{6}$$

$$ADC[i][l] = ADC[i][l] + \delta ADC[i][l] \tag{7}$$

$$DAC[i][l] = DAC[i][l] + \delta DAC[i][l] \tag{8}$$

$$V_{res} = V_{res} + noise + non - linearity \tag{9}$$

where i is the output code shown in (1). The errors in the above equations are generated randomly. Output referred noise and non-linearity are also added to the residue at each stage as described above. The conversion is done by adding the weight of the stage divided by the gain of the stage with the incoming residue to generate the output residue. The output of the flash A/D produces the digital code from each stage.

3.1. Opamp Model

The gain of the opamp or sample/hold is initialized at the beginning of the program. The model allows for the maximum equivalent output non-linearity(le) for each stage to be incorporated. The non-linearity can be modeled as a single bow or as a double bow as shown in Fig. 5. The non-linearity for a single bow is modeled as in (10) and for the double bow as in (11).

$$SingleBow = 4 * le * V_{res} * (1 - V_{res}) \tag{10}$$

$$DoubleBow = 64/3 * le * V_{res} * (1 - V_{res}) * (V_{res} - 0.5) \tag{11}$$

4. ACCURACY BOOTSTRAPPING

Accuracy bootstrapping [6] is a form of digital self calibration wherein the A/D converter is used to calibrate itself. To illustrate the concept let us use a 1.5 bits/stage architecture as shown in Fig. 6. The contribution of each stage to the conversion result is represented as a weight. Thus

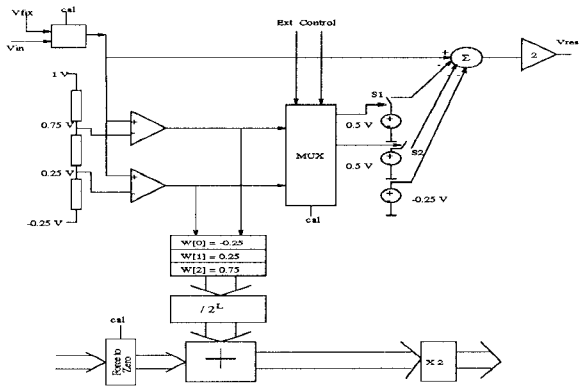

Figure 6. Single Stage Modified for Calibration

the input voltage in (5) is represented as a sum of weighted coefficients and can be written as

$$DigitalOutput = [[[[[\frac{W_{L-1}}{A^L}]A + \frac{W_{L-2}}{A^L}]A + ...]A + \frac{W_0}{A^L}]A \quad (12)$$

Comparing (5) and (12), we get

$$W_l^i[c] = \frac{V_l^{DAC}[c]A^{(L-1-l)}}{A_{L-1}....A_{l+1}} \quad (13)$$

which is the weight of each stage. The value of the weights, W, is stored in a RAM. The basic idea of accuracy bootstrapping is to individually measure all the DAC levels of each converter stage, using the remaining stages of the pipeline. The measurements are used to update the values of the weights stored in the RAM, and the process is repeated until each stage has been calibrated. The algorithm described in [7] has also been implemented in the simulator.

5. PROGRAM DESCRIPTION

5.1. Input and Output Format

The stage parameters can be initialized either at the command line or through an input file. The parameters initialized are the number of stages, the number of redundant stages, the gain per stage and the calibration algorithm used. Then, the errors in the various components of Fig. 6, the gain error, the flash ADC errors, the DAC errors, the non-linearity and the output referred noise are initialized as percentages of the full scale. The A/D can then be simulated with or without these errors. The errors are incorporated in a random fashion. The output of the program for different inputs can be output to the screen or to a file in an easily readable format or it can be plotted out.

5.2. Routines Used

The various routines used within the software are for:

1. Ramp or Sinusoidal Input : The A/D can be simulated with both sinusoidal or ramp inputs which sweep over the entire range in user specified steps.

2. INL and DNL calculation : Two of the most important ADC specifications are the INL and DNL specifications. INL (Integral Non Linearity) is the maximum deviation of the actual transition points in an ADC's transfer characteristic from the straight line drawn between the end points (first and last code transitions). DNL (Differential

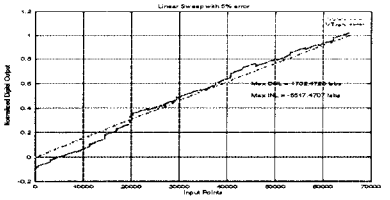

Figure 7. Uncalibrated ADC Transfer Characteristic

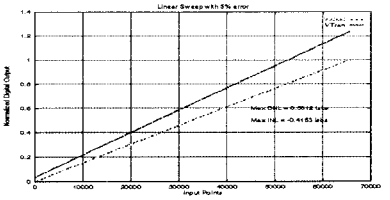

Figure 8. Calibrated ADC Transfer Characteristic

Non Linearity) is defined as the difference between the ideal bin width of the converter and the actual width of each bin . A bin is defined as the set of input voltages yielding the same output code.

3. Fast Fourier Transform (FFT) : The Fast Fourier Transform can be performed on the output with plotting capabilities.

Fig. 2 gives an overview of how the program works. As can be seen, the various modules for the components especially the conversion stage can be replaced by individual models and thus the user can use the program to target his particular application.

6. RESULTS

The Fig. 7 shows the transfer curve for a 16 bit A/D with two redundant stages with a 5% error in the component values. Note the non-linearity in the curve before the calibration is performed.The INL and DNL are -5517.47 lsb and 1732.47 lsb respectively. Fig. 8 shows the transfer characteristic for the same A/D with accuracy bootstrapping applied. The INL and DNL are -0.4153 lsb and 0.5012 lsb respectively. As can be seen, accuracy bootstrapping linearizes the transfer characteristic. A global offset and gain error is present which can easily be corrected.

6.1. Multiple Parallel Pipelines

Parallelism in the signal path is one way to increase conversion speed. The speed critical input S/H and interstage circuits are time inter leaved i.e the various paths or ADC's are multiplexed in time [8] as shown in Fig. 1 as if they are effectively a single converter operating at a much higher

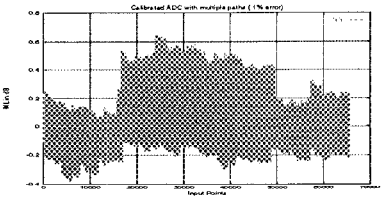

Figure 9. INL error of 16 bit multi-pipe ADC after Calibration

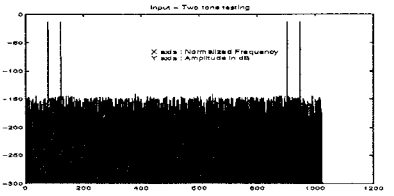

Figure 10. FFT of the Input

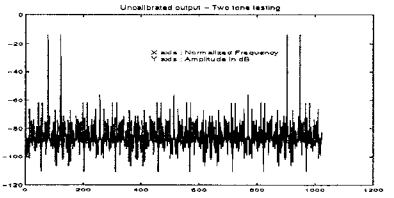

Figure 11. FFT of the Output with No Calibration

sampling rate. The program has the capability to simulate parallel pipelines with different error and non-linearity parameters for each of the individual pipelines. Using the program, we have shown a technique for calibrating parallel pipes called global normalization, which is described in [9]. Fig. 9 shows the INL errors after calibration of a 16 bit 4 pipeline ADC. The DNL error for the same example was 0.79 lsb.

7. FAST FOURIER TRANSFORM (FFT)

SFDR (Spurious Free Dynamic Range) is defined as the ratio in decibels between the magnitude of the fundamental component and the magnitude of the largest harmonic or inter-modulation product. Offset, gain and timing mismatches between the multiple channels give rise to fixed pattern effects which in the frequency domain are manifested as spurious harmonics [10].

In single tone testing, the input is a single sine wave. The FFT of a single Tone should be a single pulse at N*(frequency of sine wave)/2π.

In two tone testing, two sinusoids, whose periods are not integral multiples of each other are applied to the ADC and the output frequency spectrum is studied. The ratio of the two periods is an irrational number. Fig. 10 shows the FFT of the input. Fig. 11 shows the output spectrum of the ADC with no calibration applied. Fig. 12 shows the spectrum if calibration is applied to the individual pipes.

Finally, Fig. 13 shows the spectrum with global normalization of the offset and gain mismatches. As can be seen, the SFDR has improved from approximately 50dB in the uncalibrated A/D converter to approximately 100dB with full calibration applied.

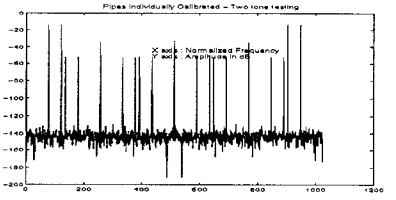

Figure 12. Individually calibrated channels

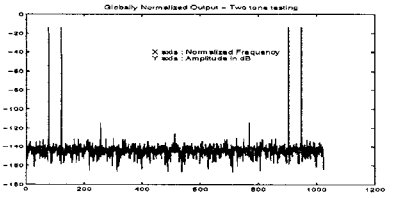

Figure 13. Output with Normalization

8. CONCLUSION

This paper described a simulator which can be used in the design of single and parallel pipelined converters. It is implemented as 4500 lines of C code on HP-UX platform. A limited functionality PC version is also available. Run time on the system for a linear ramp sweep in steps of 1 lsb for a 16 bit conversion with 2 extra stages was 46.84sec. Future improvements in this could involve incorporating higher models into the individual components and also incorporating other calibration algorithms.

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