# A 1.0625 Gbps PECL Line Driver

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**Abstract - A Line Driver capable of driving pulses on coaxial cables or laser driver packages has been designed to serve as the output of a 1.0625 Gbps Fibre Channel transmitter. This driver was designed in 0.5 mm CMOS technology and generates pulses of 1 ns width at PECL levels which are capable of driving 75 Ω, the characteristic impedance of a standard coaxial line.**

## I. INTRODUCTION

Transmitter chips capable of operating at gigahertz speeds are being designed for high speed point-to-point communication between workstations, mainframes etc., or for connections to storage devices and peripherals etc. The Line Drivers on these chips drive pulses on the communication channel, which could be coaxial or twisted-pair cables, laser diode interfaces etc.

Communication channels generally have a low characteristic impedance. Therefore, Line Drivers for high speed communications are output buffers having low output impedance and high output current drive. They also need to compensate for degradation of the pulse due to device and package parasitics and channel dispersion due to the finite bandwidth of the channel. Other considerations to be taken into account while designing a Line Driver are linearity, bandwidth, stability and speed of operation (rise/fall times).

Bipolar devices, with their high transconductance and output drive capability, have traditionally been used in the output stage of high speed Line Drivers. This approach necessitates the use of Bipolar or BiCMOS technology. However, in our design, we have focussed on obtaining the requisite performance with MOSFETs to achieve integrability with higher levels of digital circuitry in a standard CMOS technology.

### *A. Standard*

The ANSI X3T11 Fibre Channel Standard, which defines the mapping of Upper Layer Protocols (ULP's) onto the Physical Layer and the specifications for driving pulses on the Physical Layer is a standard for 1.0625 Gbps serial communication on the Fibre Channel. The transmitter for which the present Line Driver has been designed is compliant with the Fibre Channel standard.

### *B. Signal levels*

PECL (Pseudo Emitter Coupled Logic) signal levels have been specified for the output pulses. These require a minimum single-ended peak-to-peak output voltage swing of 0.6 V and a maximum of 1.4 V around $V_{DD}$ - 1.32 V. Here $V_{DD}$ was chosen to be 3.3 V. The maximum rise/fall time allowable has been defined by the Fibre Channel Standard to be 350 ps (20% to 80%), and the output impedance presented by the coaxial cable, for which the transmitter has been designed, is 75 Ω. The output port is illustrated in Fig. 1.

The PECL level output signals are available in differential and single-ended form. The single–ended outputs are $v_{o1}$ and $v_{o2}$ in Fig. 1. The differential output is $v_{o1}$ - $v_{o2}$. Differential signals result in increased noise immunity and are thus preferred for high speed transmissions.

## II. DESIGN APPROACH

### *A. Requirements*

The input to the Line Driver is assumed to be NRZ serialized data at TTL levels capable of driving minimum sized inverters. Thus the design goal is to translate these signals into PECL level output signals capable of driving a

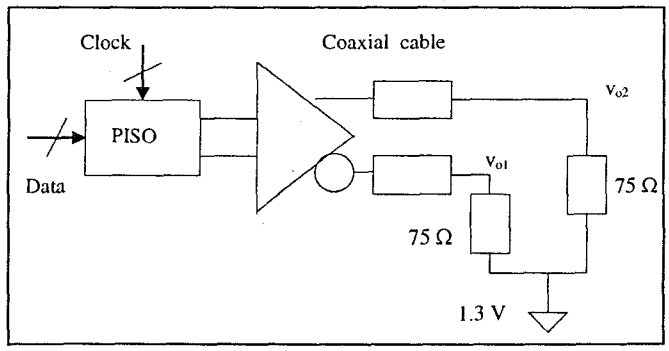


Fig. 1. Block diagram of Line Driver

75Ω impedance as well as the package parasitics.

### *B. Output Stage*

To exploit the high speed potential of non-saturating logic, Source Coupled Logic was used at the output stage of the driver. An NMOS differential amplifier was used with a tail current source to provide the requisite biasing. This is depicted in Fig. 2.

Passive pull up load devices were used to improve the speed and lower the effects of parasitics. The pull up load devices were nominally set at 30 Ω.

To determine the output current required, the driver was designed to drive a parasitic capacitance of 10 pF in parallel with the characteristic load impedance of the coaxial cable. This parasitic capacitance required an output current of 38 mA to achieve the specified rise/fall times. The quiescent tail current in the differential pair and the minimum size of the output transistors for driving this load were determined from simulation to achieve the specified signal swing and rise and fall times over temperature.

### *C. Cascaded Complementary Inverters*

The NRZ pulses supplied from the parallel-to-serial converter are only capable of driving a minimum sized inverter. To drive the load capacitance offered by the output transistors, a chain of cascaded inverters was used. This chain consisted of buffers with proportionally increasing sizes, resulting in an increase in drive capacity. The optimum ratio of device sizing from one stage to the next is well known to be e. This ratio will minimize the overall delay in the buffer but will not guarantee optimal rise and fall times at the output. To achieve the required rise and fall times, the last buffer before the source coupled pair was intentionally oversized.

TABLE I
TRANSISTOR SIZES

| Block | NMOS device size | PMOS device size |
|---|---|---|
| Inverter 1 | 1.5 u /0.6 u | 3 u / 0.6 u |
| Inverter 2 | 6.6 u / 0.6 u | 13.2 u / 0.6 u |
| Inverter 3 | 19.5 u / 0.6 u | 39.3 u /0.6 u |
| Inverter 4 | 56.4 u/ 0.6 u | 95.1 u / 0.6u |
| Inverter 5 | 149.7 u/ 0.6 u | 281 u / 0.6 u |
| Output stage | 300 u / 0.6 u | - |

With the 300u/0.6u dimensions of the output transistors, the number of buffers required to drive the source coupled pair is 5. The schematic of the Line Driver used is shown in Fig. 2, and the sizes of the transistors used are listed in Table 1 .

### *D. Timing considerations*

The propagation of the data stream through the chain of inverters produced a propagation delay which was nominally 1.4 ns. This can vary by as much as ±30 % due to process variations alone at 25° C.

For accurate transmission and reception, the data stream has to be synchronized with the output clock to achieve a delay of no more than 150 ps after the clock edge, according to the Fibre Channel Standards.

Synchronization was achieved by clocking and serializing the data stream at the end of the chain of inverters. This ensured that the delay in the output data would be caused only by the delay due to the source coupled pair at the output and the output parasitics.

## III. SIMULATION

The Line Driver was simulated by subjecting it to TTL

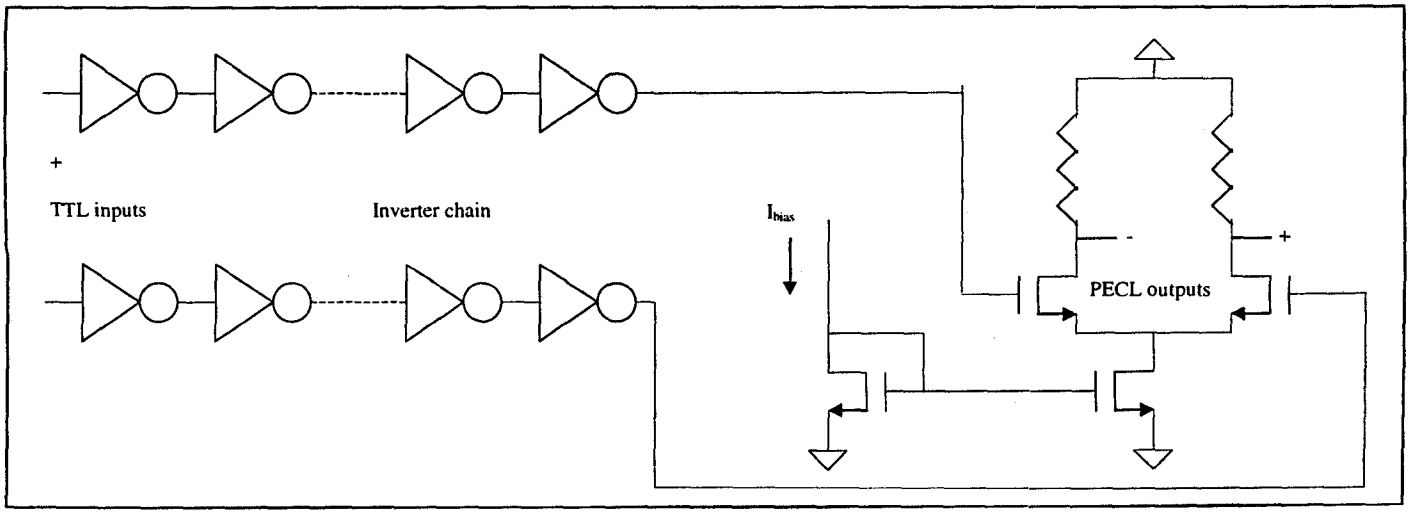


Fig. 2. Schematic of Line Driver

input pulses supplied through a minimum sized buffer. An IC package model for a commercial (Kyocera) IC package, suitable for high frequency communications was used to simulate the effects of packaging. This package takes into account not only bonding wire parasitics, but also those of the package itself from the point where the bonding wires are connected to the pad on the chip to the point where the package contacts a Printed Circuit Board.

The circuit was also simulated at high temperatures, to ascertain that the requisite swing was achieved. The results are shown in Table 2 .

## IV. Layout

Layout for the 1 GHz Line driver deserves some attention. The large drain areas and perimeters of the output transistors contribute to the parasitic load capacitance. To reduce drain areas, the fingered Poly layout illustrated in Fig. 3 was used. Using this technique, the drain areas were reduced by almost 30 % below what was achievable with a standard layout.

Another problem that needed consideration was the RC delays caused by long gate Poly lines. The delays induced in the output transistors were found to be significant and would contribute further to the delay and degradation of the output pulse. Hence, the Poly lines were strapped with metal lines to reduce their resistance and hence reduce the delay.

Finally, electromigration due to the large currents and ESD issues had to be taken into consideration. Metal line widths must be sized wide enough, and the spacing between contacts on the output pads increased to provide ESD protection at the outputs.

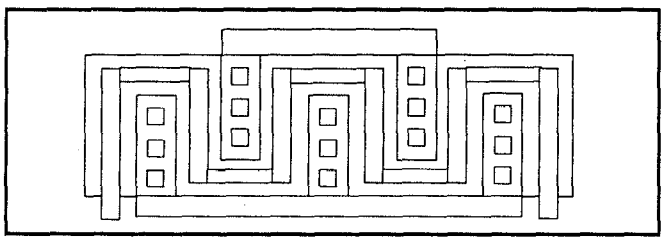

Fig. 3. Fingered poly layout

TABLE 2
Simulation results

| | 25 C | 100 C |
|---|---|---|
| Single-ended signal swing (p-p) | 1.4 V | 1.16 V |
| Rise / fall time | 83 ps | 100 ps |
| Overshoot | 0.21 V | 0.15 V |
| Power dissipation | | |
| Static | 0.258 W | 0.224 W |
| Dynamic | 0.256 W | 0.226 W |

## V. Conclusion

This paper presents the design strategy, layout approach and simulation performance of a 1.0625 Gbps Line Driver. It has been submitted for fabrication and experimental results will be reported when they are available.

The success of the all-CMOS design will lead to incorporation of the Line Driver circuit into a larger transceiver chip that can provide functionality beyond just transmitting and receiving channel data.

## References


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