A Modified Costas Loop for Clock Recovery and Frequency Synthesis.

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Abstract

A clock recovery circuit that takes advantage of self biasing, and the presence of delayed and advanced versions of the VCO output to increase the phase detector gain has been designed and simulated using a 0.6μm CMOS N-well process. This clock recovery circuit shows a fast response time. In addition to clock recovery, this circuit can be used as a frequency multiplier or synthesizer, without additional circuitry. To reduce jitter, the feed back loop is closed only when there is a control signal to adjust the VCO frequency.

1. Introduction

Phase Locked Loops (PLLs,) and Delay Locked Loops (DLLs,) find wide applications in areas such as frequency and phase modulation systems, data transmitters, data receivers, electronic drives for data storage devices, and microprocessor systems [1], [2]. PLLs, and DLLs are used to solve several problems in the areas of communication, data transmission, and data storage. These problems include jitter reduction, clock skew suppression, frequency synthesis, and clock recovery. Good PLL and DLL structures that have low input tracking jitter and a broad frequency range have been reported [3],[4]. These structures take advantage of self biasing techniques and the use of differential architectures. The reported structures employ a high loop bandwidth to suppress the jitter that results from the supply and substrate noise [3] but this high loop bandwidth causes stability problems [3], [4]. To minimize the effect of input excess phase and frequency noise requires the minimization of the loop filter bandwidth. Correspondingly, minimizing the loop filter bandwidth slows down the acquisition time, and limits the capture range [2]. Since both the acquisition time, and the lock range are also affected by the gain of the phase detector and by the sensitivity of the oscillator, we can reduce the demand on large loop filter bandwidth by increasing one or both of these corresponding gains. It is reported that the DLL can have better jitter immunity because it doesn't have a closed loop VCO.

2. Modified Costas Loop Approach

In this work we introduce a clock recovery circuit based upon the idea of a Costas loop circuit which is used for AM DSB-SC (Amplitude Modulation Double Side Band Suppressed Carrier) detection, and for carrier recovery [5], [6]. The modified circuit is shown in Fig.1. In this circuit, upper and lower signal paths are generated. Error signals e1 and e2 are subtracted to provide the control input to the VCO. Phase lead and phase lag versions of the VCO output are generated by the +δ and -δ phase shifters. These outputs are then mixed with the input, and passed through the upper and lower lowpass filters (LPF). Ideally, the upper and lower lowpass filters are identical.

The implementation of this structure can be simplified if we are using a ring oscillator to implement the VCO since different phases of the local oscillator output which provide the +δ and -δ phase shifts are inherently available.

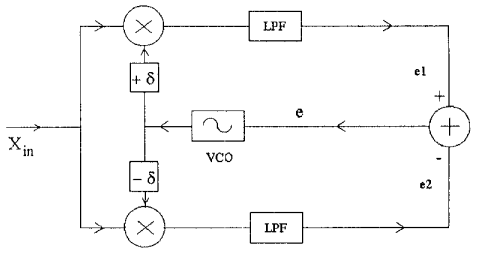

Fig.1. The Modified Costas loop basic architecture

If we have an input signal $X_{in} = V_{in}\cos(\omega_{in}t + \theta_{in})$, and a sinusoidal oscillator output $V_{lo}\cos(\omega_{lo}t + \theta_{lo})$, then it can be shown from a straight forward manipulation of trigonometric identities that the error signal will be

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$$e = e_1 - e_2 \qquad (1.a)$$

$$e = \frac{K_{lp} V_{in} V_{lo}}{2}\begin{bmatrix}\cos(\Delta\omega t + \Delta\theta - \delta) \\ -\cos(\Delta\omega t + \Delta\theta + \delta)\end{bmatrix} \qquad (1.b)$$

$$e = K_{lp} V_{in} V_{lo} \sin(\Delta\omega t + \Delta\theta)\sin(\delta) \qquad (1.c)$$

where K_{lp} is the low pass dc filter gain $\Delta\omega t = (\omega_{in} - \omega_{lo})t$, *and* $\Delta\theta = \theta_{in} - \theta_{lo}$. The error signal, e, will be zero when both the frequency, and phase differences are zeros. The equivalent phase-frequency detector is monotonic in the range [-π/2, π/2]. The phase-frequency detector is sensitive to both frequency and phase variations. To increase the sensitivity of the phase-frequency detector we choose δ to be less than and as close as possible to π/2, this can be achieved by choosing δ=(N-1)π/2N.

3. Circuit Design and Realization

An implementation of the clock recovery circuit using a fully differential VCO. is shown in Fig.2 The multipliers are implemented with 2-input AND gates. The lowpass filters and the summer are realized with a charge pump driving a charge storage capacitor. The input data, which is in a Non Return to Zero (NRZ) format, is multiplied by the VCO output to pinch the input transitions to the loop between the leading and the lagging outputs from the oscillator and this multiplier is implemented with an AND gate as well. The block labeled RB. represents a replica bias generator circuit. The typical error signals are shown in Fig.3.a, and Fig.3.b. In these figures we assume that the loop is initially locked and then a small variation in the input data frequency occurs at time tref. It is clear from the figures that if the input data frequency becomes higher than the oscillator frequency (Fig.3.a) then the pulse width of signal e1 increases, while the e2 signal pulse width becomes narrower, and if the input data frequency becomes less than the oscillator than T_{lo} where T_{in} is the input data period. T_{lo} is the local VCO period. It is interesting to note that the two error pulses are not simultaneous and even when the loop is locked on the clock of the input data the two error signals will exist but the effects will cancel each other by the end of each first half pulse period of the VCO. The timing of the error signals, and the error voltage at the output of the charge pump are given by

$$e_1 = u(t - T_{in}) - u\left(t - \frac{3T_{lo}}{2} + \Delta\right) \qquad 2.a$$

$$e_2 = u(t - T_{in} - \Delta) - u\left(t - \frac{3T_{in}}{2}\right) \qquad 2.b$$

$$e = \frac{I_{ch}}{sC_p}\left\{\frac{5}{2}(T_{lo} - T_{in})\right\} \qquad 2.c$$

where Δ is the time interval by which V_leading leads the VCO output, and by which V_lagging lags the VCO output and e is the error voltage at the output of the charge pump. C_P is the charge storage capacitor at the output of the charge pump circuit. The loop will be inherently open during the part of each period when the error signal e is zero. On the average the loop will be open for half of the period of high level input data, and will also be open over the period of time when the input has a low level. In this situation , on the average, the loop will be open for 75% of the time of operation. By neglecting the effect of the delay between the error pulses, the term e represents the change of the control voltage across the capacitor of the loop filter. The equations above show that the detector used is sensitive to both frequency and phase variations. The net integral error will be zero when $T_{lo} - T_{in} = 0$ and the two signals are in phase. This architecture is expected to be faster than the traditional PLL circuits because it has an

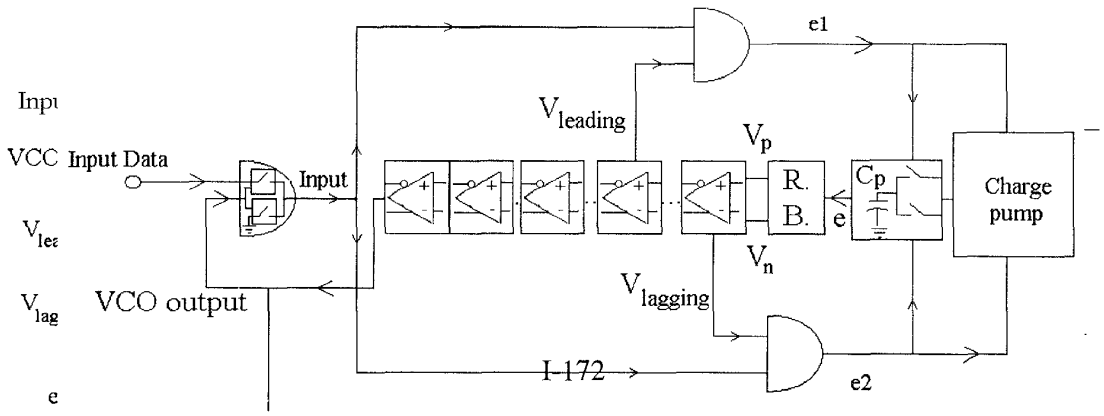


Fig. 3.a Error signals for freq. increase

Fig. 3.b Error signals for freq. Decrease

multiple of the frequency of the clock of the input data stream. If the input data is a stream of successive low level bits the error pulses will have zero level, and the loop will be open and when the input is a stream of successive high level bits the circuit will actually feed the output of the VCO to the phase detector resulting in the period of e1 being equal to that of e2 so the VCO control voltage will maintain a constant average. In both cases no change will occur on the output frequency or phase. The modified Costas Loop has been implemented using differential delay cells to form the VCO.

The delay cells are the same as those reported in [3],[4], and [7]. Those cells have symmetric load PMOS transistors. The delay cell is shown in Fig.4. The transfer function of the delay cell is

$$A(s)=\frac{V_{OS}}{V_{ID}}=\frac{-g_{m1}/C_L}{2(s+g_{m2}/C_L)} \qquad (3.a)$$

where V_{OS} is the single ended output voltage, and V_{ID} is the differential input voltage. If we assume the loss (g_{m2}) is sufficiently large to maintain a nearly sinusoidal oscillation frequency, it can be shown that the frequency of oscillation is given by the expression

$$f_{lo}=\frac{1}{2\pi}\frac{g_{m1}}{C_L}\cos(\pi/N) \qquad (3.b)$$

where N is the number of stages in the ring oscillator. Since g_{m1} is proportional to the square root of the tail current in the differential pair, it follows that f_{lo} is linearly proportional to V_n. So we can increase the frequency of oscillation by increasing Vn which will increase the radius of the circle on which the VCO poles lie, and will shift this pole locus circle horizontally to the left, correspondingly reducing Vp will shift the pole locus circle back around the origin which will give a better spectral purity of the VCO output. A replica biasing circuit is used to provide the control voltages Vn, and Vp, this is the same replica biasing presented in [3],[4], and [7]. Single ended outputs are needed to derive the multipliers (AND gates). A single-ended output is obtained by using a regular differential pair followed by two inverters.

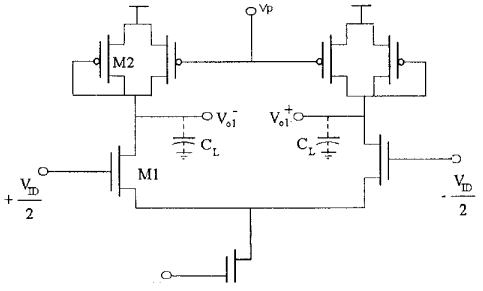


Fig. 4 The Differential delay cell

A charge pump implementation along with the charge storage capacitor is shown in Fig.5. The transistor M1 will be off, and M2 will be on when the error pulse e1 has a high level, and transistor M5 will charge the capacitor Cp at the Out node. Also transistor M4 will be off, and M3 will be on when the error pulse e2 has a high level, and transistor M6 will discharge the capacitor. The loop will be open when both error pulses e1, and e2 have a low level. The charge pump phase comparator blocks exhibit several desirable features. They haven't exhibited false lock, the input signal and oscillator output waveforms are precisely in phase when the system is in lock, and the PLL attains lock quickly[1],[2]. For a small signal analysis of the system we will assume that the phase difference between the input, and the oscillator output is small during a given period [1]. A precise analysis of the system is difficult because it is a time variant, nonlinear system so the analysis will be done based on the average charge flowing into the LPF.

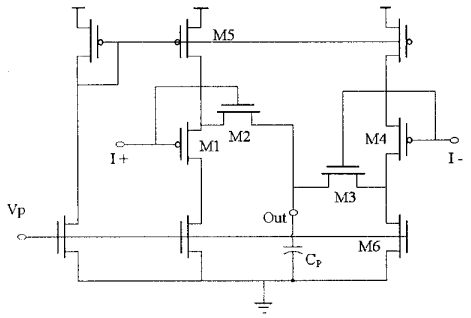


Fig.5 The charge-pump circuit.

The change in the control voltage is shown in equation (2.c). The average charge pump current is given by

$$I_{avg} = \frac{I_{ch}}{T_{lo}} \cdot \left\{ \frac{5}{2} \left(T_{lo} - T_{in} \right) \right\} \qquad (4.0)$$

and the equivalent phase detector gain, K_{pd}, is

$$K_{pd} = \frac{I_{ch}}{2\pi} \cdot [2.5] \qquad (5.0)$$

Eq. 5.0 shows that the equivalent phase detector gain is about twice that of the traditional phase detector gain that uses the charge pump circuit as a phase detector, which is $I_{ch}/2\pi$ [1]. The VCO constant, K_{osc} was obtained from the simulation where $K_{osc} = \frac{\Delta\omega}{\Delta V_{cntrl}}$. Fig. 6 is used to estimate K_{osc} for the frequency range 800MHz up to 1.1GHz, and was found to be equal to 9.974×10^9 rad/volt.

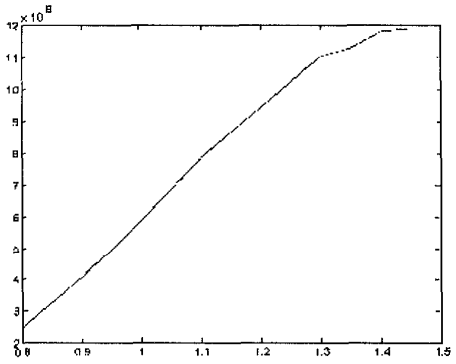
4. Simulation Results

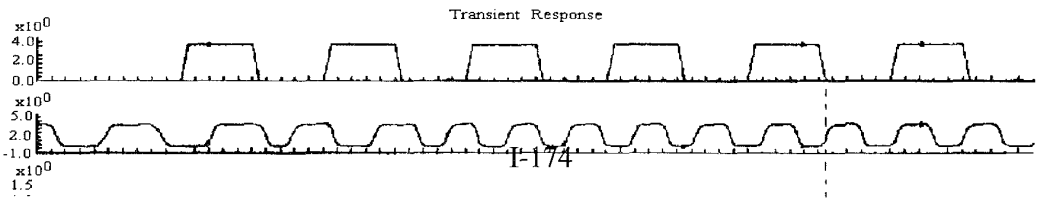
A transistor level simulation was made of the implementation of Fig.2. In this simulation, the building blocks discussed in the last section were designed in a 0.6μ CMOS process. A 5 stage voltage controlled oscillator was used to obtain a high operating frequency. This clock recovery was simulated for operation at 250MHz, 500MHz, and 1GHz data rates. The results for one simulation which are typical of the locking characteristics of the structure are shown in Fig.7. for an input data sequence. The input is NRZ data and the recovered clock must have a period that is equal to 1 bit-time of the input data. This simulation was for a 1GHz data rate. Fig7.a shows the starting of simulation when the loop acquires lock to the data clock, The oscillator was running initially at 750MHz. Fig.7.b shows the loop maintaining lock. Fig. 7.a shows that the acquisition time is in order of $10\,T_{lo}$. The acquisition time is less in the cases of lower input frequencies. From the simulation results the lock range is greater than 20% of f_{lo} at 1GHz resonant frequency, lock range and capture range are shown in table 1. In Fig.7.a it is apparent that the frequency lock is achieved very quickly but phase-lock denoted by t-lock is slower.

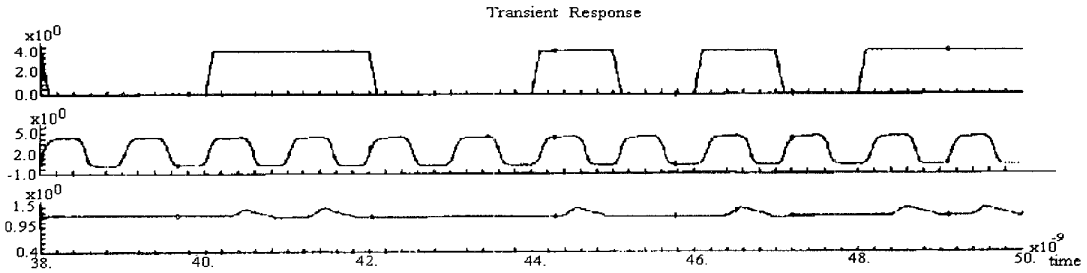
The simulation of the circuit working as a 1GHz frequency synthesizer is shown in Fig.8. In this case the input frequency is 250MHz. The problem with high order frequency multiplication is that the number of transitions at the input is low relative to the VCO frequency, which means that the circuit will see the input clock as long sequences of zeroes and ones.

Fig. 6 The VCO freq. Vs. Control voltage.

(a) Start of lock.







(b) Maintaining lock.

Fig. 7 Simulation of lock acquisition and maintenance

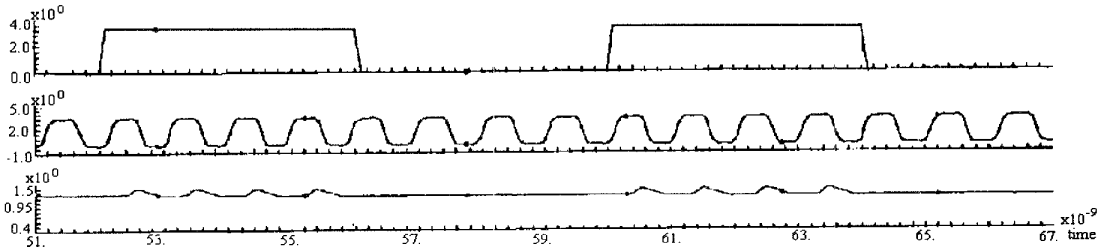


Fig. 8 Freq. synthesis operation

Table 1.

Frequency of operation	1 GHz
Lock range	830MHZ-1.17GHz
Capture range	925MHz-1.075GHz

5. Conclusion

This paper introduce a fast clock recovery circuit using a self biased differential VCO and a high gain phase detector. Low acquisition time and wide capture range can be achieved with this simple structure, which is also expected to have high noise immunity due to the loop braking over about 75% of the period of operation.

6. References

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