Matching Performance of Current Mirrors with Arbitrary Parameter Gradients Through the Active Devices

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Effects of threshold gradients at any angle across a die and through active devices on the matching characteristics of current mirrors are discussed. Results show a major improvement but also an unreported limitation in performance of common-centroid layouts. A CAD tool that predicts performance of arbitrary layouts under arbitrary parameter gradients is introduced.

1. Introduction

The performance characteristics of many linear and mixed-signal integrated circuits is dominated by the matching characteristics of current mirrors and differential amplifiers. The matching characteristics of these two key circuit elements are attributable to both systematic and random variations in both geometric parameters and process parameters. The random variations are easy to model and tradeoffs can be made between area and performance to compensate for random variations in these parameters. It is often more difficult to compensate for the systematic parameter variations and some of these systematic parameter variations are often mistakenly assumed to be random - an assumption that can cause significant errors in a statistical analysis because of the inherent correlation of these parameters. Some recent work by Felt et. el. [1] shows that the magnitude of the matching errors associated with the systematic parameter variations are comparable to that due to the random parameter variations. We believe that the impact of not correctly handling the systematic parameter variations are even more significant than suggested by Felt in the design of high-end linear circuits.

2. Parameter Gradient Modeling

In this paper, the effects of threshold voltage gradients on the matching performance of current mirrors are investigated. In particular, the effects of threshold voltage gradients at any angle across a wafer for interdigitized layouts and for common centroid geometries are compared with the matching characteristics of a simple mirror layout. The parameter gradients are modeled in a distributed way through the active devices themselves. The results show that the matching characteristics are strongly a function of the angle of the threshold gradient across a die and that, for any angle, the effects of the threshold gradient for the common centroid layout is small. The results also show, in contrast to the well-accepted premise that the effects of linear gradients can be readily modeled [2] and are inherently canceled in common centroid structure [1], that the threshold gradients through the devices themselves create an angle-dependent gradient even in common centroid structures that assumes a maximum at a 45° angle through a simple common centroid layout.

The tool developed for simulating these effects can be readily used to predict the matching characteristics of an arbitrary layout of any size for arbitrary gradients in either threshold voltage or mobility and can be extended to predict the performance characteristics of differential amplifiers in the presence of the same gradients.

The seemingly simple problem of predicting the effects of threshold voltage gradients and mobility gradients on a MOS transistor is complicated by the unavailability of a suitable simulator and by some inconsistencies on modeling these effects that have appeared in the literature. Although process simulators are an appropriate tool for simulating the effects of parameter gradients, existing process simulators are limited to two dimensional modeling and only one of these dimensions is lateral. Correspondingly, the literature that relates to modeling transistors with nonuniform threshold voltages throughout the channel region depends upon the unjustifiable assumption that the equivalent threshold voltage of a transistor can be obtained by an area integral of the position dependent threshold voltage over the channel region [3]. Although this latter approach may provide a good approximation in some applications, it is inadequate for accurately predicting matching performance of current mirrors and differential amplifiers and leads to the incorrect conclusion that linear systematic gradients in process parameters are canceled in common centroid layout schemes.

3. Simulation Result

We have developed a simulation tool which approximates the distributed channel region by a series of finite lumped-element four-transistor cells as depicted in Fig. 1 in which each cell has four edge-centered nodes that can be connected to corresponding edge-centered nodes in adjacent cells. All gates of transistors in Fig. 1 are connected together - this connection is not shown in the figure to enhance clarity. With this finite lumped-element approach, a parameter gradient of any

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magnitude and at any angle relative to the cell can be readily simulated using a conventional SPICE-type simulator.

Four different layouts of a current mirror are shown in Fig. 2. The magnitude of the threshold gradient was assumed the same across each of the layouts and the angle of the gradient was varied continuously from 0° to 90° (from south to east) across the mirrors.

The matching characteristic of these current mirrors due to threshold voltage gradients are shown in Fig. 3 for a threshold gradient of 0.322mV/u. From this simulation, it is apparent that the matching characteristics are strongly a function of the angle of the threshold gradient. Since the direction of the gradient in threshold voltage across a wafer may vary from one wafer lot to the next, this figure shows that measured results from test structures may not be good indicators of production performance. In addition to predicting the effects of an arbitrary gradient, this figure shows that a major improvement in mirror matching is achievable with the common centroid layout which is expanded in Fig. 4. From Fig. 4, it is apparent that the two common centroid structures have a worst case matching error of 0.0015% and 0.002% for a threshold gradient of 0.322mV/u and this occurs at an angle of 45° relative to the axis of symmetry of the common centroid layout.

The tool developed for this simulation has a graphical MATLAB interface that is used to automatically generate a SPICE file which can be used to simulate the performance of a circuit. The tool is specifically focused towards predicting the performance of current mirrors and differential amplifiers in the presence of arbitrary threshold voltage and mobility gradients that occur at any angle across a die. Although the tool was established for predicting circuit performance under linear gradients, arbitrary gradients in process parameters can also be simulated. The graphical interface with MATLAB allows the user to describe arbitrary layouts of current mirrors and differential amplifiers comprised of arbitrarily shaped transistors.

4. Test Chip and Measurement Method

A test chip designed to verify the validity of the gradient matching simulator is shown in Fig. 5. The test circuit on this chip was a single simple current mirror using Layout1 of Fig.2. The width and length of each transistor were identical(32um) and the spacing between the two transistors was 4um. This chip has been fabricated in 2um n-well process. In the test structure, the V_T gradient was controlled via the back bias on the transistors. The p-channel transistors were placed in a large circular n-well. Multiple contacts were placed around the entire periphery of this n-well region. Currents were then introduced at a large number of predetermined angles by selecting the appropriate diagonally opposing well contacts. These currents introduced a gradient in the well voltage which correspondingly induced a gradient in the threshold voltage of the test transistors. For dimensions of the transistors that are reasonably small relative to the diameter of the n-well, the resultant V_T gradient is quite linear. The magnitude of the well current is directly related to the magnitude of the induced threshold gradient. It can be shown that a 1.189mv/u gradient in the substrate at the location of the test device will create a threshold voltage gradient of approximately 0.322mv/u.

To avoid forward biasing the well-diffusion junction, the substrate voltage around the test current mirror was kept at about 6V, while the drain and source diffusions were restricted to be at most 5V.

5. Experimental Result

The test results of the simple structure are shown in Fig. 6. Compared to the simulation result, both curves are very similar. The peak-to-peak variation of the measured result is about 1.5% and the peak-to-peak variation of the simulation was also about 1.5%. The main difference between these two curves is a downward shift of 0.5% for the test structure compared to that of the simulation. The reason for this shift is believed due to the random mismatches in the test structure and the native gradient due to processing. Test results for the interdigitized structure are shown in Fig. 7. The results show that the simulator has successfully estimated the effect of the gradient threshold voltage in the performance of the current mirror. We believe the simulator effectively models the gradient effects in other structures as well.

6. Conclusion

A simulator suitable for predicting the performance of current mirrors in the presence of arbitrary parameter gradients has been introduced. A comparison of the performance of several layout structures shows substantial differences in the sensitivity of the mirror gain due to parameter gradients. Comparison of experimental and simulation results showed good correlation.

7. Acknowledgments

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8. References

[1] Felt, E. et. el. "Measurement and Modeling of MOS Transistor Current Mismatch in Analog IC's", *Proc. ACM, 1994*, pp. 272-277.

[2] Strojwas, A. J. et. el. "Manufacturability of Low Power CMOS Technology Solutions", *Proc. IEEE Int. Symp. on Low Power Electronic Design*, pp. 225-232, Monterey, August 1996.

[3] Pelgrom, M.J. et. el. "Matching Properties of MOS transistors", *IEEE J. of Solid State Circuits*, Vol. 24, No. 5, pp. 1433-1439, Oct. 1989.

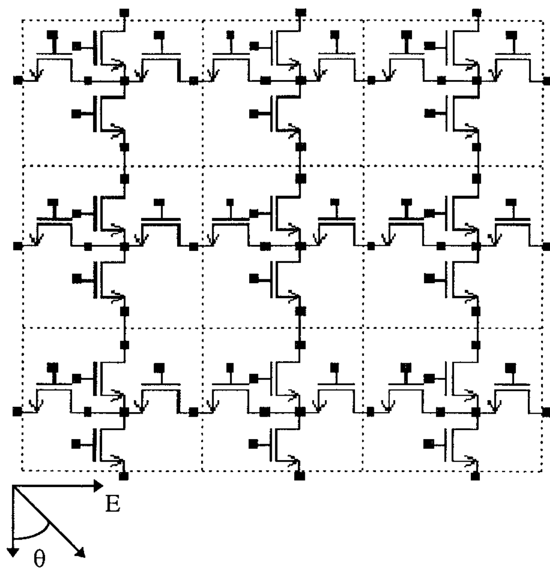


Fig. 1 Finite lumped-element model of 4-transistor cells

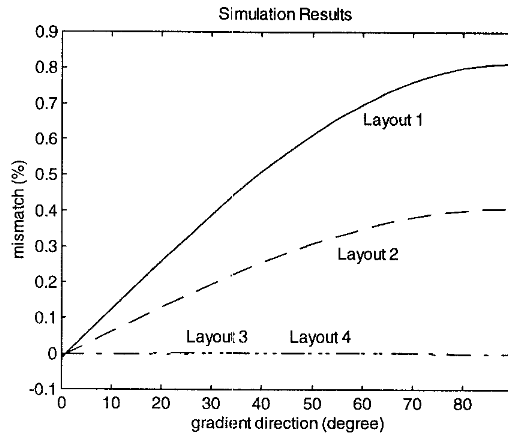
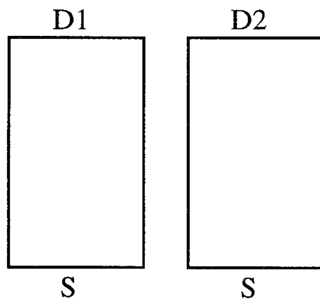
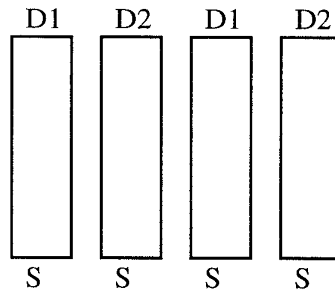


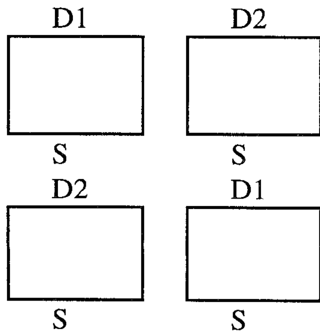
Fig. 3 Matching characteristics of the 4 mirror layouts



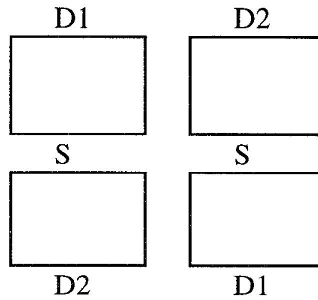
Layout 1 Simple mirror



Layout 2 Interdigitized mirror



Layout 3 Common centroid mirror without common source



Layout 4 Common centroid mirror with common source

Fig. 2 Current mirror layouts

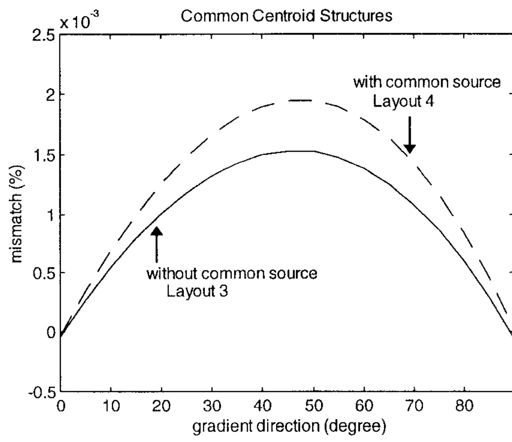


Fig. 4 Matching characteristics of common centroid layout

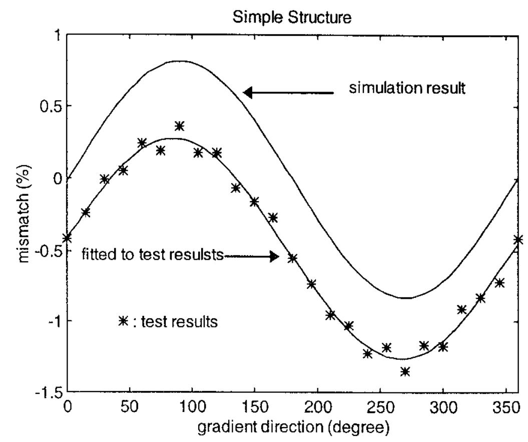


Fig. 6 Comparison between the experimental and simulation results of simple structure

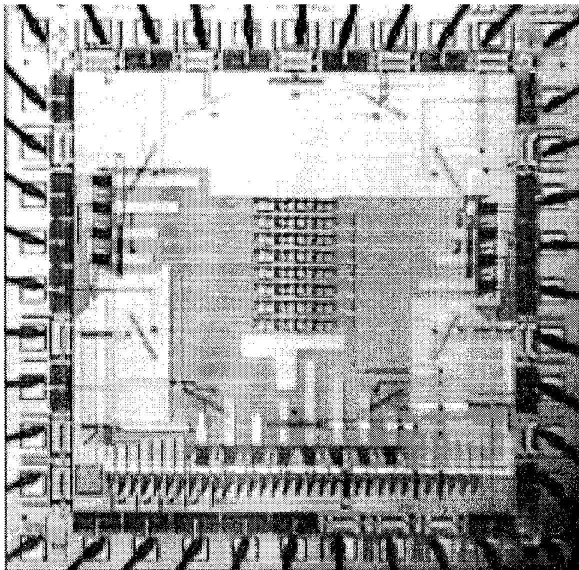


Fig. 5 Test chip of the simple mirror structure

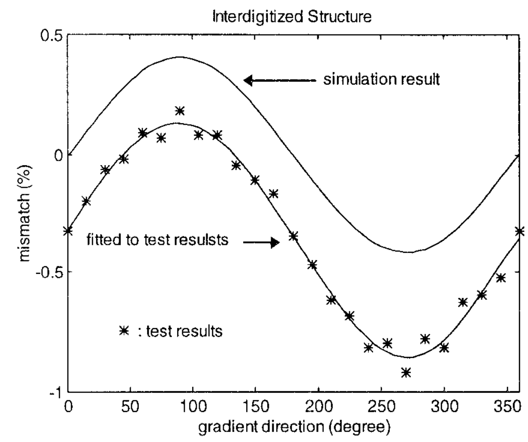


Fig. 7 Comparison between the experimental and simulation results of interdigitized structure