Deterministic Phase Jitter in Multi-Phase CMOS Ring Oscillators Due to Transistor Mismatches

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Abstract

A comparison is made of the effects of random parameter variations on the periodic mismatches in three different high-speed ring oscillators generating multi-phase clock signals. These variations in the phase-to-phase periods manifest themselves in the form of jitter which is deterministic in nature. Simulations have also been carried out to demonstrate the improvement in the jitter performance of these oscillators with device scaling.

1. Introduction

Phase Locked Loop (PLL) plays an important role in modern communication systems. It has been widely used in frequency synthesizers and data and clock recovery circuits. A PLL usually consists of a phase detector, a filter, a voltage controlled oscillator (VCO) and a divider. In many applications, multi-phase clock signals are required to be generated from the PLL. As an illustration, in some fiber-channel transmitters, parallel input digital data are transmitted serially via the fiber optic links. A PLL with multi-phase clock signals is utilized to multiplex the parallel input data to the transmitter output so that the data is transmitted serially. The multi-phase clock signals are obtained from the VCO when the VCO is realized as a ring oscillator. However, variation on each output clock phase (jitter) is a critical performance parameter. With careful PLL design, the jitter in the VCO is usually the dominant contributor on the overall PLL jitter performance, especially when the PLL is used as a frequency synthesizer [1]. Therefore, it is important to design a low jitter VCO and study the jitter performance

for different VCO architectures. To characterize the VCO jitter, it can be divided into two categories, namely random jitter and deterministic jitter. The random jitter is usually caused by power supply noise and device noise. The deterministic jitter is mainly due to the mismatches on the delay of each stage in the ring oscillator. In this paper, the effects of random parameter variations on the deterministic jitter performance of different multi-phase clock generating CMOS ring oscillators are studied and compared.

2. CMOS Ring Oscillators

A ring oscillator usually consists of a number of delay inverter stages connected in the ring topology. In the literature, many different types of inverter stages have been proposed. In this paper, we focus on the three inverter stages shown in Figure 1. The first inverter stage is a simple CMOS inverter. The second delay stage is an ECL type inverter circuit with an NMOS differential pair and a pair of PMOS active loads biased in the ohmic region [2]. The last inverter stage is based on symmetric PMOS load differential inverter proposed in [3].

An approximated analysis of the simple inverter stage is performed. $V_{in} = V_{out}$ is assumed to be the quiescent point. The transconductance is computed at this point. The input transistors provide the capacitive load. The gate-drain capacitance has been neglected. The frequency of the VCO is evaluated as g_m/C. This provides the following expression in terms of the physical sizes and the threshold voltages of the transistors.
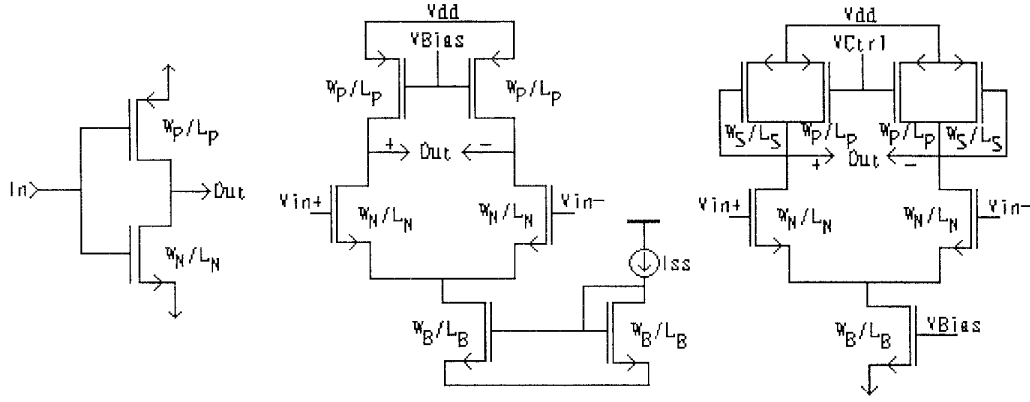
a) Simple Inverter Stage b) Differential ECL Type Delay Cell c) Symmetric Load Differential Pair

Figure 1 : Three Different VCO Stage Architectures

For the simple inverter structure,

$$f \propto \frac{1}{2\pi} * \sqrt{\frac{\mu_N \mu_P W_N W_P}{L_N L_P} \frac{\left(V_{DD} - |V_{T_P}| - V_{T_N}\right)}{\left(W_N L_N + W_P L_P\right)}}$$

Variations in the lengths, widths and threshold voltages of the devices are introduced. Since each of these variables are uncorrelated, the variance in the frequency is given by

$$\frac{\Delta f}{f} = \sqrt{\begin{array}{c} K_1^2 \frac{\Delta W_N^2}{W_N^2} + K_1^2 \frac{\Delta W_P^2}{W_P^2} + K_{21}^2 \frac{\Delta L_N^2}{L_N^2} + \\ K_{22}^2 \frac{\Delta L_P^2}{L_P^2} + K_3^2 \frac{\Delta V_{T_N}^2}{V_{T_N}^2} + K_3^2 \frac{\Delta V_{T_P}^2}{V_{T_P}^2} \end{array}}$$

where

$$K_1 = \frac{1}{2}\left(\frac{W_P L_P - W_N L_N}{W_P L_P + W_N L_N}\right)$$

$$K_{21} = \frac{1}{2}\left(\frac{W_P L_P + 3 * W_N L_N}{W_P L_P + W_N L_N}\right)$$

$$K_{22} = \frac{1}{2}\left(\frac{3 * W_P L_P + W_N L_N}{W_P L_P + W_N L_N}\right)$$

$$K_3 = \left(\frac{1}{V_{DD} - |V_{T_P}| - V_{T_N}}\right)$$

A similar analysis can be carried out for the ECL type differential pair and the symmetric load differential pair.

As mentioned in section 1, multiple clock phases can be obtained from different inverter outputs. The phase difference between inverter outputs is determined by the delays of the inverter stages. For a three-stage ring oscillator, we can obtain exactly $0°$, $120°$ and $240°$ clock phases from different inverter outputs if the delays of the inverter stages are the same. However, due to transistor mismatches, the delays of the inverter stages will not be identical and hence, the phase-to-phase periods will deviate from the ideal. This deviation can be estimated in mathematical terms as the variation of the delay of each stage with the variation of the process parameters. It is important to emphasize that the fairly large process run-dependent variations have negligible effect on the performance of the VCOs. The random variations across a die, though smaller in magnitude, lead to significant contribution to jitter. To study the effects of transistor mismatches on the variations of clock phases, three stage VCOs based on inverter stages shown in Figure 1 were simulated as discussed in the following section.

3. Simulation and Comparisons

Simulations were carried out on the three different ring oscillator configurations. The designs were tuned to consume the same amount of RMS power (3.3V*950uA = 3.135mW) and operate at approximately the same frequency ($t_d \approx 900ps$) to facilitate comparison. The random variations occurring at the die level were introduced in the physical dimensions (W & L) of all the devices of each of the stages in the 3-stage VCO as described in [4] and shown in table 1 and Monte Carlo simulations were carried out. Each Monte Carlo run provided three uncorrelated samples. Twenty Monte Carlo simulations were performed to generate adequate samples for prediction of jitter. The jitter was measured as the standard deviation of the phase-to-phase period. Variations in the threshold voltage were also introduced and a marked increase in the jitter was observed in line with predicted values as shown in table 2. The jitter for the simple inverter stage was observed to be $\approx 1.5ps$ which compares well with the theoretically estimated value of 6.2ps The gate-drain capacitance was neglected in the computations which resulted in the overestimate.

The devices were scaled up and the bias adjusted to maintain the same oscillating frequency. The random variations were recomputed each time and introduced in the design. The variations reduce in the absolute and relative sense. Jitter improves as the square root of the device scaling in all the cases as shown in Figure 2.

Variation$\left(\sigma^2\right)$	W	L	V$_t$
	$\dfrac{A_W^2}{L}$	$\dfrac{A_L^2}{W}$	$\dfrac{A_{VTO}^2}{WL}$

Note : $A_W = A_L = 0.017_A{}^{3/2}$
& $A_{VTO} = 21.2_A mV(NMOS)/24.7_A mV(PMOS)$ are process parameters

Table 1 : Random process variations across a die

Delay Stage	W & L Variations	W, L & V$_t$ variations
Simple Inverter	8.796E-13	1.44E-12
ECL type differential pair	4.835E-12	8.042E-12
Symmetric Load Differential pair	5.322E-12	8.337E-12

Table 2 : Standard deviation of the delay

a. Simple Inverter Delay Stage   b. ECL Type Differential Pair   c. Symmetric Load Differential Pair
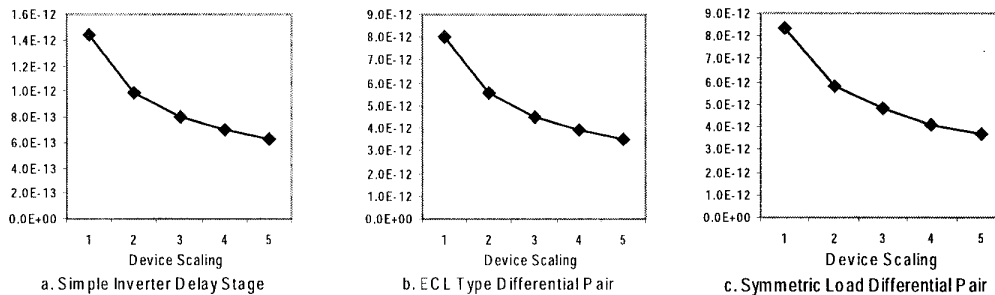
Figure 2 : Effect of device scaling on variations in the period

4. Conclusion

It is observed that the CMOS inverter-based structure offers the best performance because of the presence of fewer devices. The ECL type differential pair stage has greater jitter tolerance to device mismatches than the symmetric load differential pair structure

An important consideration in the design of multi phase generating VCOs is the matching between stages. Mismatches reflect themselves in the form of jitter when these clocks are used for serial transmission,

which is deterministic in nature. To make the stages tolerant to random process variations across a die would be a difficult task without compromising on frequency controllability. A technique to handle this in a PLL would be to design a phase detector, which would align the reference clock with each of the clock phases with appropriate phase shifts.

5. References

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