EFFECTS OF RANDOM JITTER ON HIGH-SPEED CMOS OSCILLATORS

Yiqin Chen, Satyaki Koneru, Edward Lee and Randy Geiger

Department of Electrical and Computer Engineering
Iowa State University
Ames, IA 50011

ABSTRACT

A comparison is made of the effects of device noise on the jitter of three different high-speed voltage-controlled ring oscillators. These comparisons show that oscillator architecture plays a significant role in jitter performance and that in high-speed oscillators, the device noise contributed when the MOS transistors are operating in the triode region is substantial. These comparisons also show minimal differences in the noise predicted by the simple and widely used noise model and that predicted by the more complete but more complicated model recently introduced by Sodini and Hellums.

1. INTRODUCTION

Jitter in voltage controlled oscillators and phase or delay locked loops is a major contributor to the Bit Error Rate (BER) in communication channels. Although the jitter effects may be negligible in low-speed channels, they play a major role for channel data rates in the 200MHz to 2GHz range and they will be even more problematic at higher frequencies. Jitter in these circuits is due to several factors including device noise, supply and ground noise, substrate coupling, device mismatch and data dependencies. The relative impact of each of these factors is strongly dependent upon circuit architecture, layout, and the power allocated to the building blocks that comprise the loops.

This paper focuses on the effects of device noise on jitter performance in high-speed voltage controlled ring oscillators that are operating in the 200MHz to 2GHz range. The effects of device noise on linear circuits are well understood and both analytical formulations and computer simulations can be readily obtained to predict the frequency domain performance of such circuits.

Frequency domain approaches, however, have not proven successful in characterizing the noise-induced jitter in the period of voltage-controlled oscillators. The limited literature that focuses on this problem [1,2] suggests that the mathematical formulation and the computer simulations of this jitter require a time domain transient analysis approach. The mathematical formulation of the jitter performance is complicated by several factors. First, the wave shape of the outputs of high-speed voltage controlled oscillators is not a mathematically tractable function. Second, the transistors in the oscillator typically go between the cutoff, triode and saturation regions during each period of oscillation and, even when in the triode or saturation regions, the current levels are time-variant. Third, since accurate closed-form expressions for the oscillation period are not readily attainable, the probability density function for the random part of the oscillation period is not available. The seemingly straightforward time-domain simulation approach is also limited by practical implications. Most commercial versions of the popular SPICE circuit simulators model noise only in the frequency domain and are also lacking a time-domain random number generator which would be useful for inserting time-domain noise sources. Bolcato and Poujois [3] have reported on inclusion of a transient noise simulation capability in the program ELDO and Hageman [4] has discussed using a piecewise linear current source to externally provide noise input. The concept of using a piecewise linear current source to input time-domain noise in high-speed ring oscillators is complicated by the observation that the spectral density of the noise sources are highly time dependent as each transistor in many ring oscillator structures transitions between the cutoff, triode and saturation regions during each period of oscillation. Additionally, the device drain current (in contrast to the current in the drain lead which also includes current flowing through parasitic capacitances connected to the drain lead) which can be used to characterize the time-dependent noise spectral density of a MOS transistor is not available as an output variable in some SPICE simulators.

In this paper, a comparison of the effects of device noise on the random jitter of three ring oscillators is made. A two-step approach is used for including the device noise in the simulations [5]. The oscillators are first simulated without noise to determine the time-dependent operating points. The results are passed to an external computer program which generates a time-domain noise current source which has a time-dependent spectral density that agrees with that of all transistors in the oscillator. These time-domain noise sources are then reinserted into the SPICE simulator and a second simulation is used to determine the jitter. If phase wander is excessive, a third step can be used to realign the spectral density of the individual transistors with the actual drain currents in the devices.

2. NOISE MODELS

In high frequency ring oscillators, it is believed that the 1/f noise plays a minor role since lower frequency noise components are effectively rejected by the bandpass characteristics of the oscillator. White noise in a band around the frequency of oscillation is, however, problematic as it can propagate from stage to stage in the oscillator structure itself. A commonly used model for the noise in a MOS transistor is depicted in Fig. 1.

A commonly used noise model, denoted here as Model 1, models the white noise by the current spectral density equations:

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$$S_I = \begin{cases} 0 & cutoff \\ \dfrac{4kT}{R_{FET}} & ohmic \\ \dfrac{8kTg_m}{3} & saturation \end{cases} \quad (1)$$

where

$$R_{FET} = \frac{L}{\mu C_{ox}(V_{GS}-V_T-\frac{V_{DS}}{2})W}$$

$$g_m = \frac{\mu C_{ox}(V_{GS}-V_T)W}{L}$$

This model is known to have some limitations, in part, because of the discontinuity in the spectral density as the device transitions between the triode and saturation regions.

Sodini et. el. recently discussed a more complicated model [6] based upon BSIM model parameters which offers improved modeling in the saturation region and in which the discontinuity between the triode region and saturation region has been consistently removed. This model, denoted here as Model 2, is characterized by the current spectral density equations:

noise density in triode region:

$$S_I = 4kT\mu_{eff}^2 C_{ox}^2 \frac{W^2}{L^2 I_D}\left[(V_{GS}-V_T)^2 V_{DS} - \alpha_x(V_{GS}-V_T)V_{DS}^2 + \frac{\alpha_x^2}{3}V_{DS}^3\right] - 4kT\frac{WC_{ox}\mu_{eff}}{L^2 E_c} \cdot \left[(V_{GS}-V_T)V_{DS} - \frac{\alpha_x}{2}V_{DS}^2\right] \quad (2)$$

noise density in saturation region:

$$S_I = 4kT\mu_{eff}^2 C_{ox}^2 \frac{W^2}{L_{eff}^2 I_D}\left[(V_{GS}-V_T)^2 V_{dsat} - \alpha_x(V_{GS}-V_T)V_{dsat}^2 + \frac{\alpha_x^2}{3}V_{dsat}^2\right] - 4kT\frac{WC_{ox}\mu_{eff}}{L_{eff}^2 E_c} \cdot \left[(V_{GS}-V_T)V_{dsat} - \frac{\alpha_x}{2}V_{dsat}^2\right] \quad (3)$$

where α_x represents the bulk effect on the threshold voltage.

In the results that follow, a comparison will be made with results obtained with simple noise model of (1) and those obtained with the more complicated model (2) and (3). These results show that in the applications discussed in this paper, both models give comparable results.

3. HIGH-FREQUENCY RING OSCILLATORS

Three high-frequency ring oscillators are shown in Fig. 2. All can be voltage or current controlled and all can be designed to operate at frequencies between 250MHz and 1.5GHz in a standard 0.5u CMOS process.

The gain cell of the first is based upon the basic CMOS inverter. The second was discussed by Weigandt et. el. [1], it is a differential ECL type inverter circuit with PMOS load biased in the triode region. The third uses the same VCO structure as the second but the delay cell is a symmetric PMOS load differential inverter where the PMOS devices are biased in the saturation region.

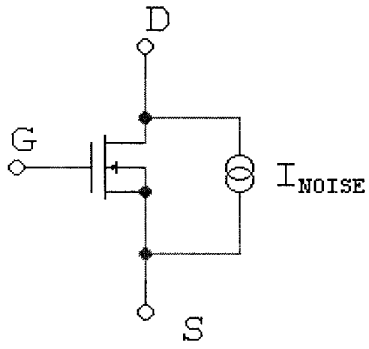


Figure. 1. Noise Model of MOS Transistor

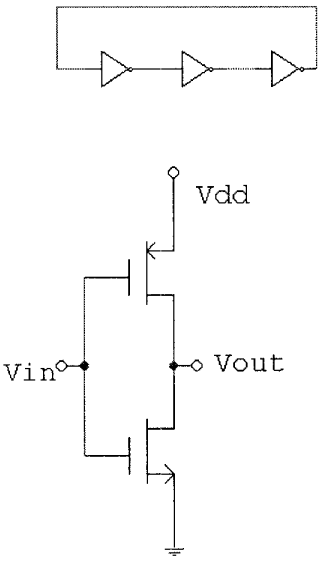
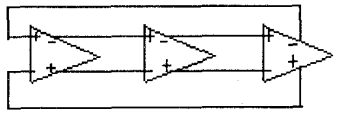


Figure. 2a VCO Structure 1 and Cell Structure



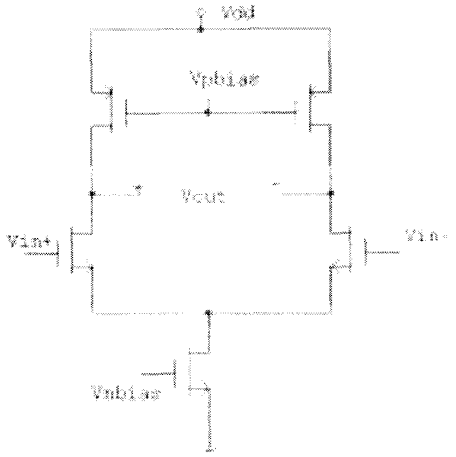


Figure.2b VCO Structure 2 and Cell Structure

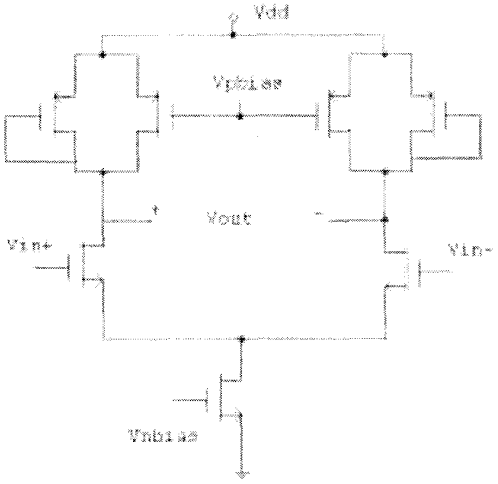


Figure.2c Cell Structure of VCO Structure 3

4. JITTER PERFORMANCE

The CMOS inverter oscillator of Fig. 2a will be used to compare the two different noise models and to assess which regions of operation of the transistors are the dominant contributors to the random jitter. In these comparisons, the ring was comprised of three inverters and the oscillator was designed in a 0.5u CMOS process to operate at a frequency of approximately 1.1GHz. Device sizes for the oscillator are shown in Table 1.

	NMOS	PMOS
W(unit: um)	2	5
L(unit: um)	0.8	0.8

Table 1: Device Size for PMOS and NMOS in Structure 1

Figure 3 shows the simulated time-domain output voltage of the oscillator, the node drain current and the time-dependent region of operation of the two transistors in one of the inverter stages. From this figure and from the noise spectral density equations (1), (2) and (3), it is apparent that the noise spectral density is strongly time dependent. The corresponding noise spectral density for the n-channel transistor as modeled by (1) (2) and (3), is shown in Fig. 4. The contributions of the spectral density from the saturation region and the triode regions is also shown in the figure for both noise models. Although there is a discontinuity in the simple spectral density model of (1) between the triode and saturation regions, the time-dependent noise spectral densities of the two noise models do not differ substantially in the ring oscillator structure.

A sample time-domain noise current which was generated from the noise spectral densities depicted in Fig. 4 is shown in Fig. 5. This was obtained using the same techniques discussed in [5]. A sampling period of 10psec. with a transition time between samples of 1psec was used to generate this noise current source. The periods of the output for the ring oscillator for a 50nsec simulation are shown in Fig. 6. The device noise manifests itself in a variation of the periods of the ring oscillator. These variations in the periods are referred to as jitter and it is characterized by the standard deviation of the periods after the oscillator reaches a steady state. For the oscillator of Fig. 2a, the random jitter contributed by all six transistors was simulated to be 85fsec using the BSIM noise model of (2). On multiple runs with different seeds for the noise current generator, there were only minor variations around this figure. To determine the relative effect of the noise in the ohmic region and the saturation region on the jitter, the simulation was made by suppressing the noise when any transistor was operating in the ohmic region. The resultant jitter due to the saturation region device noise was 52 fsec. Correspondingly, suppressing the noise when the devices are operating in the saturation region, we obtained the jitter due to the ohmic region operation to be 62 fsec (adding the results of the simulations for the two mutually groups of uncorrelated random noise sources predicts a jitter of 81fsec, slightly less than the 85fsec obtained previously.) Although the jitter noise contributed during the saturation region of operation is larger than that contributed during ohmic region operation, both regions play comparable roles in device performance. Finally, a comparison of the simple noise model of (1) was made with the more complicated noise model of (2). With the same seed, the simpler model predicts a jitter of 84 fsec suggesting that few benefits are derived from using the more complicated model.

The jitter performance of the three ring oscillator structures of Fig. 2 was compared with all oscillators operating at the same nominal frequency of approximately 500MHz and with the same power dissipation. The device sized for these structures is shown in Table 2.

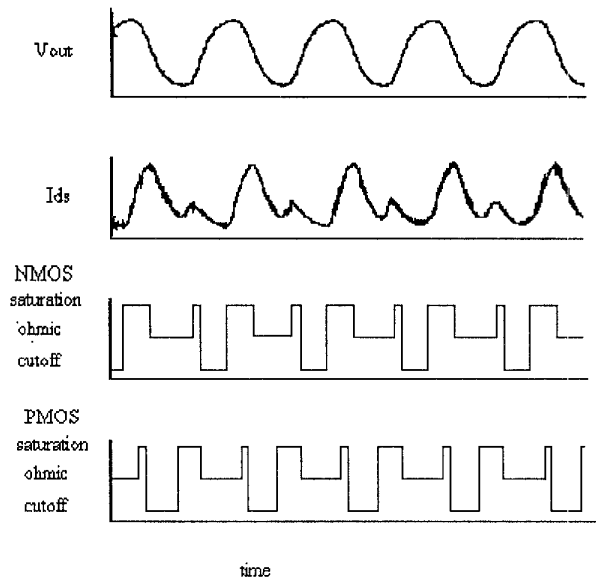


Figure.3 Region of Operation of NMOS and PMOS transistors

The simple noise model of (1) was used in these simulations. A comparison of the jitter of the three structures (including bias circuits)appears in Table 3. From this comparison, it can be seen that the architecture plays a significant role on the effects of random jitter due to device noise and that the simple CMOS structure of Fig. 2a which has less devices contributing noise offers better jitter performance.

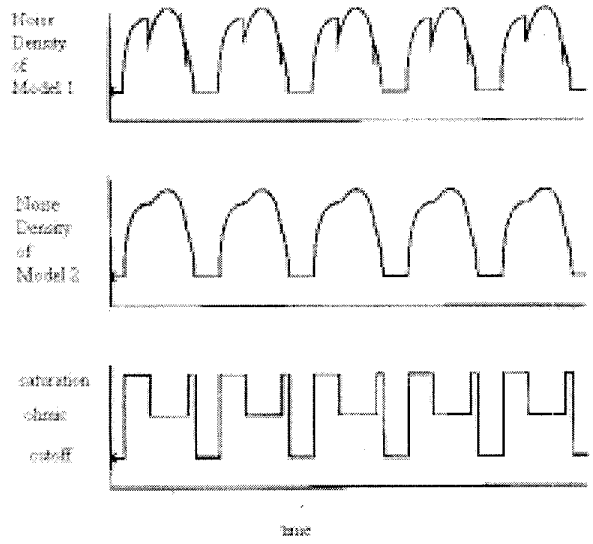


Figure.4 Noise Spectral Density for an NMOS transistor

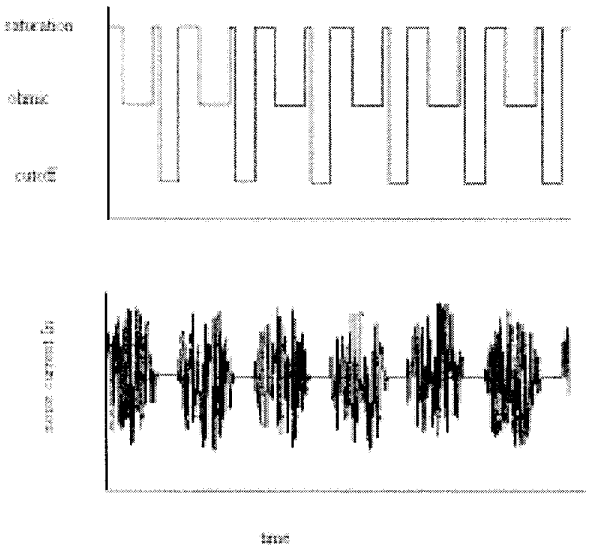


Figure.5 Noise Current in a NMOS

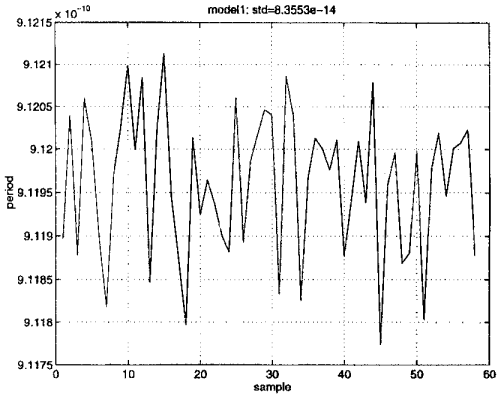


Figure.6a Random Jitter Simulation Using Model 1

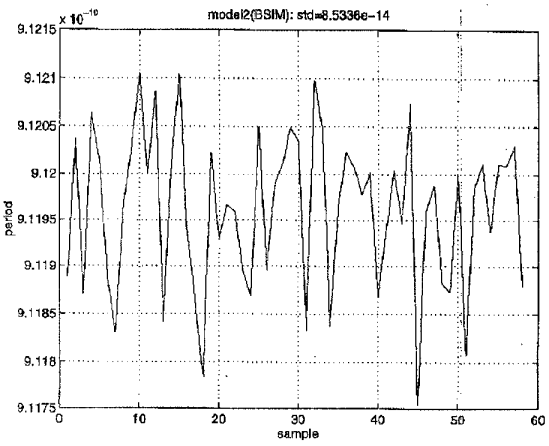


Figure.6b Random Jitter Simulation Using Model 2

Structure 1	W/L (um/um)
NMOS	7.2/1.3
PMOS	18/1.3
Structure 2	W/L (um/um)
biased PMOS	24/0.6
biased NMOS	5/0.6
differential pair NMOS	4/0.6
Structure 3	W/L (um/um)
Diode connected PMOS	27/0.6
biased PMOS	7.5/0.6
differential pair NMOS	27/0.6
biased NMOS	30/0.6

Table 2: Device Sized of Three Different VCO Structures

	Jitter(ps)
Structure 1	0.125
Structure 2	0.342
Structure 3	0.607

Table 3: Simulated Jitter in 3 Different VCO Structures

5. CONCLUSIONS

A comparison of the jitter performance due to device noise of three CMOS ring oscillators designed in a 0.5u CMOS process has been made. These comparisons show that the simple CMOS inverter-based structure which has less devices contributing to the device noise offers better jitter performance. It has also been observed in these simulations that noise contributed while devices are operating in the triode region plays a significant role in the overall noise performance and that the simple noise model that has a discontinuity in the spectral density between the ohmic and saturation regions of operation gives results very similar to those obtained with a better but more complicated noise model.

6. REFERENCE

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