A 2GHZ VCO WITH PROCESS AND TEMPERATURE COMPENSATION

Huiting Chen Edward Lee Randall Geiger
Department of Electrical and Computer Engineering
Iowa State University
Ames, IA50011, USA

ABSTRACT

A CMOS VCO with inherent compensation for temperature and process variations is presented. In thenew design, the VCO input control is divided into two parts. One is controlled by a temperature and process compensation bias circuit and the other is controlled by an external input. A phase locked loop is used as the temperature and process compensation bias circuit. Two ideally identicalVCOs are used. The control voltage of the VCO in the PLL will track the temperature and process variations. This control voltage is fed back to the VCO outside the loop. Simulation results show the total variation in the VCO frequency over a 100 °C temperature range and over the fast and slow process corners is about ±1.7 %. This is reduction of in excess of a factor of 12 when compare to a conventional VCO design based on the same delay stage.

I. INTRODUCTION

Recntly, Voltage Controlled Oscillators (VCOs) have been successfully used in high-speed clock recovery systems [1,2]. Typically, the required tuning range of the VCO is ±20% of the center frequency. This large tuning range is needed primary to enable clock recovery circuit to compensate for temperature and process variation. This results in very high gain (control voltage to frequency) requirement for VCO. Consequently, the VCO is sensitive to the noise in the system and thus becomes a source of jitter. In an attempt to minimize this sensitivity, loop filter in Phase Locked Loop (PLL) is generally designed so that the variation of the control voltage of the VCO is also large, this requires that the charge pump or loop filter have a large voltage swing as well.

This paper focuses on reducing the temperature and process dependence of the VCO. In this design,A CMOS ring oscillator structure is used and the VCO control input is divided into two additive parts. The temperature and process compensation bias circuit controls one part and an external voltage controls the other. The temperature and process compensation bias circuit is a PLL locked to a stable reference frequency; 100 MHz frequency in our example. If the reference frequency input of the PLL is temperature and process independent, the control voltage of the VCO in the PLL will track the temperature and process variations. This control voltage is fed back as a control voltage to the second VCO. Simulation results show that the second VCO has a temperature and process sensitivity of about ± 1.7% over the fast and slow process corners and over a 100 °C temperature range.

The main concept of this design is discussed in details in Section II. The component implementations of the design are discussed in section III.

II. THE ARCHITECTURE OF TEMPERATURE AND PROCESS COMPENSATION VCO

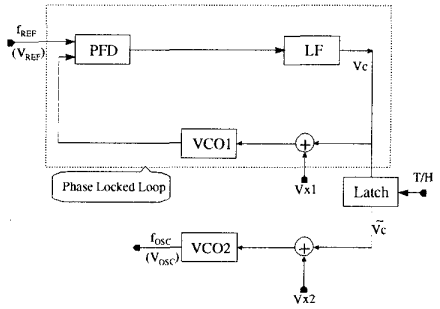

Fig (1) Basic Architecture of temperature and process compensation VCO

The basic structure of a temperature and process compensated VCO is shown in Fig (1). The PLL is comprised of three basic elements, a Phase-Frequency Detector (PFD), a Loop Filter (LF) and a VCO. The VCO has two summed control inputs: one from the output of the loop filter and the other from an external input through V_{x1}.

The operation of this structure will be described by first assuming that the external inputs to the VCOs, V_{x1} and V_{x2}, are both zero. A latch is shown in the path connecting the Vc control input of VCO1 to that of VCO2. When the latch is placed in the Hold mode, the PLL can be put in a sleep mode. In this mode, any jitter in $\tilde{V}_c$ due to jitter in the PLL will be blocked, process compensation will be maintained, power dissipation in the PLL will be decreased and the operating-time noise contributed to the system due to switching in the PLL will be eliminated. The PLL can remain in the sleep mode indefinitely if no major temperature fluctuations are sensed or can be periodically energized to update $\tilde{V}_c$ for temperature variations.

Process and temperature compensation for VCO2 can be achieved with $\tilde{V}_c$ when the latch is in the track mode. If the reference frequency of the PLL is temperature and process independent, then the frequency of the VCO1 is also independent on the temperature and process provided the PLL is locked. If the structures of the VCO1 and VCO2 are identical, the temperature and process variations would

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be nearly the same differing slightly due to random mismatch effects and small thermal gradients across the die.

The Vx1 input to VCO1 ideally has no impact on the compensation characteristics of the PLL. It is provided to facilitate obtaining architectural symmetry between the delay stages in the VCOs. The V_{x2} input to VCO2 will serve as the control input to VCO2, the gain of the VCO (freq./V_{x2}) can be made very small. This low VCO gain is desirable for reducing jitter in high-speed communication circuits where the VCO is used in a high frequency PLL for clock and data recovery.

III. 2GHZ IMPLEMENTATION

The high-frequency implementation will be focused on systems where the nominal operating frequency of VCO2 is 2GHz and where the maximum variations required on the VCO2 output is at most ± 1%. Since a data rate variation of ± 1% or less is typical of what is seen in standards for high-speed data communication networks, a VCO with this narrow adjustment range should be useful for building low-jitter clock and data recovery transceivers.

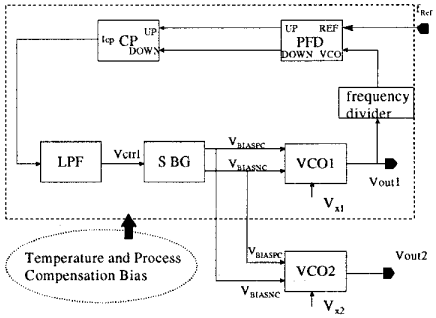

Fig (2) The schematic of temperature and process compensation VCO

A specific implementation of the structure of Fig. (1) is shown in Fig (2). Two VCOs with identical structure are used. A frequency divider is used to down converter the output frequency of VCO1 to 100MHz. The delay stages in the VCO are fully differential input and output stages with both current source and load biasing. The PFD provides both an up and a down signal to the Charge Pump (CP). The output current of the CP is filtered through the low-pass filter. The self-bias generator converts one control voltage to two. The design was implemented in a 0.35u process provided by Hewlett Packard that is available through the MOSIS program. The details of the following design discussion are applicable specifically to that process.

3.1 Delay Stage

The delay stage of the VCO is shown in Fig. (3). The compensation for the temperature and process is provided by V_{BIASNC} and V_{BIASPC}. Since process and temperature compensation which require a large adjustment range is provided by V_{BIASNC} and V_{BIASPC}, the small delay adjustment range that must be provided byVx will require only small changes in the tail current. This can be achieved by making M9 very small compared to M8. M7 is used to limit the output voltage swing and to increase to operation frequency of the VCO.

Equation (1) gives an approximate expression for the delay of the delay stage in terms of the total tailcurrent

$$T_d = \frac{C_{eff}}{\sqrt{2 * k * I_{tail}}} \qquad (1)$$

where T_d is the average delay of the high to low and the low to high transition times, C_{eff} is the effective delay stage output capacitance, I_{tail} is the differential pail tail current and

$$k = \frac{\mu C_{ox} W_1}{L_1}.$$

Since I_{tail} is the sum of I_{tailn} and I_{tailx}, the delay can be expressed as

$$T_d = \frac{C_{eff}}{\sqrt{2 * k * (I_{tail\,n} + I_{tailx})}} \qquad (2)$$

If the percent change in the delay due to changes in the current I_{tailx} is assumed to be small and if L8 and L9 are assumed to be the same, the change in delay can be given as

$$\frac{\Delta T_d}{T_d} = \frac{\Delta I_{tailx}}{I_{tail}} = \frac{2 * W_9 * V_{EB9} * \Delta V_x}{W_8 * V_{EB8}^2} \qquad (3)$$

where V_{EB8} and V_{EB9} are the excess bias voltages of M8 and M9.

Since this percentage change in delay must be provided over all temperature and process variations, it follows that

$$\frac{W_8}{W_9} < \frac{T_d}{\Delta T_d} * \frac{2 * V_{EB9} * \Delta V_x}{V_{EB8}^2} \qquad (4).$$

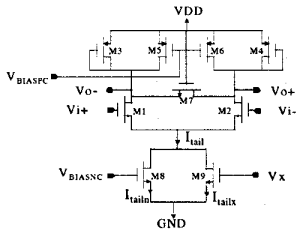

Fig (3) Delay Cell of the VCO

3.2 VCO

The VCO[1] structure along with the Self-Bias Generator are shown in Fig (4).

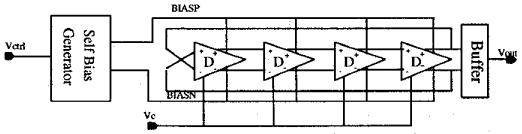

Fig (4) The whole structure of VCO

The output buffer serves two purposes. It provides a differential to single-ended conversion and isolates the influence of any loading from the frequency of oscillation of the VCO.

Circuit details of the Self-Bias Generator and the Buffer appear in Fig (5).

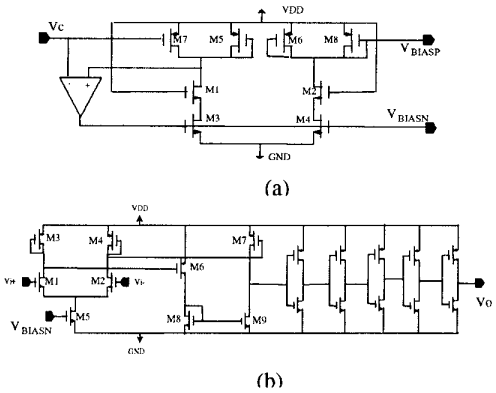

Fig (5) The schematic of self bias generator (a) and Output buffer (b)

3.3 Phase Frequency Detector

The Phase Frequency Detector (PFD) used in the design appears in Fig. (6). The detector is a rising-edge detector that generates UP and DOWN pulses on the rising edges of f_{REF} and f_{OSC}. The gate sizes in the UP path are the same as those of the corresponding gates in the DOWN path.

If f_{REF} leads f_{OSC}, the UP pulse is wider than the fixed DOWN pulse with the UP pulse width being linearly dependent upon the amount of phase lead. Iff$_{OSC}$ lags f_{REF}, the DOWN pulse is wider than the fixedUP pulse with the DOWN pulse width being linearly dependent upon the amount of phase lag. When the PLL is locked, theUP and DOWN pulses are ideally identical and of fixed width.

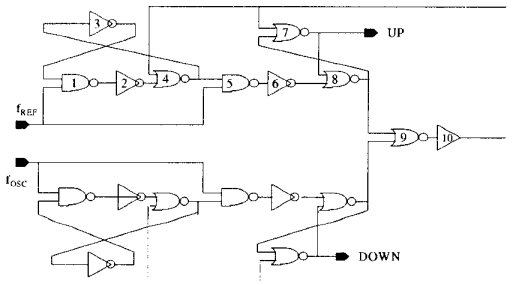

Fig. (6) The schematic of PFD

Fig. (7a) shows the relationship between the ideal UP and DOWN pulses when f_{REF} leads f_{OSC}. In this figure, we actually show a frequency difference as well. For the purpose of explanation, the amount of phase lead indicated grossly over exaggerates what would be anticipated if the phase locked loop were in or near to lock. From this figure, the fixed down pulse width and growing up pulse width are apparent. Fig. (7b) shows the corresponding relationship when f_{REF} lags f_{OSC}.

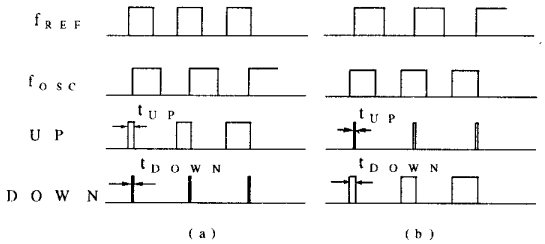

Fig (7) UP and DOWN waveform. (a)rising-edge off_{REF} leads that of f_{OSC}. (b) rising-edge off_{REF} lags that of f_{OSC}.

3.4 Charge Pump

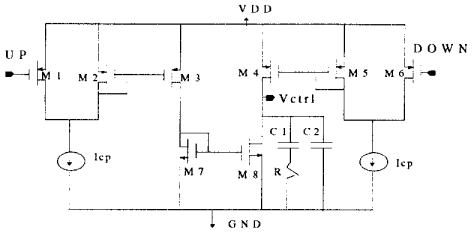

Fig. (8) the Charge Pump and Loop Filter

A charge pump along with the lowpass filter are shown in Fig. (8). The charge pump is used to convert the logical signals from the PFD into analog signals for controlling the VCOs. Ideally, when UP is active, the charge pump discharges the capacitors by mirroring the current Icp to the output as a sinking current for the duration of the UP pulse. Correspondingly, when DOWN is active, the charge pump charges the capacitors by mirroring Icp to the output as a sourcing current for the duration of the DOWN pulse.

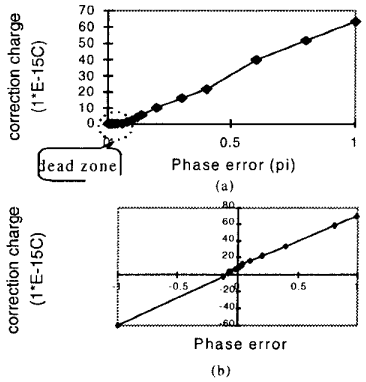

Fig (9) Phase error transfer characteristic of the VCO (a) without gate 10, has a "dead zone " (b) with delay gate 10 in PFD, no "dead zone"

Table2: Frequency of VCO2 vs. control voltage V_{x2} for best case and worst case.

Control Voltage V_{x2}*(V)	Freq. of VCO2 @ fastest process corner, and T=0 °C (best case) (GHz)**	Freq. of VCO2 @ slowest process corner, and T=100 °C (worse case) (GHz)***	Variation**** (%)
0.5	1.924	1.979	–2.82
1	2.006	1.998	0.40
1.25	2.101	2.031	3.39
VCO gain	240MHz/V	69MHz/V	

Note:
* This voltage comes from an external signal.
**The control voltage from the master PLL is 1.6 1Vin the best case
*** The control voltage from the master PLL is 0.89V in the worst case
**** Variation =