A NEW MULTIPATH AMPLIFIER DESIGN TECHNIQUE FOR ENHANCING GAIN WITHOUT SACRIFICING BANDWIDTH

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ABSTRACT

A new multistage multipath amplifier design technique is introduced that combines the formerly distinct phases of stage design and compensation. The result is an inherently stable n-stage amplifier whose gain-bandwidth product is not compromised as the number of stages is increased. The technique relies upon (n - 1) systematic pole-zero cancellations to achieve a near first-order open-loop system transfer function. The resultant amplifier architectures are attractive for realization in low-voltage processes because they accumulate gain using horizontal techniques (cascading) rather than vertical techniques (device stacking).

1. INTRODUCTION

Single stage amplifiers are often preferred for applications which require large gain-bandwidth products. These nearly first-order systems are generally stable and therefore do not suffer a reduction in the achievable gain-bandwidth product due to compensation. Usually these amplifiers achieve high DC gains without materially affecting the unity-gain frequency through the use of cascoding or gain boosting techniques. Examples include the works by Bult and Geelen [1], and Gulati and Lee [2]. Unfortunately, these techniques require vertical device *stacking* to achieve the desired gain enhancement. As a result, the gain enhanced circuits exhibit a higher minimum supply voltage than non gain enhanced circuits.

Due to the device stacking requirements, the gain-enhanced circuits are becoming less and less viable as the trend toward lower supply voltage continues.

Our goal is to develop amplifiers that are compatible with low voltage supplies while still retaining performance specifications that are comparable to those of the single stage amplifiers (i.e. simultaneous large DC-gain and high unity-gain frequency).

One method to achieve a large DC-gain without stacking devices is to cascade gain-stages. In this approach, *compensation* is required to ensure stability with feedback. Unfortunately, results presented in the literature, when compared on an equal power basis, lead to the conclusion that multistage amplifiers that are compensated using conventional techniques are unable to achieve gain-bandwidth products as large as can be achieved with the vertically-stacked single stage amplifiers.

Traditionally, amplifiers with no more than two gain stages were used because of the difficulty associated with compensating higher order structures. Compensation strategies for structures with more than two stages have recently appeared in the literature. Nested Miller Compensation (NMC) by Eschauzier et al. [3], [4] employs nested feedback loops between the overall amplifier output and the intermediate gain stages. Unfortunately, under this technique, each additional gain stage reduces the achievable gain-bandwidth product by a factor of two. Nested G_m-C Compensation by You et al. [5] involves nesting a basic block which contains both a capacitive feedback loop and a feedforward transconductance. Although the Nested G_m-C Compensation design procedure is simpler than NMC's, it yields amplifiers with performance characteristics that are comparable to those of NMC.

The amplifiers discussed here are constructed with multiple feedforward paths of differing spectral characteristics. Pole-zero cancellation in the open-loop amplifier transfer function achieves an effective first-order gain characteristic which eliminates the need for compensation to ensure stability when feedback is applied.

As shown by Kamath et al., unmatched dipoles can result in the presence of slow-settling components in the transient step response [6]. Since the proposed technique relies upon pole-zero cancellation, the existence of these mismatched pole-zero pairs can be anticipated. However, the magnitude of the slow-settling transient components can be managed by controlling the process dependent mismatch between the open-loop poles and zeros [7]. To ensure rapid settling to a given accuracy, the amount of mismatch due to process variations must be controlled and maintained below some maximum acceptable level. Therefore, this technique requires architectures that either exhibit an inherent robustness in their pole positioning or those that incorporate adaptive bias circuitry that compensates for the relevant process variations. The robustness issue is an ongoing topic of research and will not be dealt with in this paper.

In Section 2, the concept of *order-reduction* is introduced. There it is shown how the concept can be used to construct an inherently stable amplifier out of a parallel combination of higher-order systems. Section 3 reveals how a more practical implementation can be realized by collapsing the several parallel branches into one equivalent branch. The design procedure and transistor-level simulation results are presented in Section 4.

2. CONCEPT DEVELOPMENT

An amplifier is usually modeled as a linear time invariant system with an impulse response $h_T(t)$ which relates the stimulus $x(t)$ to

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the response $y(t)$. In the Frequency Domain this is written as:

$$Y(s) = H_T(s)\,X(s) \tag{1}$$

In the special case where the amplifier is composed of n paths which feed forward to a summing point that forms the output, the overall transfer function can be expressed as:

$$H_T(s) = H_1(s) + H_2(s) + \cdots H_n(s) \tag{2}$$

where the k'th term in the expansion of $H_T(s)$, (i.e. $H_k(s)$ where $1 \leq k \leq n$), corresponds to the transfer function of the k'th feedforward path in the amplifier. In what follows it will be further assumed that $H_k(s)$ is of k'th order for $1 \leq k \leq n$.

The new design strategy presented here stems from the observation that, under certain conditions, it is possible to create a system with an overall transfer function which is k'th order by summing the outputs of $(k+1)$'th and k'th order systems. This process is referred to as *order reduction* and is facilitated by pole-zero cancellation in the system transfer function.

Figure 1 illustrates the concept of order reduction. Under certain conditions, which will be derived, the overall transfer function $H'_k(s) = \frac{Y(s)}{X(s)}$ is k'th order while the constituent transfer functions $H_{k+1}(s)$ and $H_k(s)$ are $(k+1)$'th and k'th order respectively.

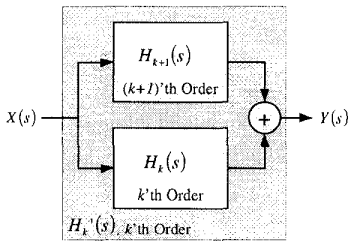

Figure 1: Block diagram of order reduction procedure

Intuitively, if $H_k(s)$ and $H_{k+1}(s)$ are designed so that at some frequency the contribution to the output of $H_k(s)$ is equal in magnitude but opposite in phase to the contribution of $H_{k+1}(s)$, then the outputs will cancel. The frequency at which the destructive interference occurs defines the location of the zero.

To derive conditions that will result in order reduction we will assume that $H_k(s)$ and $H_{k+1}(s)$ are both all pole transfer functions of the form:

$$H_k(s) = \frac{A_k}{\left(1 - \frac{s}{P_{k1}}\right)\left(1 - \frac{s}{P_{k2}}\right)\cdots\left(1 - \frac{s}{P_{kk}}\right)} \tag{3}$$

It will be further assumed that each of the poles are real and positioned in the left half plane. To simplify the notation, the poles will be numbered in the order of decreasing magnitude (i.e. $|p_{k1}| > |p_{k2}| > \cdots > |p_{kn}|$).

It will be further assumed that the poles of $H_k(s)$ will coincide with the k highest frequency poles of $H_{k+1}(s)$. Under these assumptions $H'_k(s)$ can be expressed as:

$$H'_k(s) = \frac{(A_k + A_{k+1})}{\prod_{i=1}^{k-1}\left(1 - \frac{s}{P_{ki}}\right)}\left(\frac{1 - \frac{A_k s}{P_{k+1,k+1}(A_k + A_{k+1})}}{\left(1 - \frac{s}{P_{kk}}\right)\left(1 - \frac{s}{P_{k+1,k+1}}\right)}\right) \tag{4}$$

If

$$P_{kk} = \left(\frac{A_k + A_{k+1}}{A_k}\right) P_{k+1,k+1} \tag{5}$$

is satisfied, then the zero exactly cancels the second lowest frequency pole P_{kk} and (4) reduces to:

$$H'_k(s) = \frac{(A_k + A_{k+1})}{\left(\prod_{i=1}^{k-1}\left(1 - \frac{s}{P_{ki}}\right)\right)\left(1 - \frac{s}{P_{k+1,k+1}}\right)} \tag{6}$$

Notice that (6) is k'th order even though it is composed of k'th and $(k+1)$'th order systems. Thus order reduction has occurred. Certain relationships among the spectral properties of the constituent systems were required for the reduction to take place. Specifically, the order-reduction constraints are:

1. All poles of $H_k(s)$ and $H_{k+1}(s)$ are distinct, real and negative.
2. The k highest frequency poles of $H_{k+1}(s)$ are coincident with the k poles of $H_k(s)$.
3. The lowest frequency poles of $H_{k+1}(s)$ must satisfy the relationship:

$$P_{k+1,k+1} = \left(\frac{A_k}{A_k + A_{k+1}}\right) P_{kk} \tag{7}$$

Recursive application of the order reduction concept can be used to design an n-stage amplifier with a first-order response. Since the resultant amplifier is first-order, no post-design compensation step is required to ensure stability with feedback. Figure 2 illustrates how the concept is applied to design a three stage amplifier. Notice that the amplifier is composed of three parallel systems. One is first-order, another is second order and the third system is third order. In general, a n-stage amplifier consists of n parallel systems that incrementally vary in complexity from first-order to n'th order. The higher order systems create the large gain at lower frequencies while the lower order systems extend the bandwidth by providing gain at high frequencies.

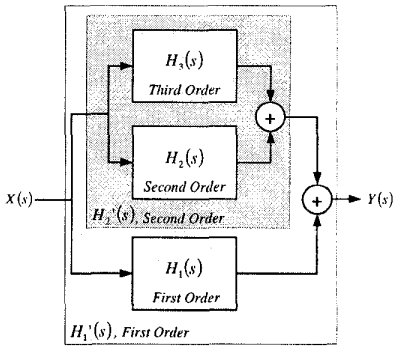

Figure 2: Design of three stage amplifier using multipath compensation

The relationships required among the spectral characteristics of the constituent systems that are necessary to achieve a first-order overall response can be easily derived by recursively applying the order reduction concept. For an n-stage amplifier the requirements are:

$$P_{ki} = P_{ii} \qquad \text{where } 1 \leq i \leq n-1 \text{ and } i+1 \leq k \leq n \tag{8}$$

and

$$P_{kk} = P_{nn}\left(\frac{\sum_{i=k}^{n} A_i}{A_k}\right) \qquad \text{where } 1 \leq k \leq n-1 \quad (9)$$

where P_{ki} is the i'th pole of $H_k(s)$ where $1 \leq i \leq k$.

Equation (8) specifies that each pole of every constituent system gets mapped onto one of n discrete frequencies $P_{11} \cdots P_{nn}$ and (9) specifies the relative spacing between the P_{ii}'s. Figure 3 illustrates the meaning of (8) and (9) for a four stage amplifier.

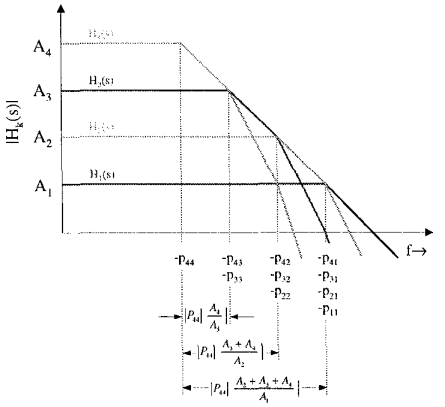

Figure 3: Approximate magnitude plots of the constituent systems' required transfer functions

As an example of (9) for a four-stage amplifier, if the stage gains, A_k $1 \leq k \leq 4$, and a low-frequency pole, P_{44}, are known, the remaining pole locations can be determined by the following equations:

$$P_{33} = P_{44}\left(\frac{A_3 + A_4}{A_3}\right) \quad (10)$$

$$P_{22} = P_{44}\left(\frac{A_2 + A_3 + A_4}{A_2}\right) \quad (11)$$

$$P_{11} = P_{44}\left(\frac{A_1 + A_2 + A_3 + A_4}{A_1}\right) \quad (12)$$

The following numerical example demonstrates the order reduction technique.

$$H_T(s) = H_1(s) + H_2(s) + H_3(s) \quad (13)$$

$$H_T(s) = \frac{10}{\left(1 + \frac{s}{821000}\right)} + \frac{200}{\left(1 + \frac{s}{821000}\right)\left(1 + \frac{s}{41000}\right)} + \frac{8000}{\left(1 + \frac{s}{821000}\right)\left(1 + \frac{s}{41000}\right)\left(1 + \frac{s}{1000}\right)} \quad (14)$$

$$H_T(s) = \frac{8210}{1 + \frac{s}{1000}} \quad (15)$$

3. CIRCUIT REALIZATION

In the previous section, the concept of an inherently compensated multipath amplifier was presented. It was shown that recursive application of the order reduction principle allows us to design an n-stage amplifier that exhibits a first-order response. In this section, a circuit that implements the multipath compensation technique is presented.

The block diagram of a three stage amplifier shown in Figure 2 suggests an obvious circuit realization. One could simply replace each of the $H_k(s)$ blocks with a k-stage common source transconductance amplifier.

A strategy for the design of such a system would be to first design the output stage $H_1(s)$. It should exhibit a first-order transfer characteristic with an acceptable gain-bandwidth product while driving the required capacitive load. The architecture of the stage should be chosen to ensure compatibility with low supply voltages. The resultant single stage amplifier would have a modest DC gain because traditional vertical gain enhancement methods are not acceptable. Subsequently, a second order system, $H_2(s)$, and a third order system, $H_3(s)$, are added to boost the low frequency gain without compromising the gain-bandwidth product of the original stage. The multipath architecture results in an amplifier that exhibits a single pole transfer characteristic with a large DC gain and a unity gain frequency equal to that of the original output stage. Although this type of realization is straightforward and convenient, it has a few drawbacks. First, as expressed in (8), matching of the pole locations in each of the parallel branches is required. If the amplifier is constructed with n independent parallel branches, precise matching may not be possible. A method which guarantees exact coincidence of the poles would be more appealing. Second, traditional n-stage amplifiers only have n stages. But the proposed architecture requires $\frac{(n+1)n}{2}$ stages which is always greater than n for a multistage amplifier. These additional stages consume both die area and power. A realization that does not consume excess power or die area is desirable. Finally, the proposed architecture forms the output signal by summing n signals at the output node. This could be performed by making each of the $H_k(s)$ blocks a transconductance amplifier and summing currents. However, this approach reduces the maximum obtainable unity gain frequency for a given amount of power because each of the n branches contributes parasitic capacitance to the output node.

For these reasons, an architecture that consolidates the n parallel branches of the architecture into one lower complexity branch is desirable. With this goal in mind, consider again $H_T(s)$ from (2) which is repeated here as:

$$H_T(s) = \sum_{k=1}^{n} H_k(s) \quad (16)$$

Substituting for $H_k(s)$ from (3) and enforcing (8) yields:

$$H_T(s) = \sum_{k=1}^{n}\left(\frac{A_k}{\prod_{i=1}^{k}\left(1 - \frac{s}{P_{ii}}\right)}\right) \quad (17)$$

Consider the scenario where the DC gain of each stage, A_k, can be decomposed into the product of other more fundamental gain coefficients such as:

$$A_k = \prod_{i=1}^{k} \tilde{A}_i \quad (18)$$

where the ˜ is used to signify that A_k and $\tilde{A}_i$ are not necessarily the same. Substituting (18) into (17) results in:

$$H_T(s) = \sum_{k=1}^{n}\left(\prod_{i=1}^{k}\left(\frac{\tilde{A}_i}{1 - \frac{s}{P_{ii}}}\right)\right) \quad (19)$$

which can also be written as:

$$H_T(s) = \frac{\tilde{A}_1}{1-\frac{s}{P_{11}}}\left(1+\frac{\tilde{A}_2}{1-\frac{s}{P_{22}}}\left(\cdots\left(1+\frac{\tilde{A}_n}{1-\frac{s}{P_{nn}}}\right)\right)\right) \quad (20)$$

When $H_T(s)$ is written in this form it makes it easier to see that it can be realized as a single branch consisting of single pole amplifier stages and adders. Figure 4 illustrates the realization.

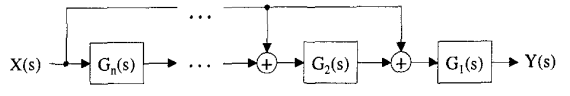

Figure 4: Alternative implementation of a multipath compensated amplifier

Note that although this diagram has just as many blocks as the block-diagram of Figure 2, they are lower order blocks. In fact, the frequency response of each of the blocks in Figure 4 corresponds to a single-pole low-pass response of the form:

$$G_k(s) = \frac{\tilde{A}_k}{1-\frac{s}{P_{kk}}} \quad (21)$$

Consolidating the branches has reduced the total number of required stages from $\frac{(n+1)n}{2}$ to n. This reduction in complexity implies reduced area and power requirements. Furthermore, the consolidation also ensures that the pole coincidence requirements expressed by (8) are satisfied. Additionally, higher bandwidths for a fixed amount of power are obtainable using this architecture because there are fewer devices contributing parasitic capacitance to the output node.

Consolidation also simplifies the relation that specifies the required pole spacing. Substituting (18) into (9) and casting the result as a recursive relation yields:

$$P_{kk} = P_{nn} + \tilde{A}_{k+1}P_{k+1,k+1} \qquad 1 \le k \le n-1 \quad (22)$$

As an example of the recursion, consider a four-stage amplifier. If the stage gains, $\tilde{A}_k$ $1 \le k \le 4$, and a low-frequency pole, P_{44}, are known, the remaining pole locations can be determined by computing the following equations in order:

$$P_{33} = P_{44} + \tilde{A}_4 P_{44} \quad (23)$$

$$P_{22} = P_{44} + \tilde{A}_3 P_{33} \quad (24)$$

$$P_{11} = P_{44} + \tilde{A}_2 P_{22} \quad (25)$$

Equation (22) has a physical interpretation. The product $\tilde{A}_i P_{ii}$ found in the equation corresponds to the gain-bandwidth product of the i'th rightmost stage of the amplifier. In words, the equation says, the magnitude of the pole at stage k should exceed the magnitude of the dominant pole by a value equal to the gain-bandwidth product of the preceding stage. Figure 5 illustrates the relationship among the poles in terms of the $\tilde{A}_i$'s for a five stage amplifier.

4. TRANSISTOR-LEVEL SIMULATION

Previous sections of this document introduced the concept of multipath amplifier design and suggested architectures for implementing the concept. In this section, a transistor-level implementation of a multipath amplifier is considered.

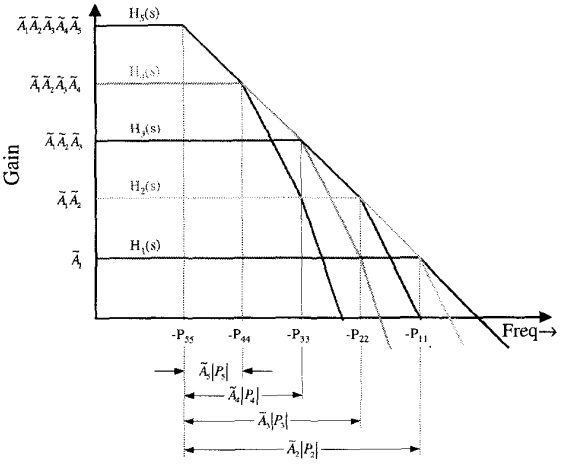

Figure 5: Required pole locations in terms of $\tilde{A}_i$'s for a five stage multipath compensated amplifier

Figure 6 shows the schematic diagram of a three stage amplifier that is the direct implementation of the block diagram shown in Figure 4. In order to avoid the possibility of other factors complicating the simulation results which might lead to incorrect conclusions, the circuit was kept as simple as possible.

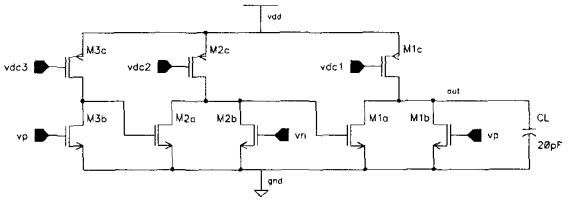

Figure 6: Circuit that was simulated to demonstrate the validity of the multipath compensation concept

The circuit consists of three stages. Stage one, termed the output stage, is composed of transistors M1a, M1b and M1c, stage two is made of M2a, M2b, and M2c, and stage three is composed of M3b and M3c. The circuit contains three different signal paths from the input to the output node. A low gain, high frequency path is created by transistor M1b. A high gain, low frequency path is created by transistors M3b, M2a, and M1a. A mid gain, mid frequency path is derived from transistors M2b and M1a.

4.1. Design Procedure

The first step in the design procedure is to design the output stage. This step is important because the designer has to make the critical, application dependent, design tradeoff between power consumption and gain-bandwidth for the overall amplifier. The decision has implications on die area as well.

In the output stage of Figure 6, for fixed DC bias voltages, increased quiescent current results in an increase in the unity gain frequency, however, the increase is not linear. The unity gain frequency is given by the ratio of the transconductance of one of the

drivers to the total capacitance seen on the output node $\left(\frac{g_m}{C_{out}}\right)$. In order to maintain the same DC bias voltages while increasing the current, a proportional increase in the transistors' widths is required. Unfortunately, the increased widths are accompanied by a proportional increase in parasitic capacitance on the output node. The parasitic capacitance on the output node is directly proportional to the quiescent current, I, while the transconductance is proportional to $\sqrt{I}$, thus making the relationship between power and bandwidth nonlinear.

After the output stage is designed, the remaining stages need to be designed such that the design criteria expressed in (8) and (22) are satisfied. One can attempt to derive analytical expressions for the stage currents and device sizes that will satisfy the conditions specified in the equations. However, due to the effect of device parasitics not accounted for in the small signal model, especially the gate-drain capacitances, these equations will not result in accurate pole-zero cancellations. As a result, a computer simulation was used as a part of the design process. Figure 7 illustrates a computer-aided design procedure. First, the entire amplifier is designed using initial guesses at the required stage currents. Given these initial conditions, the pole-zero cancellation won't be exact and the response of the system will not be first-order.

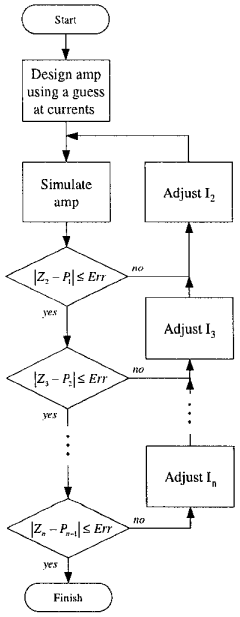

Figure 7: Design procedure used to optimize the amplifier response

Next, a nested iteration is begun where the amplifier is simulated and the poles are compared to the zeros. If the separation of a pole and zero is greater than a given threshold, then the corresponding stage's current is adjusted and the process continues. Notice that the procedure is *nested*. In this situation, this means that before a change is contemplated for a given stage, that all stages to the right already meet the convergence criterion. Nesting requires more computation than a non-nested approach but it is necessary to improve the convergence of the algorithm.

An amplifier was designed for a 100MHz unity-gain frequency while driving a 20pF load with the proposed design methodology using a typical 0.5μ CMOS Process. HSPICE level 49 models derived from parametric data were used. The resultant circuit parameters are presented in Table 1.

Table 1: Circuit parameters

Quiescent Currents		
I_{Q1}	20.0mA	
I_{Q2}	78.0μA	
I_{Q3}	0.288μA	
Transistor	Width	Length
M1a	283λ	2λ
M1b	283λ	2λ
M1c	3787λ	2λ
M2a	14λ	16λ
M2b	14λ	16λ
M2c	107λ	16λ
M3b	3λ	224λ
M3c	3λ	48λ
Other Parameters		
C_L	20pF	
V_{DD}	3.3V	
V_{SS}	0.0V	
V_{IQ}	1.65V	
V_{OQ}	1.65V	
V_{DC1}	1.9V	
V_{DC2}	1.65V	
V_{DC3}	1.65V	

Figures 8 and 9 contain plots of the simulated AC open loop and unity gain transient step responses of the multipath compensated amplifier that was designed. The simulations predict a 90 dB DC gain and a unity gain frequency of 100MHz while using 68mW to drive a 20pF load. The response appears first-order except for the appearance of a high-frequency right half plane zero whose effect is inconsequential because it occurs at frequencies that are several orders of magnitude greater than the unity gain frequency. With a 0.5 Volt step input, the amplifier settles to 90% of its final value in 9.1nS and to 99% in 11.3nS. The pole-zero cancellations of this structure are not perfect, thus some deterioration in the settling time is experienced.

5. CONCLUSION

In this paper we introduced the concept of *order reduction* as a method of constructing a k'th order system out of a combination of k'th and $(k+1)$'th order systems. It was shown how a nested iteration of the order reduction procedure can be used to design an n-stage multipath amplifier. The resultant amplifier exhibits a first-order response and therefore does not require any additional compensation. Since additional compensation steps are not required, the resultant amplifiers do not exhibit the reduction in achievable gain-bandwidth product for a given amount of power that is usually associated with compensation. To demonstrate the feasibility of the concept, simulation results for a simple three stage amplifier were presented that predict a 90 dB DC gain and a unity gain frequency of 100MHz while driving a 20pF load. The unity-gain step response achieves 10% settling in 9.1nS and 1% settling in 11.3nS.

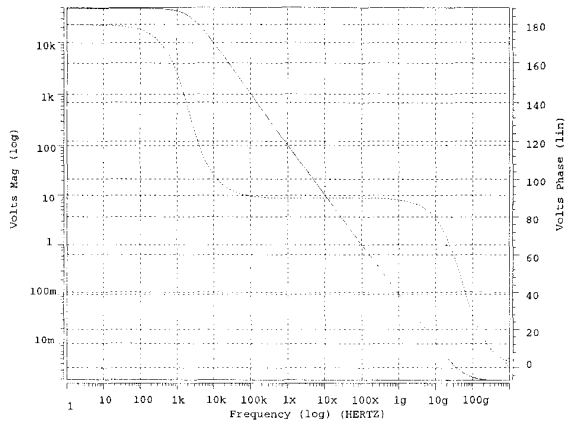

Figure 8: Simulated open loop response of the multipath compensated amplifier

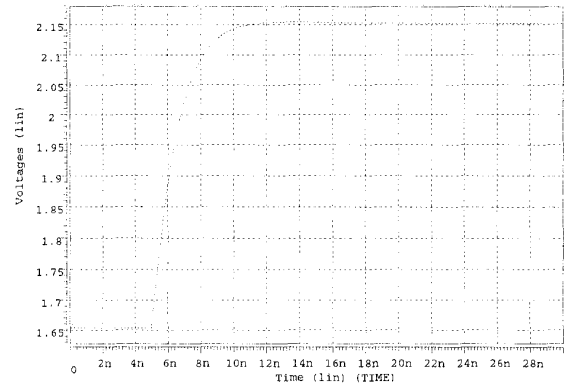

Figure 9: Simulated unity-gain step response of the multipath compensated amplifier

6. ACKNOWLEDGMENT

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