AMPLIFIER DESIGN FOR FAST SETTLING PERFORMANCE

by

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Abstract

A design strategy for minimizing a feedback amplifier's step-response settling time is introduced. Central to this approach is the clear identification of the independent design parameters characterizing the amplifier and the introduction of a figure of merit for assessing the settling performance of an amplifier that is independent of power, supply voltage and capacitive loading. With this approach, the settling performance of a given amplifier architecture can be optimized and the relative performance of different amplifier architectures can be assessed. Emphasis in this paper is on the two-stage operational amplifier architecture but the technique readily extends to other widely used operational amplifier structures.

Introduction

Due to the critical importance played by operational amplifier performance in almost all integrated analog systems, operational amplifier design has received considerable attention throughout the years. In particular, two-stage structures have been widely studied and reported in the literature [1,2,3] as well as in textbooks focusing on linear circuit design [4,5,6]. Some have attempted to formalize systematic design methodologies for this structure including [4,6]. Collectively, the authors have derived expressions for a diverse group of amplifier performance parameters including DC gain (Ao), gain bandwidth product (GB), slew rate (SR), phase margin, settling time, etc. It is well known that there are interrelationships between the performance parameters and design parameters such as bias current levels and device sizes. Invariably tradeoffs between the performance parameters are made during the design process. Although parameters such as phase margin, gain bandwidth product, slew rate, etc. may be related to settling time, in many applications, the settling time of the amplifier itself is of primary concern with little or no concern about the values of the other parameters. This paper focuses solely on designing amplifiers for fast settling. The issue of rapid settling has received only limited attention in the literature [7,8].

It is well known that several application and design variables affect the settling time of a given amplifier architecture. These include the size of the capacitive load that must be driven, the sizes of the transistors, the bias current levels, the supply voltage and the power supplied to the amplifier. What is less known, however, are how these variables affect the settling time. For example, it is often argued that increasing the tail current of a differential pair will result in faster settling. However, increasing the tail current also affects operating points, power dissipation, phase margin, and signal swing. An increase in tail current may require subsequent changes in device sizing or component values to re-establish the required operating points or signal swings. These latter changes will, in turn, impact the settling time making it less clear what benefits, if any, are derived from increasing the tail current.

This problem can be addressed by deriving the explicit relationship between the performance parameter of interest and the set of design degrees of freedom associated with the chosen circuit topology. The process of identifying a practical set of independent design parameters is discussed in [9]. For notational convenience, the key relationships between the performance parameters and the design parameters for the two stage operational amplifier of Figure 1 that were presented in [9] are reviewed here.

Parameter Spaces for Amplifier Design

In the two-stage amplifier of Figure 1, the most natural set of design parameters is the set $S_{natural}$ defined by

$S_{NATURAL}$ = {W1, L1, W3, L3, W5, L5, W6, L6, W7, L7, Iss, Cc}

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In contrast to the natural design parameter set which contains the minimal set of design parameters required to fully define an amplifier realization, the performance parameters such as the gain-bandwidth product (GB), open-loop DC gain (Ao), phase margin (ϕm) or pole Q, slew rate (SR), settling time (Ts), and power dissipation (P) which are available in the literature and textbooks are expressed in terms of an alternate but much larger parameter set.

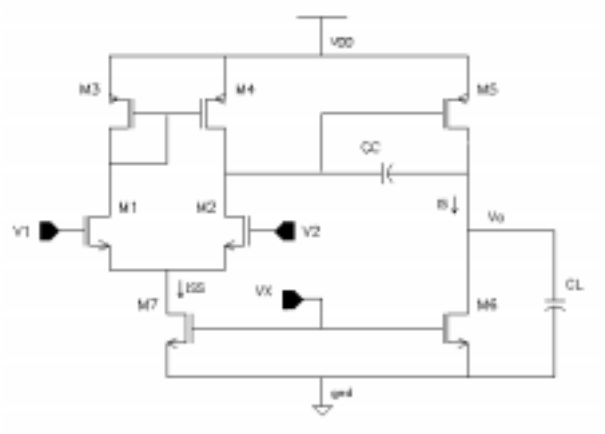

Figure 1 Basic two-stage operational amplifier

$$S_{ALTERNATE} = \{g_{oo}, g_{od}, g_{m5}, C_C, V_{GS1Q}, V_{GS3Q}, V_{GS5Q}, V_{GS6Q}, V_{GS7Q}, I_{SS}, g_{o2}, g_{o4}, g_{o5}, g_{o6}\}$$

The difficulty of using this parameter set is associated both with its large size and the inherent interrelationships that exists between parameters in the set.

In [9] a practical alternative to the natural design parameter space, which includes a minimal set of design parameters, was introduced. It simplifies the fundamental design equations to the point that performance optimization becomes viable and, in particular, the expression for settling time is sufficiently simplified so that insight into how settling time can be optimized becomes apparent. The alternate formulation is based on the design parameter space

$$S_{PRACTICAL} = \{P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, n1, n3, n5, n6, n7\}$$

where P is the total power dissipation, θ is the ratio of the magnitude of the quiescent current in M5 to the tail current Iss, V_{EBk} is the excess bias voltage for the k'th transistor defined by $V_{EBk} = V_{GSQk}-V_{Tk}$ and n_k is the minimum feature scaling factor. This alternate practical design parameter space was chosen for several reasons. One is because of the simplification of the expressions that results for some of the key performance parameters and another is the inherent decoupling between design parameters that exists for some fundamental performance parameters. A third is the inherent relationships that exist between common mode input range and output signal swing and the excess bias voltages.

The relationships between this design parameter space and the natural design parameter space are readily obtained. These relationships are

$$I_{SS} \cong \frac{P}{V_{DD}(1+\theta)} \tag{1}$$

for M1 to M4,

$$I_{DQ}=Iss/2 \tag{2}$$

for M5 and M6,

$$I_{DQ}=\theta Iss \tag{3}$$

and for M7,

$$I_{DQ}=Iss \tag{4}$$

The W/L ratios for all transistors are given by the expression

$$\left(\frac{W}{L}\right)_i \cong \frac{2I_{DQ}}{\mu_i C_{OX} V_{EBi}^2} \tag{5}$$

The values for W and L for each of the transistors are obtained from the relationship

$$L_k = n_k L_{min},$$
$$W_k = L_k(W/L)_k \quad \text{for } (W/L)_k > 1 \tag{6}$$

and

$$W_k = n_k W_{min},$$
$$L_k = W_k/(W/L)_k \quad \text{for } (L/W)_k > 1 \tag{7}$$

The common mode input range and the output signal swing are also of interest. In terms of the practical parameter space, these levels are given by the expressions

$$V_{i\max} = V_{DD} - \left|V_{EB3}\right| + V_{T1} + V_{T3} \tag{8}$$

$$V_{i\min} = V_{EB1} + V_{EB6} + V_{T1} \tag{9}$$

$$V_{o\max} = V_{DD} - \left|V_{EB5}\right| \tag{10}$$

$$V_{o\min} = V_{EB6} \tag{11}$$

Settling Time Characterization

The step response of a non-ideal feedback amplifier often progresses through two distinct phases of operation as the output settles to its steady-state value. Depending upon the magnitude of the input step and the architecture under consideration, the amplifier output may *slew* for a finite period of time directly after the application of the input step. Eventually, the amplifier will discontinue slewing and enter a linear mode of operation. Two possible step responses for a finite gain amplifier are depicted in Figure 2. In Figure 2a, an initial slew mode is shown followed by a linear settling interval. In Figure 2b, the amplifier remains in the linear mode throughout the entire settling interval.

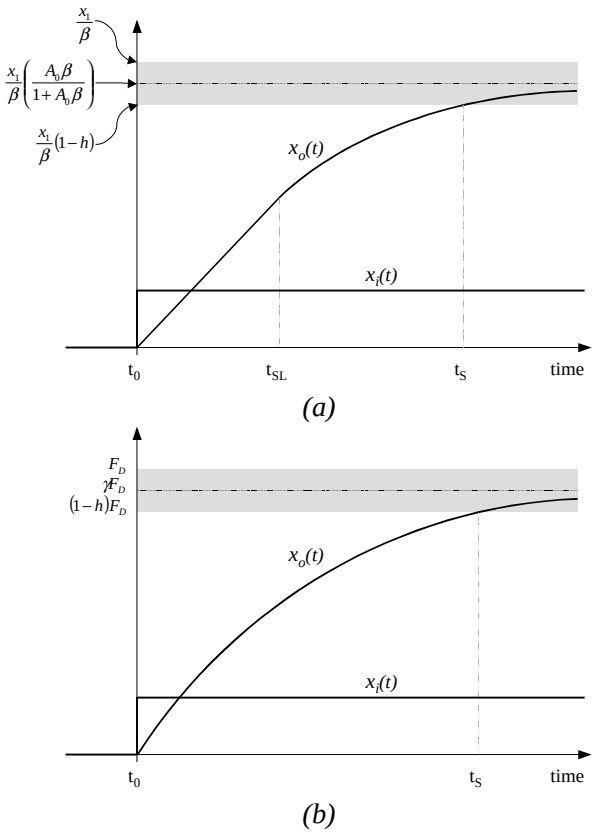

Figure 2 Two example step responses (a) nonlinear slewing followed by linear settling and (b) linear settling only.

It can be readily shown that the time required to settle to within h of the desired value of F_D for a step of amplitude X1 with a slew period followed by a linear settling period is given by the expression

$$T_S = \frac{\gamma F_D}{SR} + \frac{\ln\left[\dfrac{SR}{\beta GBF_D(\gamma + h - 1)}\right] - 1}{\beta GB} \tag{12}$$

where SR is the amplifier slew rate, GB is the amplifier gain-bandwidth product, β is feedback factor, Ao is the DC amplifier gain, $\gamma = \beta Ao/(1+\beta Ao)$ and $FD = X1/\beta$. The first term on the right side of (12) is the time during which the amplifier is in slew and the second term corresponds to the linear settling period. For the case of no slew, the first term vanishes yielding

$$T_S = \frac{\ln\left[\dfrac{SR}{\beta GBF_D(\gamma + h - 1)}\right] - 1}{\beta GB} \tag{13}$$

Equations (12) and (13) are not yet in terms of the proposed design parameters. If the amplifier is compensated for a pole Q of $\left(1/\sqrt{2}\right)$ which is close to the value of Q needed for a 60-degree phase margin, it follows readily that the parameters A_O, GB, and SR in (12) and (13) can be expressed in terms of the practical design parameters as

$$A_O = \frac{4}{\left(\lambda_n + \lambda_p\right)^2 V_{EB1}\left|V_{EB5}\right|} \tag{14}$$

$$GB = \frac{P}{V_{DD}(1+\theta)V_{EB1}C_C} \tag{15}$$

$$= \frac{P\left(2\theta V_{EB1} - \beta\left|V_{EB5}\right|\right)^2}{4C_L\theta\beta V_{DD}(1+\theta)V_{EB1}^2\left|V_{EB5}\right|} \tag{16}$$

$$SR = V_{EB1}GB = \frac{P\left(2\theta V_{EB1} - \beta\left|V_{EB5}\right|\right)^2}{4C_L\theta\beta V_{DD}(1+\theta)V_{EB1}\left|V_{EB5}\right|} \tag{17}$$

where the compensation capacitor C_C is given by

$$C_C = 4C_L\theta\beta\frac{V_{EB1}\left|V_{EB5}\right|}{\left(2\theta V_{EB1} - \beta\left|V_{EB5}\right|\right)^2} \tag{18}$$

Now, replacing parameters in (12) and (13) with the expressions of (14)-(18), it follows for the slew scenario that

$$T_S = \frac{4C_L\theta\beta V_{DD}(1+\theta)V_{EB1}\,|V_{EB5}|}{P(2\theta V_{EB1}-\beta\,|V_{EB5}|)^2}\left[\frac{X_1 Ao}{1+\beta Ao}+\frac{V_{EB1}}{\beta}\left(\ln\left[\frac{V_{EB1}}{X_1(\gamma+h-1)}\right]-1\right)\right] \quad (19)$$

and for the no-slew scenario,

$$T_S = \left[\frac{4C_L\theta V_{DD}(1+\theta)V_{EB1}^2\,|V_{EB5}|}{P(2\theta V_{EB1}-\beta\,|V_{EB5}|)^2}\cdot \ln\left(\frac{4\beta}{4h\beta+V_{EB1}\,|V_{EB5}|\,(h-1)(\lambda_n+\lambda_p)^2}\right)\right] \quad (20)$$

Equations (19) and (20) are expressed in terms of the practical design parameters . More importantly, however, is the observation that the total power, P, the load capacitance C_L and the supply voltage V_{DD} all appear explicitly as factors in these two equations. Thus these can be factored out to obtain a normalized settling time characteristic which has units volts defined by

$$V_{SHAT} = \frac{TsP}{V_{DD}C_L} \quad (21)$$

It thus follows from (19) that for the slew case, V_{SHAT} is given by

$$V_{SHAT} = \frac{4\theta\beta(1+\theta)V_{EB1}\,|V_{EB5}|}{(2\theta V_{EB1}-\beta\,|V_{EB5}|)^2}\left[\frac{X_1 Ao}{1+\beta Ao}+\frac{V_{EB1}}{\beta}\left(\ln\left[\frac{V_{EB1}}{X_1(\gamma+h-1)}\right]-1\right)\right] \quad (22)$$

and for the non-slew case from (20), V_{SHAT} is given by

$$V_{SHAT} = \left[\frac{4\theta(1+\theta)V_{EB1}^2\,|V_{EB5}|}{(2\theta V_{EB1}-\beta\,|V_{EB5}|)^2}\cdot \ln\left(\frac{4\beta}{4h\beta+V_{EB1}\,|V_{EB5}|\,(h-1)(\lambda_n+\lambda_p)^2}\right)\right] \quad (23)$$

The term V_{SHAT} is a figure of merit for characterizing the settling performance of an amplifier and does not depend upon the independent design parameter, P, or upon either the load capacitance or the supply voltage. The term V_{SHAT} is determined by the architecture of the operational amplifier and by the parameters used to characterize the fabrication process. It follows from an examination of (22) and (23) that V_{SHAT} is determined by the three independent design parameters θ, V_{EB1}, and V_{EB5}. The balance of the parameters that appear in V_{SHAT} are system specifications and process parameters. It also follows from (22) and (23) that the settling time improves linearly with the independent design parameter P and inversely with V_{DD} and C_L.

Settling behavior of the two-stage amplifier

In the preceding section, a figure of merit, V_{SHAT}, was introduced for characterizing the settling performance of the two stage operational amplifier. This section emphasizes the practical design tradeoffs that can be made to improve the settling performance.

Since the parameters P, V_{DD} and C_L have been normalized out of the expression for V_{SHAT}, it suffices to consider the effects of θ, V_{EB1}, and V_{EB5} on V_{SHAT}. An examination of (22) and (23) shows a nonlinear dependence on these three parameters. Although an analytical analysis of the effects of these parameters is manageable, a better appreciation for performance can be obtained numerically. In what follows it will be assumed that, power dissipation is fixed at 3.43E-4W, V_{DD}=3.3V and C_L=1pF. A 1V step input was applied in a unity gain (β=1) feedback configuration. To maintain acceptable common mode input and output signal swings the excess biases for M7 and M6 were chosen to be 0.8V. It was also assumed that a 0.35u CMOS process was available for circuit fabrication. Under these conditions, we will consider three cases. The first will focus on the effects of independently varying θ, the second on the effects of varying V_{EB5} and the third on the effects of varying V_{EB1}. Corresponding predictions of V_{SHAT} as computed by (21), (22), and (23) appear in the following tables. Also appearing in the tables are the predicted settling times and simulated values of V_{SHAT} obtained from full SPICE-level simulations of the operational amplifiers with the device sizes as extracted from (2)-(5).

Table 1 Case 1: Vary θ, Fixed V_{EB1}=0.596V, V_{EB5}=0.386V (error: +/-7mV)

Split factor, θ	T_{settle}	Vshat	Vshat (calc.)
0.62	130.9ns	13.6V	21.1V
1	83.33ns	8.64V	12.2V
1.5	70.08ns	7.28V	9.7V
3	59.3ns	6.21V	8.0V
4	58.73ns	6.02V	7.54V

Table 2 Case 2: Vary V_{EB5}, Fixed V_{EB1}=0.596V (error +/-8mV), split factor θ=3

VEB5	Settling time	Vshat	Vshat(calc.)
0.669V	53.2ns	5.59V	6.1V
0.390V	59.3ns	6.21V	8.0V
0.174V	70.67ns	7.39V	9.85V

Table 3 Case 3: Vary V_{EB1}, Fixed V_{EB5}=0.390V(error +/-0.4mV), split fact θ=3

VEB1	Settling time	Vshat	Vshat(calc.)
0.4602V	66.43ns	6.97V	8.84V
0.6032V	59.3ns	6.21V	8.0V
0.7969V	55.26ns	5.77V	7.38V

From the simulation results, it is apparent that the settling time improves as more current is split to the second stage under the assumption that total power dissipation and V_{DD} are fixed Correspondingly, raising the excess bias voltages on M_1 and M_5 improves settling as well. In addition to explicitly demonstrating the tradeoffs between the design parameters θ, V_{EB1} , and V_{EB5} and the settling time, it is apparent that settling time improves linearly with power and inversely with supply voltage and load capacitance. Finally, these results shed insight into questions such as that posed at the outset of this work about whether increasing the tail current I_{SS} will actually improve settling. In particular, Case 1 shows that under a fixed power assumption, increasing the tail current I_{SS} results in a decrease in the split factor θ and thus a deterioration of the settling time.

Conclusions

Using the traditional expressions for the performance parameters of an operational amplifier, performance optimization is difficult because the relationships among the performance parameters and the circuit's degrees of freedom are unwieldy. If the performance parameter equations are expressed in terms of the practical alternative design space that is based on relevant design parameters rather than the natural design parameters, then the expressions for some of the key performance parameters are significantly simplified. Depending upon the application, certain performance parameters are critical whereas others are not. As a result, a "one-size fits all" design procedure is not possible. Rather, the design procedure has to be tailored to reflect the priorities of the specific application.

A figure of merit, VSHAT, has been introduced for characterizing the settling performance of operational amplifiers. This figure of merit is independent of the power dissipation, total load capacitance and supply voltage for the two-stage operational amplifier. Simple expressions relating the relevant design parameters to the settling characteristics of a feedback amplifier were presented. From these expressions, it is apparent that significant improvements in performance are attainable through judicious selection of the excess bias voltages and partitioning of the bias currents. Although emphasis in this work is on the two-stage amplifier, the technique readily extends to other widely used structures including the folded cascode and the regulated cascode structures.

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Bibliography

[1] J.E. Solomon, "The monolithic op amp, A tutorial study", *IEEE J. Solid-State Circuits*, Vol. SC-9, pp. 314-332, Dec. 1974.

[2] P.R. Gray, R.G. Meyer, "MOS Operational Amplifier Design-A Tutorial Overview", *IEEE J. Solid-State Circuits*, Vol. SC-17, pp. 969-982, Dec. 1982.

[3] J. McCreary, "CMOS OP AMP Design - a tutorial", Lecture Notes from Course "Design of Bipolar and MOS Circuits", Stuttgart, Sept. 1983.

[4] P.E. Allen and D. R. Holberg,"CMOS Analog Circuit Design", Holt, Rinehart and Winston, New York, 1987.

[5] D.A. Johns and K. Martin, "Analog Integrated Circuit Design", Wiley, New York, 1997.

[6] K.R. Laker and W.M.C. Sansen, "Design of Analog Integrated Circuits and Systems", McGraw Hill, New York, 1994.

[7] K. Bult, and G. J. G. M. Geelen, "A Fast-Settling CMOS Op Amp for SC Circuits with 90-dB DC Gain," *IEEE J. Solid-State Circuits*, Vol. 25, No. 6, pp. 1379-1384, 1990.

[8] B. Y. Kamath, R. G. Meyer, and P. R. Gray, "Relationship Between Frequency Response and Settling Time of Operational Amplifiers," *IEEE J. Solid-State Circuits*, Vol. SC-9, No. 6, pp. 347-352, Dec. 1974.

[9] Y. Chen, M. E. Schlarmann, and R. L. Geiger, "An Improved Design Formulation Suitable for Optimization of Operational Amplifiers," *To appear in Proc. IEEE 1999 MWSCAS (Las Cruces, NM)*