

# An Improved Design Formulation for Design and Optimization of Operational Amplifiers\*

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**Abstract**-An alternative approach to designing operational amplifiers is presented that focuses on identifying a minimal design parameter space that emphasizes relevant design parameters rather than natural design parameters. It is shown that considerable simplification of some of the key performance parameters can be obtained with an alternative design parameter space while still maintaining the same mathematical models for the amplifier. This simplification provides additional insight into the operation of the amplifier and makes performance optimization more manageable. Design examples are presented which demonstrate how the simplified parameter equations can be utilized to efficiently design amplifiers that satisfy certain performance specifications.

## I. INTRODUCTION

The two-stage amplifier shown in Fig. 1 is one of the most basic of the operational amplifier structures. This structure has received considerable attention in the literature [1-3] as well as in textbooks focusing on linear circuit design [4-6]. Some have attempted to formalize a systematic design strategy for this structure including [5,6], but the differences in approach are substantial resulting in significantly different implementations exhibiting substantially different performance parameters with neither approach developed for optimal performance.

In this paper we will focus on formalizing the design problem in such a way that the designer will have added insight into the operation of an amplifier so as to generate more optimal designs. Although emphasis will be on the two-stage amplifier, the technique readily extends to other widely used structures including the folded cascode, the regulated cascode and the gain-boosted cascode structures. This formalization will be based upon identifying both the performance requirements and the degrees of freedom that constrain a given design problem.

It will be shown that the most natural design parameters and particularly those usually considered in the literature create complicated mathematical expressions for some of the most critical performance parameters making performance optimization difficult. An alternative to the natural design parameter space which includes a minimal set of design parameters will be introduced that simplifies the fundamental design equations to the point that performance optimization becomes viable.

## II. PROBLEM FORMULATION

The two-stage operational amplifier with capacitive load of Fig. 1 is comprised of 7 transistors, a load capacitor  $C_L$ , a

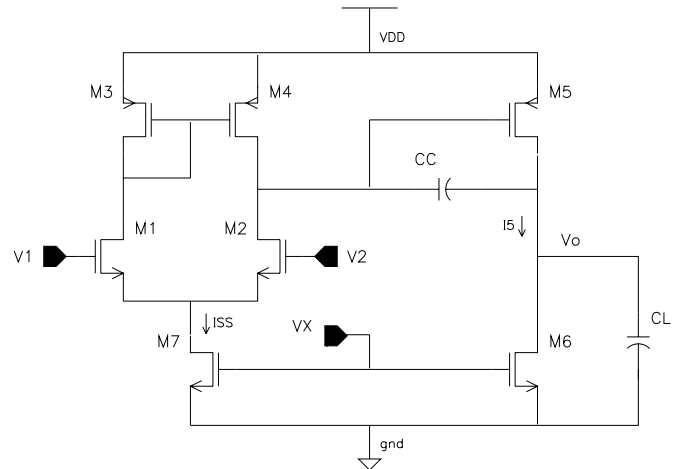


Fig. 1. Basic two stage operational amplifier

compensation capacitor  $C_C$ , a bias voltage  $V_x$ , and a power supply  $V_{DD}$ . Transistors M1 and M2 are generally matched as are transistors M3 and M4. If the load capacitor and supply voltage  $V_{DD}$  are assumed specified, there are 12 degrees of freedom available to the designer, specifically determined by the design parameters  $W_1, L_1, W_3, L_3, W_5, L_5, W_6, L_6, W_7, L_7, I_{SS}$ , and  $C_C$ . We will define the natural design parameter space for the operational amplifier of Fig. 1 to be the design parameter set listed above, specifically

$$S_{\text{NATURAL}} = \{W_1, L_1, W_3, L_3, W_5, L_5, W_6, L_6, W_7, L_7, I_{SS}, C_C\}$$

Table 1 lists some of the important performance parameters commonly used to characterize the performance of an operational amplifier. In most of the parameters, the dimensional design parameters appear only as width/length ratios thus reducing the number of degrees of freedom by five from 12 to 7. This observation leads to a second reduced set of natural design parameters

$$S_{\text{NATURAL-REDUCED}} = \{(W/L)_1, (W/L)_3, (W/L)_5, (W/L)_6, (W/L)_7, I_{SS}, C_C\}$$

where  $(W/L)_k = W_k/L_k$ . With the large number of performance parameters and the small number of design parameters, the designer must make tradeoffs during the design process. In addition to a set of performance parameters that often create a highly over constrained design requirement, the relationship between the performance parameters and the natural design parameters of  $S_{\text{NATURAL}}$  is highly nonlinear.

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TABLE I  
COMMON PERFORMANCE PARAMETERS OF OPERATIONAL  
AMPLIFIERS

Parameter	Description
A <sub>o</sub>	Open-loop DC Gain
GB	Gain-Bandwidth Product
φ <sub>m</sub> (or Q)	Phase Margin (or pole Q)
SR	Slew Rate
T <sub>SETTLE</sub>	Settling Time
A <sub>T</sub>	Total Area
A <sub>A</sub>	Total Active Area
P	Power Dissipation
σ <sub>VOS</sub>	Standard Deviation of Input Referred Offset Voltage (often termed the input offset voltage)
CMRR	Common Mode Rejection Ratio
PSRR	Power Supply Rejection Ratio
V <sub>imax</sub>	Maximum Common Mode Input Voltage
V <sub>imin</sub>	Minimum Common Mode Output Voltage
V <sub>omax</sub>	Maximum Output Voltage Swing
V <sub>omin</sub>	Minimum Output Voltage Swing
V <sub>noise</sub>	Input Referred RMS Noise Voltage
S <sub>v</sub>	Input Referred Noise Spectral Density

### III. DESIGN EQUATIONS

Central to the design of any operational amplifier is managing the compensation of the amplifier so that with the desired feedback the amplifier maintains an acceptable phase margin. The small signal model of the operational amplifier of Fig. 1 is shown in Fig. 2. In this small-signal model, the gate-drain overlap capacitances have been neglected as have the capacitances on the common source node of M1 and M2 and the diffusion capacitances on the node connected to the drain of M1.

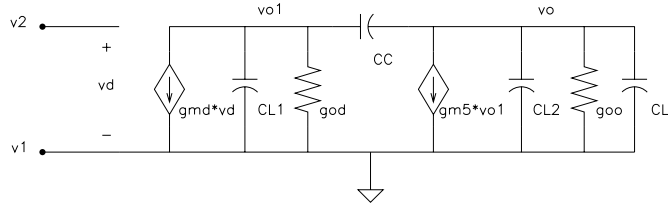


Fig. 2. Small signal model of the two-stage operational amplifier

A standard analysis of this circuit yields the gain expression

$$A(s) = \frac{g_{md}(g_{m5} - sC_C)}{s^2 C_C C_L + s g_{m5} C_C + g_{oo} g_{od}} \quad (1)$$

where

$$g_{md} = g_{m1} = g_{m2} \quad (2)$$

$$g_{od} = g_{o2} + g_{o4} \quad (3)$$

$$g_{oo} = g_{o5} + g_{o6} \quad (4)$$

$g_{mi}$  and  $g_{oi}$  respectively are the small signal transconductance and output conductance of transistor  $M_i$ . Here assuming  $C_C$

and  $C_L$  are large compared to the parasitic capacitances and the transconductance gains are large compared to the output conductances. The DC gain of the amplifier is given by

$$A_O \cong \frac{g_{md} g_{m5}}{g_{oo} g_{od}} \quad (5)$$

The gain bandwidth product is given by

$$GB \cong \frac{g_{md}}{C_C} \quad (6)$$

If feedback is applied, and assuming that the transconductances are much larger than the channel conductances, the closed-loop voltage gain of the noninverting amplifier is given by the expression

$$A_{FB}(s) \cong \frac{\frac{g_{md} g_{m5}}{C_C C_L} \left(1 - s \frac{C_C}{g_{m5}}\right)}{s^2 + s \left(\frac{g_{m5} - \beta g_{md}}{C_L}\right) + \frac{g_{md} g_{m5} \beta}{C_C C_L}} \quad (7)$$

where  $\beta$  is the gain of the feedback network. Although the phase margin is commonly used for compensating an amplifier, the pole Q of the feedback amplifier may be more useful. It follows from (7) that the pole Q of the feedback amplifier is given by the expression

$$Q = \sqrt{\frac{C_L}{C_C}} \sqrt{\beta} \frac{\sqrt{g_{m5} g_{md}}}{(g_{m5} - \beta g_{md})} \quad (8)$$

Rewriting (8) in terms of  $C_C$ , we obtain the design equation

$$C_C = \frac{C_L \beta}{Q^2} \frac{g_{m5} g_{md}}{(g_{m5} - \beta g_{md})^2} \quad (9)$$

The slew rate of the amplifier is commonly approximated by the expression

$$SR \cong \frac{I_{SS}}{C_C} \quad (10)$$

where  $I_{SS}$  is the quiescent tail current driving the input differential pair.

The input common mode input range and the output signal swing are defined respectively by the equations

$$V_{i\max} = V_{DD} + V_{GS3Q} + V_{T1} \quad (11)$$

$$V_{i\min} = V_{GS1Q} + V_{GS7Q} - V_{T7} \quad (12)$$

$$V_{o\max} = V_{DD} + V_{GS5Q} + V_{T5} \quad (13)$$

$$V_{o\min} = V_{GS6Q} - V_{T6} \quad (14)$$

The performance parameters given in (5) through (14) are expressed in terms of an alternate but much larger parameter set

$$S_{\text{ALTERNATE}} = \{g_{oo}, g_{od}, g_{m5}, C_C, V_{GS1Q}, V_{GS3Q}, V_{GS5Q}, V_{GS6Q}, V_{GS7Q}, I_{SS}, g_{o2}, g_{o4}, g_{o5}, g_{o6}\}$$

The difficulty of using this parameter set is associated both with its large size and the inherent relationship that exists between groups of parameters in the set.

#### IV ALTERNATE FORMULATION OF THE DESIGN PROBLEM

The purpose of an alternate characterization is to generate a new design space which will simplify the expressions for the key performance parameters sufficiently to give the designer added insight into both how the amplifier operates and how tradeoffs can be made between the design parameters to optimize amplifier performance. This alternate parameterization must be in terms of a set of independent parameters and should provide for a straightforward mapping to the natural design parameters of  $S_{\text{NATURAL}}$ .

The first step in this formulation will be to transfer the power dissipation from the performance parameter category to the design parameter category. The focus on power as a design parameter is made because power is actually the most important design parameter in many designs and because of the vital role power plays in many of the key performance parameters. The compensation capacitor is transferred to the performance parameter category since it will not be used as a design parameter. With these changes, we propose the alternate design parameter space comprised of

$$S_{\text{ALT}} = \{P, \theta, V_{\text{EB1}}, V_{\text{EB3}}, V_{\text{EB5}}, V_{\text{EB6}}, n_1, n_3, n_5, n_6, n_7\}$$

where  $P$  is the total power dissipation,  $\theta$  is the ratio of the magnitude of the quiescent current in M5 to the tail current  $I_{\text{SS}}$ ,  $V_{\text{EB}k}$  is the excess bias voltage for the  $k$ 'th transistor defined by  $V_{\text{EB}k} = V_{\text{GSQ}k} - V_{\text{TK}}$  and  $n_k$  is the minimum feature scaling factor defined as the ratio between the length (or width if  $L > W$ ) of a minimum sized transistor with a given  $W/L$  specification and the length of the device actually used. It can be shown that these form an independent parameter space that completely characterizes the performance of the amplifier. Further, most performance parameters of interest are not dependent upon the last five parameters in  $S_{\text{ALT}}$  and most are dependent only on  $P$ ,  $\theta$ ,  $V_{\text{EB1}}$ , and  $V_{\text{EB5}}$ . The use of excess bias voltages of transistors as design parameters was selected, in part, because common mode input range and output signal swing are becoming increasingly important as power supply voltages decrease and these design parameters can be used to obtain very simple and explicit expressions for input and output signal swings. The inclusion of the parameter  $\theta$  was made because it reflects the split of power between the first and second stage of the amplifier.

The relationship between this alternate design parameter space and the natural design parameter space is readily obtained. For convenience, these are expressed here in terms of  $W/L$  ratios rather than in terms of  $W$  and  $L$  values.

$$I_{\text{SS}} \cong \frac{P}{V_{\text{DD}}(1+\theta)} \quad (15)$$

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 \cong \frac{P}{\mu_n C_{\text{OX}} V_{\text{DD}} V_{\text{EB1}}^2 (1+\theta)} \quad (16)$$

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 \cong \frac{P}{\mu_p C_{\text{OX}} V_{\text{DD}} V_{\text{EB3}}^2 (1+\theta)} \quad (17)$$

$$\left(\frac{W}{L}\right)_5 \cong \frac{2P\theta}{\mu_p C_{\text{OX}} V_{\text{DD}} V_{\text{EB5}}^2 (1+\theta)} \quad (18)$$

$$\left(\frac{W}{L}\right)_7 \cong \frac{2P}{\mu_n C_{\text{OX}} V_{\text{DD}} V_{\text{EB7}}^2 (1+\theta)} \quad (19)$$

$$\left(\frac{W}{L}\right)_6 \cong \theta \left(\frac{W}{L}\right)_7 \quad (20)$$

The values for  $W$  and  $L$  for each of the transistors are then obtained from the relationship

$$L_k = n_k L_{\text{min}}, W_k = L_k (W/L)_k \text{ for } (W/L)_k > 1 \quad (21)$$

and

$$W_k = n_k W_{\text{min}}, L_k = W_k / (W/L)_k \text{ for } (L/W)_k > 1 \quad (22)$$

Expressions for most of the key performance parameters in Table 1 in terms of the alternate parameter space follow. In these expressions, it is assumed that the value of the pole  $Q$  was set at  $(1/\sqrt{2})$  which is close to the value of  $Q$  needed for a 60-degree phase margin. This was achieved by invoking the constraint of (9) relating the pole  $Q$  to the value of the compensation capacitor.

$$A_o = \frac{4}{(\lambda_n + \lambda_p)^2 V_{\text{EB1}} |V_{\text{EB5}}|} \quad (23)$$

$$C_c = 4C_L \theta \beta \frac{V_{\text{EB1}} |V_{\text{EB5}}|}{(2\theta V_{\text{EB1}} - \beta |V_{\text{EB5}}|)^2} \quad (24)$$

$$GB = \frac{P}{V_{\text{DD}}(1+\theta)V_{\text{EB1}}C_c} = \frac{P(2\theta V_{\text{EB1}} - \beta |V_{\text{EB5}}|)^2}{4C_L \theta \beta V_{\text{DD}}(1+\theta)V_{\text{EB1}}^2 |V_{\text{EB5}}|} \quad (25)$$

$$SR = V_{\text{EB1}} GB = \frac{P(2\theta V_{\text{EB1}} - \beta |V_{\text{EB5}}|)^2}{4C_L \theta \beta V_{\text{DD}}(1+\theta)V_{\text{EB1}} |V_{\text{EB5}}|} \quad (26)$$

$$V_{i\text{max}} = V_{\text{DD}} + V_{\text{EB3}} + V_{\text{T1}} + V_{\text{T3}} \quad (27)$$

$$V_{i\text{min}} = V_{\text{EB1}} + V_{\text{EB7}} + V_{\text{T1}} \quad (28)$$

$$V_{o\text{max}} = V_{\text{DD}} + V_{\text{EB5}} \quad (29)$$

$$V_{o\text{min}} = V_{\text{EB6}} \quad (30)$$

Some observations about the closed-form parametric expressions expressed in terms of the independent design variables of  $S_{\text{ALT}}$  are justified. Consider, for example, the two different expressions for the DC gain  $A_o$  of (5) and (23). Equation (5) suggests that increasing the power by increasing  $I_{\text{SS}}$  will decrease the gain and that there are four  $W/L$  ratios that can be used to either decrease or increase the gain. In fact, 5 parameters from  $S_{\text{NATURAL\_REDUCED}}$  affect the gain  $A_o$ . Examination of (23), however, shows that the gain is completely determined by two parameters of  $S_{\text{ALT}}$ , specifically the excess bias voltages  $V_{\text{EB1}}$  and  $V_{\text{EB5}}$ , and that if these excess bias voltages are fixed, power plays no role in

the gain. Similar observations can be made with other performance parameters.

#### V DESIGN PROCEDURE

Depending upon the application, certain performance parameters are critical others are not. As a result, a one-size fits all design procedure is not possible. Rather, the design procedure has to be tailored to reflect the priorities of the specific application. Therefore, there are many possible design procedures that could be presented. In this section, an example will demonstrate how those expressions can be utilized to efficiently design amplifiers that satisfy certain performance specifications.

*Design Procedure: Satisfying  $A_O$ ,  $P$ ,  $GB$ , and common mode input and output range requirements:*

Assume the following performance parameters are given: Input and Output common mode ranges ( $V_{imin}$ ,  $V_{imax}$ ,  $V_{omin}$ ,  $V_{omax}$ ), DC gain ( $A_O$ ), power dissipation ( $P$ ) and gain bandwidth ( $GB$ ). Furthermore, assume the loading capacitance  $C_L$  is known.

1. Choose the smallest channel length by considering matching requirements.
2. Using (27), (29), and (30) and the specified input and output common mode ranges, determine the excess bias voltages,  $V_{EB3}$ ,  $V_{EB5}$ , and  $V_{EB6}$ .
3. Using (23) and the DC gain requirement, determine  $V_{EB1}$ .
4. Substitute  $V_{EB1}$  into (28) and use the minimum common mode input voltage to determine  $V_{EB7}$ .
5. Choose the current split factor  $\theta$  and substitute it and the power dissipation specification ( $P$ ) into (15) to determine the bias current  $I_{SS}$ .
6. Calculate the size of the compensation capacitor  $C_C$  using (24).
7. Check the  $GB$  specification. Adjust  $\theta$  if necessary.
8. Using the excess biases and the quiescent currents already determined, calculate all transistors' sizes.
9. Implement the structure, check phase margin and all performance parameters. Modification may be required to satisfy all specifications.

Numerical Example:

Given specifications:  $A_O \cong 66\text{dB}$ ,  $GB \cong 5\text{MHz}$ ,  $V_{omin} = 0.25\text{V}$ ,  $V_{omax} = 3.1\text{V}$ ,  $V_{imin} = 1.1\text{V}$ ,  $V_{imax} = 3\text{V}$ ,  $V_{DD} = 3.3\text{V}$ ,  $P = 0.17\text{mW}$ ,  $\beta = 1$ . Assume  $V_{Tn} = 0.6$ ,  $V_{Tp} = -0.7$ ,  $\lambda_n = 0.04$ ,  $\lambda_p = 0.18$ ,  $C_L = 1\text{pF}$

1. Choose  $L_{min} = 2\mu\text{m}$ ,  $n_5 = 1$ .
2.  $V_{EB3} = -0.2\text{V}$ ,  $V_{EB5} = -0.2\text{V}$ ,  $V_{EB6} = -0.25\text{V}$
3. Select  $V_{EB1} = 0.2\text{V}$
4. Calculate  $V_{EB7} = 0.3\text{V}$
5. Choose  $\theta = 1$ , so  $I_{SS} = 25.7\mu\text{A}$
6. Calculated  $C_C = 3.7\text{pF}$
7. Check  $GB = 5.38\text{MHz}$
8.  $(W/L)_{1,2} = 6.79$  select  $13/2$ ,  $(W/L)_{3,4} = 13.89$  select  $27.8/2$ ,  $(W/L)_5 = 27$  select  $54/2$ ,  $(W/L)_{6,7} = 8.7$  select  $17.4/2$ .
9. Implement the structure and check the phase margin and other relevant performance specifications. Modify as necessary.

The final design parameters are summarized in Table 2.

TABLE 2

CIRCUIT DESIGN AND PERFORMANCE PARAMETERS FOR EXAMPLE 1

$(W/L)_{1,2}$	13/2	$(W/L)_{3,4}$	24.5/2	$(W/L)_5$	54/2
$(W/L)_{6,7}$	17.4/2	$C_C$	3.7pF	$\phi_{\text{phase}}$	45.4deg.
$I_{SS}$	25uA	$I_5$	26.68uA	$\theta$	1.06
$GB$	5.2MHz	$P$	0.17mw	$V_{EB7}$	0.2

Note: parasitic gate-source capacitance of  $M_5$  was considered in calculating compensation capacitor  $C_C$ .

#### VI CONCLUSION

Using the traditional expressions for the performance parameters of an operational amplifier, performance optimization is difficult because the relationships among the parameters and the circuit's degrees of freedom are too complicated. The high level of complexity is due to the fact that the expressions are cast in a design space that is based on a set of natural or convenient design parameters.

This work demonstrates that if the performance parameter equations are expressed in an alternative design space that is based on relevant design parameters rather than the natural design parameters, that the expressions for some of the key performance parameters are significantly simplified. As a result, designers gain additional insight and the task of performance optimization becomes more manageable. Examples are presented which show how the simplified parameter equations can be utilized to design two stage amplifiers that satisfy certain performance specifications.

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