Gain Error Correction Scheme for Multiply-By-Two Gain Amplifier in Pipelined ADC

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Abstract - **A simple scheme for correcting the gain error of multiply-by-two gain amplifiers that are used in pipelined ADC's using analog technique is proposed. This scheme only requires a programmable capacitor array, a comparator, and a small amount of low speed digital circuitry, which can be shared between different pipelined stages. The resultant gain of two can have accuracy better than 15 bits for typical common-mode voltage error and amplifier and comparator offset voltages.**

I. Introduction

High speed and high accuracy analog-to-digital converters (ADC's) are in increasing demand due to emerging telecommunication systems. Pipelined ADC has the advantage of good speed, modest area and attractive power consumption over other ADC's such as successive approximation, sigma delta, flash, and serial converters. However, component mismatches limit the accuracy of pipelined ADC. A single stage in pipelined ADC consists of a comparator, a multiplied-by-two gain amplifier (×2), and a digital-to-analog converter (DAC). Gain error and offset in the ×2, comparator offset, and errors in the DAC output levels give rise to non-linearity in pipelined ADC. To achieve high accuracy performance, both analog [1 2 3] and digital [4 5] calibration techniques have been reported. Digital correction techniques require extra digital hardware, which dissipates considerable power and inject switching noise into the substrate. Analog calibration approaches such as capacitor mismatch correction approaches require additional clock cycles during normal operations, making the conversion slower. An analog self-calibrating method for pipelined ADC's is proposed here. Each component in the pipeline ADC that substantially contributes to non-linearity in the performance of the converter is calibrated individually. These components are the comparator, the ×2, and the DAC's. Parameters in these components that are calibrated are the input offset voltages of the comparator and the opamp, the gain of the ×2, and the DAC output levels. In this work, focus is given to gain error correction. A calibration scheme that produces a precision gain of two for the ×2 is proposed. The scheme requires a programmable capacitor array (PCA) for capacitor trimming, a comparator, and a small amount of digital circuitry, which can be shared by different pipelined stages. Analyses of the proposed scheme will be presented and discussed. Issues such as comparator and amplifier offsets, capacitor mismatches, and common-mode voltage of the reference voltage will be addressed. This scheme can be used to achieve a gain of two with an accuracy of more than 15 bits. The effects of both common mode input voltage and amplifier offset are of second order to the gain accuracy.

II. Gain Error Correction Scheme

An implementation of ×2 without the switches is shown in Figure 1. If the differential gain of the opamp is very large, the differential gain of the ×2 is only affected by the capacitor matching. A scheme is proposed to correct for the gain of the ×2 as follows. Basically, one or more of the capacitors in the ×2 are trimmed until a gain of two is achieved. Assume that perfect reference voltages $+V_{REF}$ and $-V_{REF}$ (with respect to ground) are available, a gain of two can be detected by inputting a single reference voltage, V_{REF} or $-V_{REF}$, to the ×2. The differential output of the ×2, which is equal to $2V_{REF}$ in the ideal case, is compared

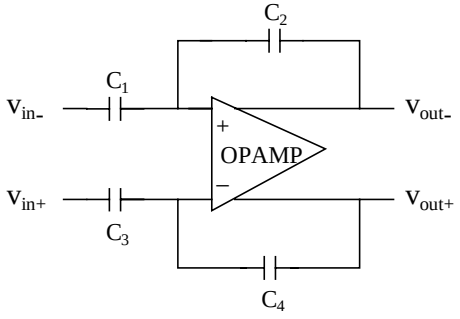

Fig. 1. Multiply-by-two gain amplifier.

to the difference of the reference voltages, which is also $2V_{REF}$ in the ideal case. However, perfect $+V_{REF}$ and $-V_{REF}$ are not usually available. The two actual reference voltages available can be defined as

$$V_{REF+} = V_{CM} + V_{REF} \quad (1)$$

$$V_{REF-} = V_{CM} - V_{REF} \quad (2)$$

where V_{CM} is the common-mode voltage of the reference voltages. Ideally, $V_{CM} = 0$. Trimming of the capacitor is performed first with V_{REF+} as the input voltage to the positive terminal of the ×2. The negative terminal of the ×2 is grounded. The capacitor is trimmed until the differential output of the ×2 reaches $(V_{REF+} - V_{REF-})$. The digital code of the PCA after this calibration is stored in a register. The same capacitor is again trimmed with V_{REF-} as the input voltage and the differential output voltage being compared to $(V_{REF-} - V_{REF+})$. The digital code of the PCA after this calibration is stored in a second register. In the following analysis, it is shown that by averaging the two values of the capacitor that are determined from the two calibrations, a very precise gain can be achieved.

The proposed scheme is shown in Figure 2 and the required clock signals are given in Figure 3. The operation of this scheme is as follows. During ϕ_1 and ϕ_2, V_{REF+} is input and the differential output is given by

$$v_{out+} - v_{out-} = A_d(V_{REF+} + V_{OS1}) \quad (3)$$

A_d is the differential gain and V_{OS1} is the offset voltage of the ×2. During ϕ_3, comparison is made between the differential output and $(V_{REF+} - V_{REF-})$. The differential voltage at the input of the comparator, v_x, is given by

$$v_x = (V_{REF+} - v_{out+}) - (V_{REF-} - v_{out-}) + V_{OS2} \quad (4)$$

where V_{OS2} is the offset voltage of the comparator. From Equations (3) and (4), it follows that

$$v_x = (V_{REF+} - V_{REF-}) + V_{OS2} - A_d(V_{REF+} + V_{OS1}) \quad (5)$$

In the ideal case where V_{CM}, V_{OS1}, and V_{OS2} are zero, $A_d = 2$, $V_{REF+} = \frac{1}{2}(V_{REF+} - V_{REF-})$, and $v_x = 0$. When V_{CM}, V_{OS1}, and V_{OS2} are non-zero and $A_d \neq 2$ due to component mismatch in the feedback capacitors of the ×2, v_x becomes non-zero. As mentioned above, the correction for the capacitor mismatches can be accomplished using PCA's. In this paper, the analysis is shown for the case where C_2 and C_4 are assumed to be PCA's, and gain adjustment is achieved by trimming these PCA's. At the beginning of a calibration, the following conditions are imposed: (1) The incrementer is set to zero and (2) the digital code of the PCA is set to zero, which corresponds to the maximum

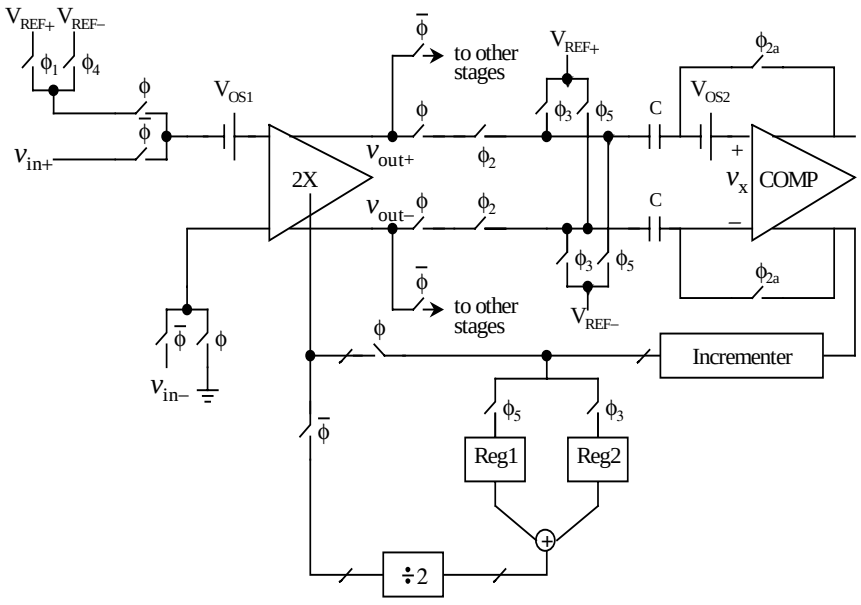

Fig. 2. Scheme for gain error correction.

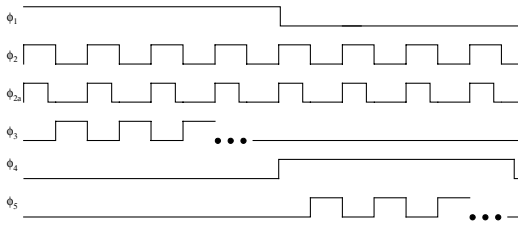

Fig. 3. Clock signals for gain error correction scheme.

capacitance given by the PCA. Under these conditions, the gain of the ×2 is less than two and $v_x > 0$. With $v_x > 0$, the incrementer increments by one level, turning off the corresponding switches in the PCA, trimming the capacitor and therefore, increasing the gain of the ×2. V_{REF+} is again sampled and compared to $V_{REF+} - V_{REF-}$. This process is repeated until $v_x = 0$, ideally. From Equation (5), the close-loop gain of the amplifier after this calibration step, $A_{d,1}$, is given by

$$A_{d,1} = \frac{2V_{REF} + V_{OS2}}{V_{REF} + V_{CM} + V_{OS1}} \tag{6}$$

The digital correction code for the PCA is stored in register 1 (Reg1 in Figure 1). After this, ×2 is calibrated again with V_{REF-} being the input voltage. Similarly, the close-loop gain of the amplifier for this calibration, $A_{d,2}$, can be obtained and is given by

$$A_{d,2} = \frac{-2V_{REF} + V_{OS2}}{-V_{REF} + V_{CM} + V_{OS1}} \tag{7}$$

From a practical viewpoint, one easy way to average the gains is to average to two digital codes of the PCA obtained from the above two calibration steps. Using this average as the digital code for the PCA, the gain of the amplifier can be expressed as

$$A_{d,ave} = \frac{2}{\frac{1}{A_{d,1}} + \frac{1}{A_{d,2}}} = \frac{4 - \frac{V_{OS2}^2}{V_{REF}^2}}{2 - \frac{V_{OS2}V_{CM}}{V_{REF}^2} - \frac{V_{OS1}V_{OS2}}{V_{REF}^2}} \tag{8}$$

It can be observed from the above equation that the effects introduced by V_{CM}, V_{OS1}, V_{OS2} are of second ordered ones. Assuming a typical value of 0.5% error in V_{CM}, V_{OS1}, and V_{OS2} with respect to V_{REF}, $A_{d,ave}$ is approximately 2±0.0000625 (15 bit accuracy). The challenge in this scheme falls on the design of the PCA, which is discussed below.

A precise expression for the gain in terms of the parameters of the operational amplifier is difficult to obtain due to mismatches between all the capacitors. The approximation given in Equation (8) is obtained assuming the amplifier is ideal and the capacitors in the positive and negative feedback path are matched. In this situation, the closed loop gain can be determined using the single-end version of the amplifier shown in Figure 1 and is given by $A_d = C_1/C_2$. Replacing C_2 by $(C_{2A} + C_{2B})/2$, the average gain expression of Equation (8) is obtained, where C_{2A} and C_{2B} are trimmed capacitor after the two calibrations. The validity of the above assumptions made to obtain the average gain expression in Equation (8) for the high-resolution end of the performance spectrum deserves attention. A SPICE simulation was undertaken using an inverting configuration with feedback resistors on a fully differential folded-cascode opamp designed in 1.2 μm CMOS process. With mismatches in all four resistors, the simulation results verify that the average differential gain can be obtained using the average values of the resistors as discussed.

III. PCA DESIGN

It can be shown that the required adjustment on a capacitor to produce a precision gain of two is dictated by V_{OS1}, V_{OS2}, V_{CM}, and Δ's (equations are not shown here). For ± 1V reference, $V_{CM} = -0.5\%V_{REF}$, $V_{OS1} = -0.5\%V_{REF}$, $V_{OS2} = x-0.5\%V_{REF}$ and Δ's = –0.5%, the PCA needs to be variable over a range of ±1.5%. It can be estimated from the following equation that 2^{11} levels in the PCA are required for 15-bit gain accuracy.

$$\left| \frac{C_1}{C_2} V_{REF} - 2V_{REF} \right| \le \frac{1}{2} V_{LSB} \tag{9}$$

The left hand side of the equality in Equation (9) represents the error in the output voltage of the amplifier due to capacitor mismatch and this has to be within ± 0.5 LSB of the ideal output voltage, $2V_{REF}$.

To acquire 2^{11} levels in the PCA, the PCA has to be designed in such a way that introducing a capacitor of reasonable magnitude to the array will result only in a small change in the overall capacitance (i.e., 0.003%). A design for such a PCA is proposed and shown in Figure 4. By connecting a relatively much smaller

capacitor compared to that of C in series, adding or removing an x_iC, y_iC or z_iC results in only a small change in the overall capacitance. The array is split into three smaller arrays to keep the ratio between the largest capacitor and the smallest capacitor small for better matching. The required range of capacitance is accomplished with the ratio of the largest capacitor to the smallest capacitor being 16.

IV. Conclusions

A scheme for correcting the gain error in switched capacitor ×2 has been proposed. Effects introduced by amplifier offset, comparator offset, and common mode voltage of the reference voltage are shown to be of second order to the gain accuracy. The analyses show that using this scheme, a gain of two with accuracy better than 15-bit level is achievable with amplifier and comparator offsets of 5mV, 0.5% capacitor mismatch, 0.5% error in the common-mode voltage, and a reference voltage of ±1 V. It was determined that under these conditions, a PCA having 2^{11} levels that is capable of varying over a range of 1.5% is required. A structure for such a PCA was also proposed. The ratio of the largest capacitor to the smallest capacitor required for the PCA is approximately 16.

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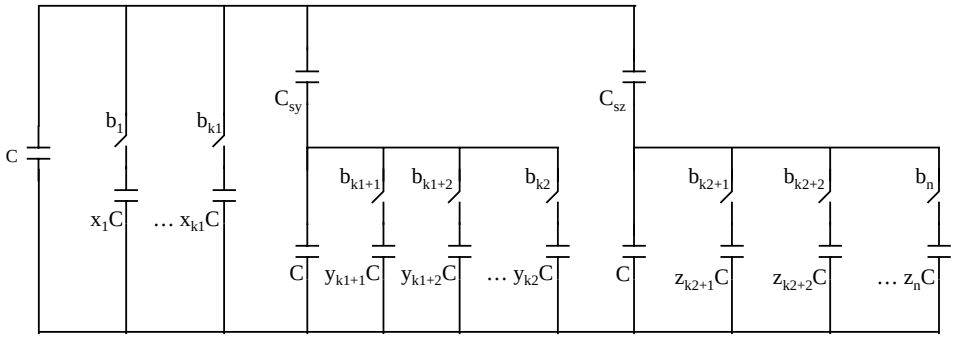

Fig. 4. Proposed capacitor array.