Gradient sensitivity reduction in current mirrors with non-rectangular layout structures

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Abstract- **A new current mirror structure using a non-rectangular dual-drain device with a shared channel to reduce the matching sensitivity to linear parameter gradients is introduced. The new structures are compared with conventional common centroid layouts for threshold voltage gradients at all angles across the active area of a mirror. Results show that in some applications, significant improvement in matching characteristics with the proposed non-rectangular structures over what is achievable with conventional layout techniques can be achieved.**

I. INTRODUCTION

Paralleling the increasing demand for cost-effective high-end mixed-signal systems is the need for improved matching performance in basic circuit blocks. Researchers have proposed models for predicting matching characteristics of closely-placed devices [1-3], but these models have been used almost exclusively to assess performance characteristics of circuits and layout techniques that have been well-known for over two decades.

It is generally agreed that the matching performance of closely placed devices is affected by both systematic and random variations in device characteristics. The traditional approach for managing the affects of random variations is to increase the area of the matching-critical devices to the level that the random mismatch effects are reduced to an acceptable level. Systematic effects are generally assumed to be represented by linear gradients in the matching-sensitive part of the circuit and common centroid layout techniques are generally used to minimize the effects of the linear gradients. The standard common centroid layout technique for a current mirror or a differential pair uses two cross-connected pairs of rectangular transistors. Felt et. al. [3] have recently reported that the effects of systematic variations are often comparable to the effects of random variations even with good layout techniques thus affirming the need for managing simultaneously the effects of both systematic and random variations.

An integral model, discussed in the following section, is widely used to model the effects of parameter gradients through the active area of a transistor. It can be easily shown with the integral model that the effects of linear parameter gradients occuring at any angle are eliminated with any common centroid layout technique, in apparent contradiction to the observations in [4]. Several new current mirror layout techniques were introduced [4] which offer a reduction in the effects of linear parameter gradients over what is attainable with conventional common centroid layout structures.

In this paper, the effects of parameter gradients on a class of current mirrors using nonrectangular structures in which the active channel region of the mirror is shared between the input and output of the device is explored. In contrast to existing mirror circuits in which the matching-sensitive part of the circuit is comprised of two source-coupled transistors, the nonrectangular structure discussed in this paper is a 4-terminal device that can be viewed as a dual-drain transistor. Although variations in threshold voltage (V_T), mobility (u), C_{OX}, and even some other parameters affect mirror matching, the dominant effects are generally threshold voltage variations. In this paper, only the effects of spatially dependent threshold voltage variations are considered. In particular, it is shown that the proposed nonrectangular mirror structure can be designed so that the mirror gain is significantly less sensitive to gradients in the threshold voltage than what is achievable with the widely used common centroid structures.
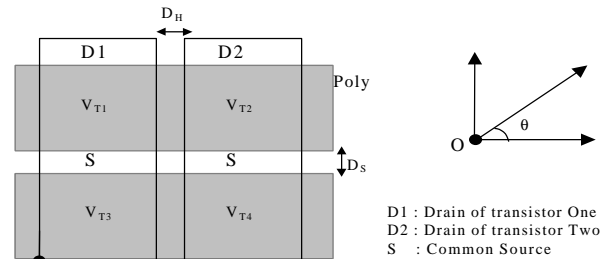

Figure 1. A Widely Used Common Centroid Layout Structure

II. MODELING OF PARAMETER GRADIENTS

In this section, the effects of threshold voltage gradients on the matching performance of current mirrors are investigated. The common centroid layout shown in Fig. 1 is widely used to help compensate for the effects of linear parameter gradients on current mirror matching. This layout generally offers better matching performance than other layout schemes such as simple or interdigitized structures.

The threshold voltage is commonly modeled as a distributed position-dependent parameter through the active devices, $V_T(x,y)$. The widely used approach for predicting the effects of threshold gradients on a transistor is based upon deriving an equivalent threshold voltage [1] for the devices as given by the following equation.

$$V_{Teq} = \frac{\int_{active\ area} V_T(x,y)\ dxdy}{Active\ Area} \qquad (1)$$

However, it has been observed that this simple integral model can significantly skew matching results. An alternative approach that gives better results for some layout structures is based upon the segmented integral model [4]. It will be used for the following mismatch analysis. In the segmented integral model, the V_T's of all individual unit transistors are calculated separately and the resultant lumped devices are then placed in parallel. For the Kth lumped component, the threshold voltage is given by

$$V_{Teq,K} = \frac{\int_{active\ area,K} V_T(x,y)\ dxdy}{Active\ Area,K} \qquad (2)$$

If the threshold voltage gradient is linear with amplitude α and the gradient direction is θ as indicated in Fig. 1, it follows that for the common centroid current mirror layout of Fig. 1:

$$V_{T1} = V_{TN} + \frac{\alpha W}{4}\cos\theta + \alpha(D_{V/S} + \frac{3L}{2})\sin\theta \qquad (3)$$

$$V_{T2} = V_{TN} + \alpha(D_H + \frac{3W}{4})\cos\theta + \alpha(D_{V/S} + \frac{3L}{2})\sin\theta$$

$$V_{T3} = V_{TN} + \frac{\alpha W}{4}\cos\theta + \frac{\alpha L}{2}\sin\theta$$

$$V_{T4} = V_{TN} + \alpha(D_H + \frac{3W}{4})\cos\theta + \frac{\alpha L}{2}\sin\theta$$

where D_H is the minimum separation, usually 4 lambda, between the two drain diffusions, D1 and D2, and D_S is the minimum required distance between the two channels. V_{T1}, V_{T2}, V_{T3} and V_{T4} are the resultant equivalent threshold voltages of the four transistors of equal sizes of (W/2)/L and V_{TN} is the threshold voltage at the base point O in Fig. 1. V_{T1} and V_{T4} correspond to the two unit transistors of "Transistor One" and V_{T2} and V_{T3} correspond to the two unit transistors of "Transistor Two".

The above equations were used to plot the mismatch for $0 \le \theta \le 360°$, $V_{TN}=0.7339V$, $\alpha=1mV/\mu m$, W=120μm, L=26μm, and $D_H=4\mu m$ as shown in Fig. 2 where mismatch is defined by,

$$Mismatch = \frac{I_{D2} - I_{D1}}{I_{D1}} x100\ \% \qquad (4)$$
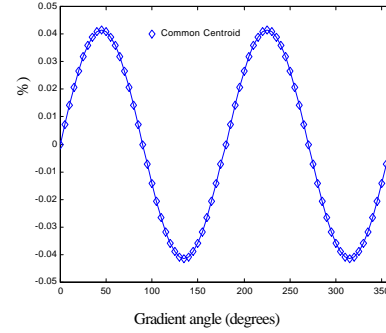

Figure 2 Matching Performance of Common Centroid Layout of Fig. 1 Versus Gradient Angle

The simulation results show, in contrast to the well-accepted premise that the effects of linear gradients can be readily modeled [5] and inherently canceled in common centroid structures [3]. The threshold gradients through the devices themselves create an angle-dependent mismatch even in common centroid structures. The common centroid layout of Fig. 1 exhibits maximum mismatch at gradient angles of $\theta = 45°$, 135°, 225° and 315°.
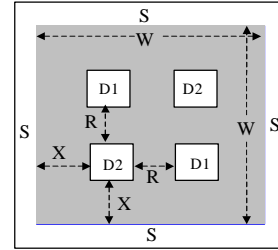

Figure 3. Waffle Layout Structure

III. NON-RECTANGULAR STRUCTURE

A non-rectangular layout of a current mirror is shown in Fig. 3. In this circuit, the polysilicon region (gray) and the two regions labeled D1 are connected together and serve as the input current node. The diffusion labeled S is thought of as the 'source' for the device and is connected to ground. The two regions labeled D2 are connected together and serve as the output current node. This is a special case of what is occasionally termed a "waffle transistor" and will be designated as a "waffle structure" throughout the remaining of this paper. The distinction between the waffle structure of Fig. 3 and the waffle transistor is significant. In a waffle transistor, the diffusion "islands" internal to the gate polysilicon are alternately source and drain connections. In the waffle layout of the current mirror of Fig. 3, there is no inherent two-transistor equivalent circuit but instead a distributed dual-drain device in which the source comprises

the perimeter of the polysilicon region and the dual drains are alternately connected islands internal to the gate polysilicon.

The active region is shared between the two drains in this layout. In what follows, it will not only be shown that this dual-drain device performs as a current mirror but that in the presence of parameter gradients, if properly designed, it can offer better matching performance than what is achievable with the standard common controid layout of Fig. 1. Without going into a rigorous definition of what constitutes a "common centroid" characteristic in a distributed dual-drain transistor, it can be shown that the waffle structure is also a common centroid layout.

Because the waffle mirror is not representable with two distinct source-connected transistors, standard modeling techniques cannot be applied to the structure. A special simulator [6] was developed for characterizing the structure and for predicting matching characteristics in the presence of either linear or non-linear gradients through the active channel region. It uses a finite lumped-element model approach. The simulator can also be used to predict the matching characteristics of an arbitrary layout of any size for arbitrary gradients in threshold voltage or any other process parameters and as such, can be used to overcome the errors inherent in both the integral model and the segmented integral model used to simulate the common centroid layout of Fig. 1.

IV. SIMULATION RESULTS

For the waffle structure of Fig. 3, the drain current and matching performance are affected by both the size and the positions of the drain contacts in the layout. The relationship between the drain current (with gate tied to D1 and D2 left open) and the positions of the drain contacts for the 2μm CMOS process available through MOSIS was evaluated using the simulator. Results are given in Figure 4. In this simulation, the total active area was kept fixed at 6144 μm^2 as was the size of the drain contacts which were 4μm x 4μm. It is observed that the drain current increases when the drain contacts approach to the edge of source.

The worst-direction matching characteristics of the waffle structure for a gradient of α=1mV/μm when used as a current mirror were simulated and are shown in Fig. 5 as a function of the total active area. In this simulation, the distance X was kept at 3/16W, R was 3/8W and the drain contacts were square with a side length of 1/8W. The worst-direction mismatch occurred at θ = 45°, 135°, 225° and 315° as was the case for the common centroid structure of Fig. 1.

It is well known that in current mirrors implemented with rectangular transistors, the standard deviation of the random mismatch decreases with the square root of the total active area. The effects of random mismatch for the waffle structure were simulated with a value of A_{VTO} of 5.3mV. μm.

The standard deviation of the mismatch expressed in percent is also shown in Fig. 5.
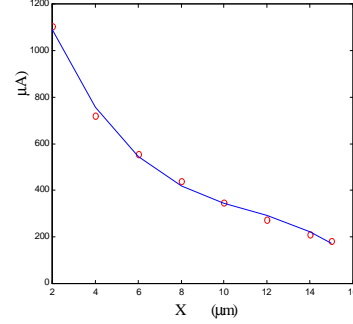

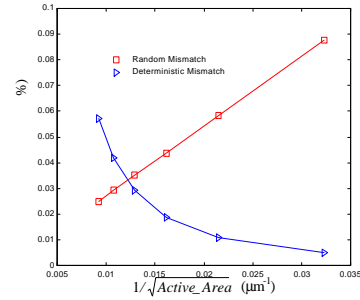Figure 4. Drain Currents with the Positions of Drain Contacts

Figure 5. Deterministic and Random Mismatches of Waffle Structure

The results show that the random mismatch is linearly proportional to $(1/\sqrt{Active\_Area})$ and the systematic mismatch is approximately inversely proportional to $(1/\sqrt{Active\_Area})$. Thus, tradeoffs must be made between increasing the active area to reduce random mismatch effects and decreasing the area to minimize worst-case gradient effects. These same tradeoffs must be made when using conventional layout structures [1].

The matching characteristics of the waffle structure will now be compared with those of the common centroid structure of Fig. 1. In order to make a fair comparison on the matching performance, the common centroid structures are designed to have the same active areas, the same nominal drain current and the same excess bias (V_{GSQ}-V_T) as the waffle structures. The comparison is made for a waffle structure that is 40μm x 40μm as a function of the parameter X in Fig. 3. The drain diffusions were fixed at 4μm x 4μm. Since changing the parameter X will result in a change in either current or excess bias voltage, we kept the excess bias fixed and allowed the current to vary (while keeping the current the same in both the waffle structure and the corresponding common centroid structure of Fig. 1). The comparison of the worst-direction matching performance is

shown in Fig. 6 for a gradient magnitude of α=1mV/μm. This figure shows that the waffle structure can offer significantly better matching performance than the common centroid structure in the presence of linear parameter gradients but also that the positioning of the drain diffusions is important. It is also observed that the matching performance of the waffle mirror structure for a fixed active area improves when the drain contacts are moved farther from the source contact.

Figure 7 shows the mismatch as a function of angle for a waffle structure with W=40μm, X=10μm and with 4μm drain diffusions as compared with that of the common centroid structure of Fig. 1. As before, the same active area, current and excess bias were used for both layouts.

From a practical viewpoint, it must be emphasized that the comparative results presented in Fig. 7 are obtained for a specific parameter gradient and a specific total active area. The relative performance of the two structures is strongly dependent upon both active area and the relative positioning of the drain diffusions in the waffle structure. Different parameter gradients and/or different relationships between the excess bias and the nominal drain current will affect where the crossover in performance between the common centroid layout of Fig. 1 and the waffle structure occurs.

The issue of optimality of the proposed waffle structure has not yet been determined. As is apparent from Fig. 3, even for a given active area, tradeoffs between the size and location of the drain diffusions can be made. Optimal structures should offer even better performance than that which was presented here.

V. CONCLUSION

A non-rectangular layout structure of a current mirror based upon a distributed-channel dual-drain device has been introduced. This structure can offer improved mirror matching in the presence of linear parameter gradients over what is attainable with the standard common centroid layout schemes in some applications. The performance crossover between a conventional common centroid layout and the new structure is dependent upon the magnitude of the parameter gradients, the bias current level and the excess bias voltage.
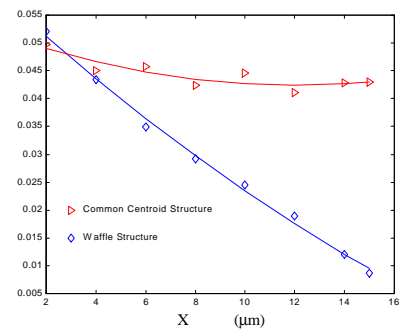
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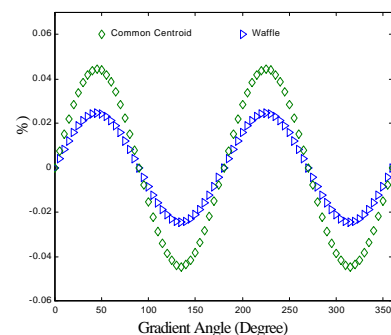Figure 6. Comparison of Waffle and Common Centroid Structure with a Fixed Active Area

Figure 7. Performance Comparison of Common Centroid and Waffle Structure

REFERENCES

[1] M. J. M. Pelgrom, A.C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors", IEEE J. Solid-State Circuits, vol. SC-24, pp. 1433-1439, 1989.
[2] K. R. Lakshmikumar, R. A. Hadaway, and M. A. Copeland, "Characterization and modeling of mismatch in MOS transistors for precision analog design," IEEE J. Solid-State Circuits, vol. SSC-21, pp. 1057-1066, 1986.
[3] E. Felt, et. al, "Measurement and Modeling of MOS Transistor Current Mismatch in Analog IC's", Proc. ACM, 1994, pp. 272-277.
[4] Mao-Feng Lan, Anilkumar Tammineedi, and R. L. Geiger, "A New Current Mirror Layout Technique for Improved Matching Characteristics," in Proc. MWSCAS, Las Cruces, New Mexico, Aug 8-11, 1999.
[5] A.J. Strojwas, et. al, "Manufacturability of Low Power CMOS Technology Solutions", Proc. IEEE Int. Symp. on Low Power Electronic Design, pp. 225-232, Monterey, August 1996.
[6] Mao-Feng Lan , Randall Geiger, "Matching Performance of Current Mirrors with Arbitrary Parameter Gradients Through the Active Devices", ISCAS, June 1998.