Simulation of Matching-Critical Circuits with Laterally Distributed Process and Device Parameters

Mao-Feng Lan and Randall Geiger
Department of Electrical and Computer Engineering
Iowa State University, Ames, IA 50011, U.S.A.
email : rlgeiger@iastate.edu

It is well recognized that the performance of many linear and mixed-signal integrated circuits is limited by the performance of matching critical circuit elements such as current mirrors and differential amplifiers. The impact of mismatch is of increasing concern as attempts are made to reduce supply voltages, decrease feature sizes, reduce power and increase the frequency of operation of the analog circuitry on a chip. The matching performance of basic circuit elements is attributable to both systematic and random variations in geometric parameters, process parameters and device parameters. Conventional wisdom suggests that random variations are easy to model and tradeoffs can be made between area and performance to compensate for random parameter variations. It is often more difficult to compensate for the systematic variations in parameters. The systematic variations often change from batch to batch, from wafer to wafer, and from die location to die location on a wafer. Based upon simple lumped parameter models which are amenable for inclusion in existing simulators such as SPICE, designers have developed simple rules of the thumb for sizing devices to manage the effects of random variations and layout strategies which invariably use segmentation and close placement of common-centroid structures for reducing or eliminating the effects of systematic parameter variations. Although this approach works well for non-demanding applications, the experimental performance and yield of high-end circuits is not in agreement with simulation results. The discrepancies are attributable to the inability to accurately model or simulate either random or systematic parameter variations in the channel region of the active devices. Iteration with device sizes and layout styles at the silicon level can improve performance but such an approach will not yield optimal designs and is both costly and time consuming.

The preferred route for optimizing the design and layout is based upon simulation. The seemingly simple problem of predicting the effects of systematic and random variations on a MOS transistor is becoming complicated by the unavailability of a suitable simulator. Existing models and simulators provide little insight into how to change either the size or layout to improve performance. The major reason existing simulators can not be used is that there is no mechanism for incorporating either systematic or random channel variations in lateral directions of device or process parameters and it is these lateral variations that play a key role in the performance of high-end matching-critical circuits.

We are developing a tool, MOSGRAD, that can be used to simulate the effects of distributed two-dimensional systematic and random variations in both process and device parameters on the performance of matching-critical circuits. This tool approximates the distributed channel region by a series of finite lumped-element cells. Each cell has four edge-centered nodes that can be connected to corresponding edge-centered nodes in adjacent cells. With this finite lumped-element approach, systematic variations in process or device parameters of any magnitude and at any angle relative to the cell can be readily simulated using a conventional SPICE-type simulator. Arbitrary systematic parameter variations and random parameter variations can also be accommodated. This tool has been used for predicting the effects of systematic and random parameter variations on the performance of current mirrors and offset voltages of differential amplifiers. It has also been used for predicting the performance of non-conventional circuit structures in which multiple drain and/or source regions share a common channel region and in predicting the performance of non-conventional layouts which may incorporate nonrectangular transistors or multiply-segmented transistors.

As a front end to the tool, a graphical users interface is incorporated in which the user graphically enters the circuit structure that is to be simulated. The output of the graphical interface is a lumped-element circuit that is passed to a conventional simulator. The tool has been successfully used to obtain layouts for current mirrors that offer significantly reduced sensitivity to linear gradients when compared to what is attainable with standard 2-segment common-centroid structures. It has also uncovered some fundamental limitations in the previously unquestioned relationship between the effects of random variations on circuit performance and gate area.