A High Frequency CMOS 4th Order digitally programmable Bandpass Filter

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Abstract—A high frequency fourth order CMOS continuous time Band-pass filter with programmable bandwidth and center frequency is presented in this paper. Simulations show That center frequency can be tuned from 141MHz to 603MHz for a 1.2pF capacitive load. This filter has been designed in TSMC 0.25u digital process with 2.5V power supply. The filter consumes around 105mW with a die area of 0.4 mm^2 and -32dB THD.

I. INTRODUCTION

With the rapid increase of the information transfer rates of many systems, the need for high frequency filters is, nowadays, a must. High-speed communication and storage systems need continuous-time filters with bandwidths variable over a wide range, while keeping the relative shape of the frequency response identical irrespective of the set bandwidth, and maintaining an adequate dynamic range. Typical system examples of such communication systems include magnetic storage (disc and tape drives), optical storage (CD-ROM drives) and high-speed local area networks (LAN) [1]. Moreover, high-frequency analog filters are used as preprocessing blocks in front of an ADC or as post processing blocks after a DAC [2].

The demand for system mobility, greater pacing densities, smaller size and low power requirements have driven the industry to use the low-cost digital CMOS process with supply voltages less than 3V [3]. This filter has been designed in TSMC 0.25u digital process that operates from 2.5V power supply.

Filter tunability is another major issue in the design of filters. Frequency tunability is important in order to maintain a stable response of the filter over process and temperature changes as well as selecting the frequency of operation where less noise exists. For this reason, the demand for programmable filters increased in a big way since the emergence of the disk-drive market [4].

For high frequency application, Gm-C based filters are commonly used [1][2]. Pavan [1] presented a 4th order Butterworth filter implemented in a 0.25u digital CMOS technology. The filter was tunable digitally over the range 65MHz to 350MHz. The filter consumes 70mW from a 3.3V power supply. In this paper, the architecture in [1] has been adopted but different functional

blocks were used. The filter is implemented in a 0.25u digital CMOS process with 2.5V power supply. The center frequency of this filter is digitally tunable over the range 141MHz to 603MHz and consumes 105mW with a die area of 0.4mm^2 and THD less than -32dB. The output swing of the filter is 400mV$_{pk\text{-}pk}$.

This paper is organized as follows. In section II, filter design is presented. Section III presents the simulation results. The conclusion of this paper will be in section IV.

II. FILTER DESIGN

In this section, the design of the filter and its components will be presented. The filter is a fourth order Butterworth filter with a maximum center frequency of 603MHz. The filter has been implemented in a 2.5V 0.25u digital TSMC CMOS process. The main components in the filter are the fully differential folded cascode OTA, common mode feed back ,CMFB, circuit, biasing current generator circuit, and sandwich capacitors. Each of these blocks will be described separately in the various subsections to follow.

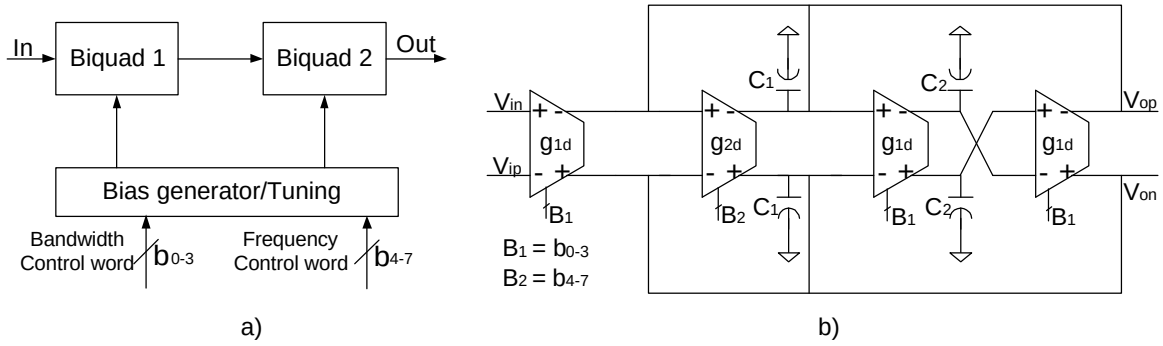

Figure 1 a) Fourth order filter. b) Implementation of Each biquad.

A. Filter Design

The fourth order filter is realized as a cascade of two biquadratic sections as shown Figure 1.a). Each biquad is a standard Gm-C biquad configuration based on the double integrator loop. The only difference between the two biquads is the values of the damping transconductor. The transconductors are digitally programmed by a four-bit word as shown in Figure 1.b). There are two digital words to program the filter; one is used to program the bandwidth and the second is used to program the center frequency of the filter according to the following relationships.

The transfer function of each biquad is:

$$\frac{Vod}{Vid} = \frac{g_{1d}\, sC_2}{s^2 C_1 C_2 + sC_2 g_{2d} + g_{1d}^2} = \frac{\frac{g_{1d}\, s}{C_1}}{s^2 + s\frac{g_{2d}}{C_1} + \frac{g_{1d}^2}{C_1 C_2}} \quad (1)$$

Where the center frequency is:

$$w_0 = \frac{g_{1d}}{\sqrt{C_1 C_2}} \quad (2)$$

And the bandwidth is:

$$BW = \frac{g_{2d}}{C_1} \quad (3)$$

According to equation (2), the center frequency can be tuned by programming g_{1d}, while the bandwidth can be tuned by programming g_{2d}. Each OTA is constructed from sub-OTAs comnnected in parallel, thus changing the values of $g_{1d,}$ and g_{2d} can be done by turning the sub-OTAs ON and OFF using he digital control word as will be described later.

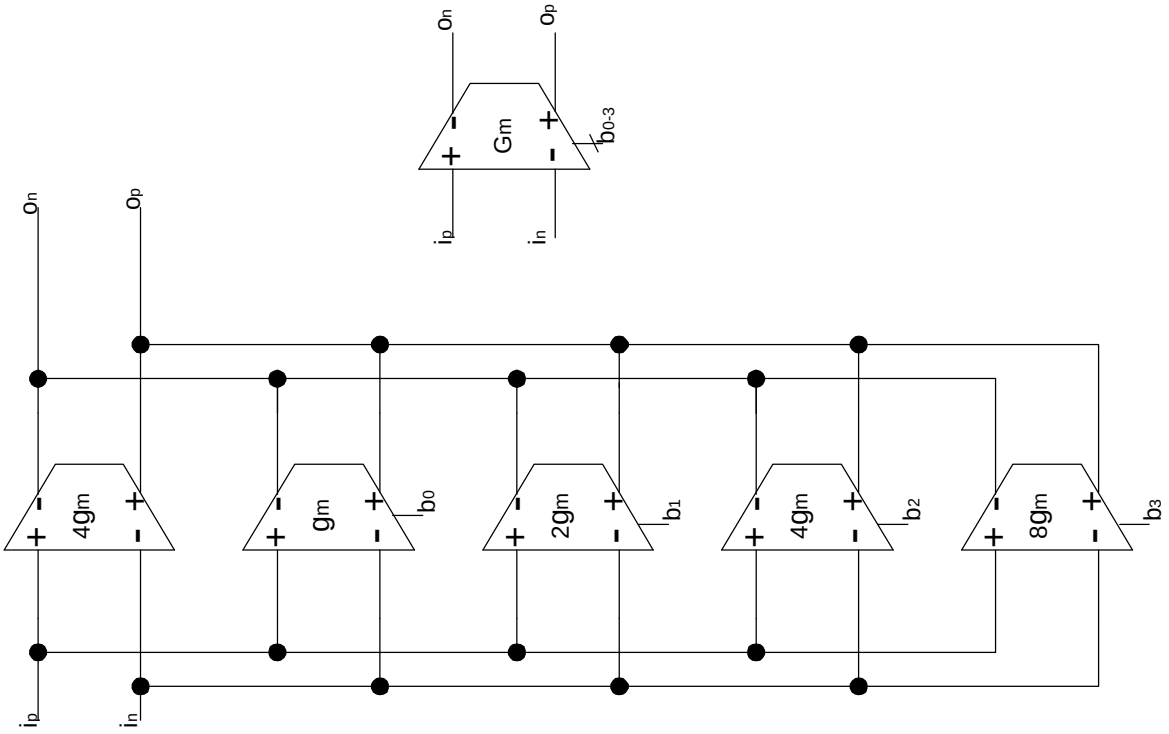

Figure 2 Programmable Gm.

B. OTA design

To allow for programmability of the effective G_m of the filter OTAs, each OTA consists of sub-OTA circuits; G_m, $2G_m$, $4G_m$ and $8G_m$ that are connected in parallel as shown in Figure 2. Based on the control word, the OTA can be configured as $4g_m$ when the control word is 0000, $5g_m$ when the control word is 0001, $6g_m$ when the control word is 0010, …, and $19g_m$ when the control word is 1111. The sub-Operational Transconductance Amplifier (OTA) schematic is shown Figure 3, where a fully differential folded cascoded architecture was chosen for the implementation of each OTA.

The main draw back of using fully differential OTA is the need of a common mode feed back (CMFB) circuit, since the CMFB circuit must be a high-speed circuit such that it won't slow down the operation of the OTA. The CMFB circuit speed performance should be comparable to the unity gain frequency of the differential path. The CMFB circuit is shown in Figure 3 [5]. Dummy devices were added in parallel with every sub-OTA input differential pair such that approximatly constant capacitance is achieved when some of the transconductors are switched ON or OFF. The dummy devices are switched ON when its transconductor is turned OFF and switched OFF when its transconductor is turned ON. The switching of the transcoductors is accomplished by controlling the gates of the tail currents using transistor switchs.

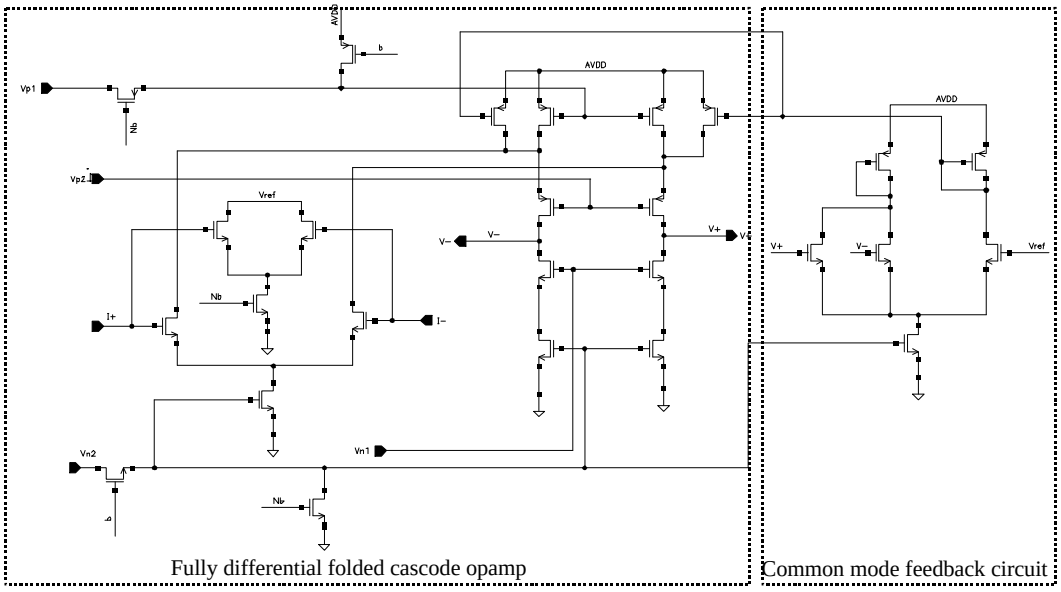

Figure 3 Fully differential folded cascode with CMFB circuit.

III. SIMULATION RESULTS

The fourth order filter has been simulated and layedout. It is dracula clean. Unfortunately, we don't have an extraction tool to extract the layout in order to be able to run post layout simulation. This might be the next step in the future work. However parasitics have been included in simulations mentioned in this work.

The simulation has been carried out for different cases in order to investigate the performance of the circuit under different conditions. The three design corners have been simulated and the results are summarized in

Table 1. Figures showing some simulation results are presented at the end of this paper.

The AC response of the filter is plotted, while changing the control word. It shows that the center frequency of the filter under nominal conditions can be varied from 141MHz up to 600MHz as the control word is changed from 0000 to 1111. The bandwidth can also be tuned around the center frequency. For example, when the filter is running at 603MHz, the bandwidth of the filter can be tuned from 17MHz to 119MHz.

AC analysis has been also carried out for the OTA when it is configured as $4g_m$ and when it is configured as $19g_m$ with a load of 0.5pF. For the $4g_m$ OTA, the unity gain frequency is 211MHz with phase margin of 84^o, while the unity gain frequency is 907MHz with a phase margin of 68^o for the $19g_m$ OTA. Capacitance of 0.5pF has been selected because it is the largest load capacitance that a single OTA can see.

Transient simulations show that the THD of the filter is slightly less than -32dB for the maximum output range of 400mV, center frequency of 603MHz, and BW of 17MHz.

The power consumption of the filter is around 105mW, and it is fairly constant under different corners. Different corners include changing the temperature to 100 C^o with slow NMOS and PMOS devices, SS models, temperature of -40 C^o with fast devices, FF models, and 25 C^o with typical devices, TT models. Power supply considered here is 2.5V one. The reason for choosing 2.5V as a power supply for all the corners is because we believe that for such low voltage applications, the customer will guarantee that the power supply is fairly constant over different conditions. However simulations with power supply of 2.3V to 2.7V are also considered.

Table 1 Summary of simulation results.

Center Frequency range	141MHz-603MHz
Bandwidth range at 603MHz	17MHz – 119MHz
Output swing	400mV pk-pk
Power Dissipation(mW)	105mWatt
THD	-32.6dB

Table 2 Circuit characteristic under different conditions.

	TT	SS	FF
Power Dissipation(mW)	105	104	108
Frequency Range(MHz)	141-603	120-512	204-891

IV. CONCLUSION

In this work we implemented a digitally programmable high frequency fourth order Butter worth bandpass filter. Simulation under typical conditions shows that this filter has a programmable center frequency in the range of 141MHz-603MHz. The bandwidth of the filter is also digitally programmable in order to overcome process and temperature variations from our nominal conditions.

This filter has been designed in TSMC 0.25u CMOS. Today, TSMC 0.18u CMOS is readily available and the design can be transformed to the new technology. Future work will iclude two steps: First, the design can be modified to be scalable by using the gate capacitance of the transistors as C_1 and C_2. The next step will be the actual implementation of the filter in the new process.

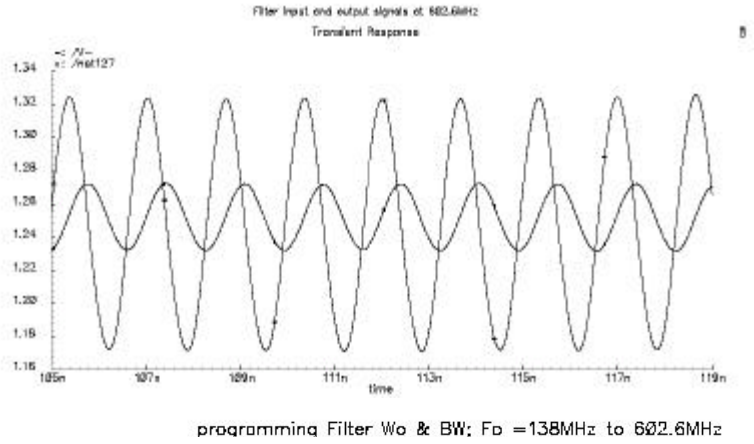

Figure 4.a filter input and output waveforms

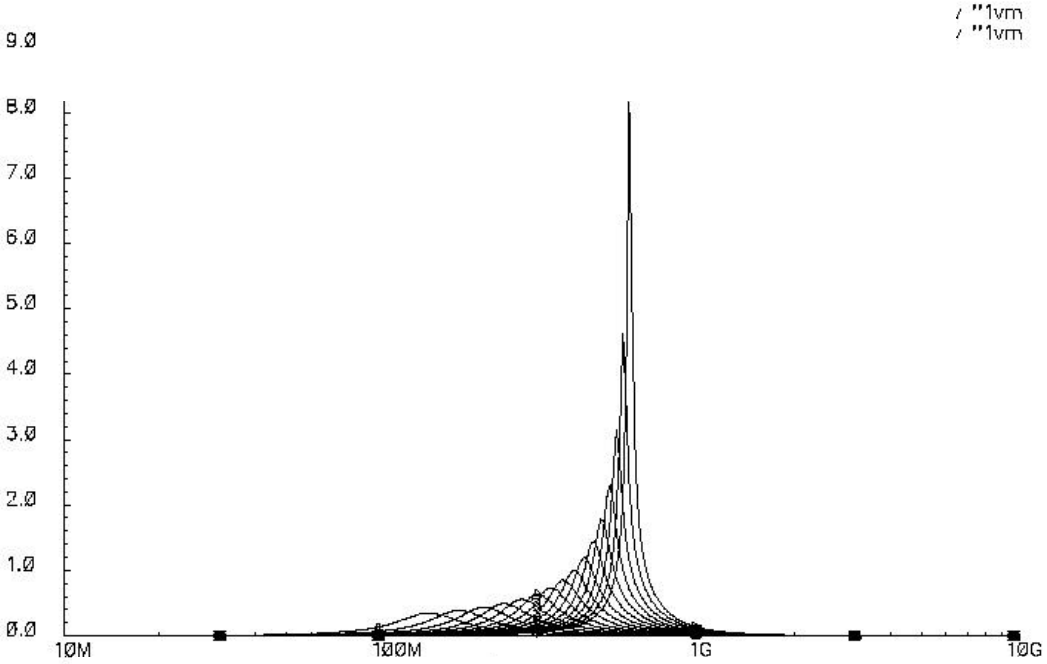

Figure 4.b Tuninng Filter center frequency

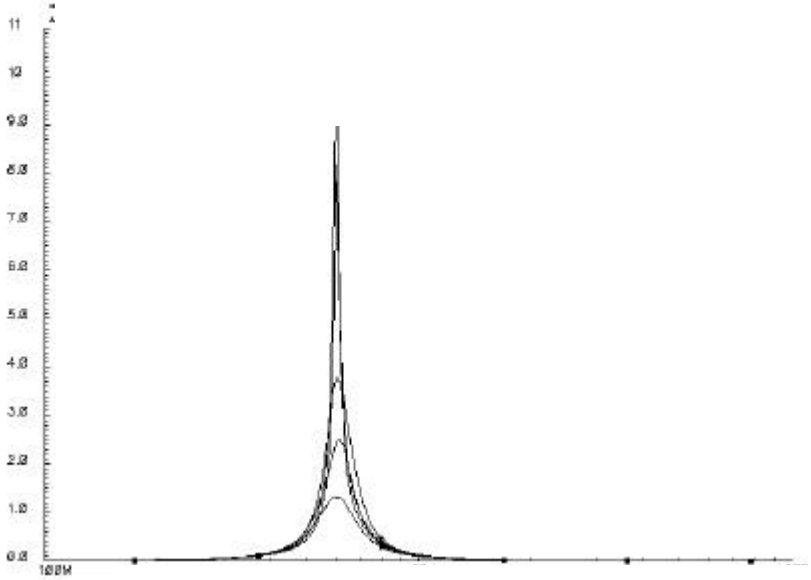

Figure 4.c Programming filter BW at Fo=603MHz

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