MAXIMIZING THE OSCILLATION FREQUENCY OF CMOS VCOS*

Huiting Chen, Randall Geiger

Department of Electrical & Computer Engineering
Iowa State University
Ames, IA50011, USA

Abstract-Techniques for enhancing the operation frequency range for voltage controlled ring oscillators are discussed. It is shown that substantial improvement in speed is achievable with concentric layout techniques and with transconductance density optimization. Simulation results for a VCO designed in a 0.35μm CMOS process are presented which show a center frequency of 4.5 GHz and a tuning range of ±12%.

I. INTRODUCTION

In recent years, there has been a growing interest in very high speed communication circuits. The design of monolithic VCOs in standard CMOS processes has been the subject of several research efforts. Voltage controlled ring oscillators have relative good jitter performance and are widely used in the high speed communication circuits. This paper focuses on the design of very high speed voltage controlled ring oscillators. Using these design techniques, a VCO with a 4.4 GHz operation frequency in a 0.35μm CMOS process is discussed.

In Section 2, the model that describes the delay stage is developed. In Section 3, techniques increasing the oscillator's frequency are discussed. In Section 4, simulation results are presented.

II. VCO DESIGN THEORY

One common structure for the delay cell of a ring oscillator is shown in Fig. 1. In this structure, the delay of the cell is a function of the transconductance per unit capacitance of the input transistors and the active loads.

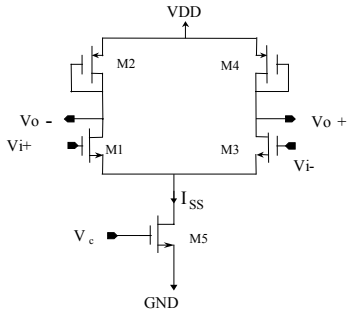

Fig. 1. Delay cell of the ring oscillator

If we can keep the VCO output voltage swing small, the VCO frequency can be obtained by using a small signal model. Fig. 2 is the simplified small signal model of the delay cell.

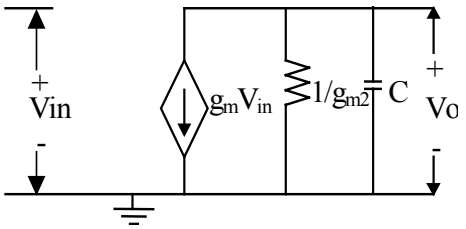

Fig. 2. The small signal model of VCO delay cell

where g_{m1} and g_{m2} are the transconductance of the input transistor and the load transistor, respectively, and C is the total capacitance seen by the output node. The capacitance C is the sum of the diffusion capacitance on the drain of M1, M2, the load capacitance $C_{L,}$ and the gate capacitance of the next stage which is essentially $C_{ox}W_1L_1$ where W_1 and L_1 are the width and length of M_1.

The transfer function of the delay stage, assuming loading by an identical stage is:

$$A(s) = \frac{Vo}{Vi} = \frac{-g_{m1}}{sC + g_{m2}} \tag{1}$$

Since ideally every stage has the same transfer function described by (1), the characteristic polynomial of the closed loop of an n stage VCO is

$$D(s) = (s + g_{m2}/C)^n + (-g_{m1}/C)^n \tag{2}$$

from (2) it follows that the pole locations are:

$$p = (-1)^{\frac{1}{n}} * \frac{g_{m1}}{C} - \frac{g_{m2}}{C}$$

$$= \pm cos(\pi/n) * \frac{g_{m1}}{C} - \frac{g_{m2}}{C} \pm j * sin(\pi/n) * \frac{g_{m1}}{C}$$

$$= \alpha + j * \beta \tag{3}$$

where α is the damping factor of the loop and β is the natural frequency of the loop.

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At the onset of oscillation, at least one pair of poles must be located in the right half plane (RHP). The poles move towards the left half plane (LHP) as the loss increases. It can be shown that the output waveform is a pure sinusoid when right-most pair of poles is located on the jω axis. In this structure, the damp factor of the loop α, becomes zero, from (3) it follows that

$$\cos(\pi/n)*\frac{g_{m1}}{C}=\frac{g_{m2}}{C} \tag{4}$$

To sustain oscillation, the pole must be kept in the right half plane (RHP), i.e., α is greater than zero. Thus the oscillation criteria is:

$$\cos(\pi/n)*\frac{g_{m1}}{C}>\frac{g_{m2}}{C} \tag{5}$$

Fig. 3 shows the pole locations of the VCO under the condition that g_{m2} is established to maintain the damping factor of the right-most pole pair at zero. Under this condition the oscillation frequency of the VCO is

$$\omega=\beta=\sin(\pi/n)*\frac{g_{m1}}{C} \tag{6}$$

Substituting (4) into (6), the frequency of the VCO can alternately be written as

$$\omega=\cot an(\pi/n)*\frac{g_{m21}}{C} \tag{7}$$

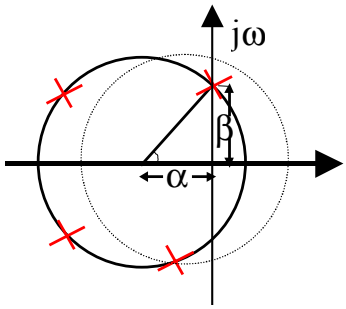

Fig. 3. The pole location of a 4-stage VCO.

In the structure of Fig. 1, g_{m1} is the transconductance of the input transistor M1. g_{m1} is proportional to the square root of the bias current of the input transistor. g_{m2} is the transconductance of the load transistor. Actually it is the impedance seen by the output node. g_{m2} is proportional to the square root of the bias current of the load transistor.

From (6) and (7), the strategy for the design of a high speed VCO is apparent. These can be summarized:

a. Minimize the total capacitance seen by the output node.
b. Maximize the transconductance per unit capacitance (gm/c) for the input transistors and load transistors.
c. Minimize the stage number n.

III. High Speed VCO Design Techniques

Most existing strategies for design of VCOs have been directed at applications where the frequency of oscillation is well below the f_t of a process. At higher frequencies, some luxuries afforded the designer tend to limit the oscillation frequency potential of a process. In this section, we will focus on the impact of layout, load selection and stage gain on high frequency operation.

A. Layout techniques for frequency enhancing

The total capacitance seen at the output node and the transconductance per unit capacitance are dependent upon both the process parameters of a given process and the layout of the delay stage. Although layout is not critical for low speed oscillations, it plays an important role in the design of VCOs that are designed to operate at frequencies that approach the f_t of a process. In this subsection, the effect of layout on the frequencies of operation is discussed.

From (6) and (7), it is apparent that one efficient way to increase the VCO frequency is to minimize the capacitance seen by the output node. This will be minimized when only parasitic and required loading capacitance of the following stage are included. The size of this capacitance is highly layout dependent.

Consider the conventional layout structure shown in Fig. 4. Following the design rule in a typical CMOS process, the minimum diffusion area of the source and the drain are:

$$A = \text{Drain Area} = \text{Source Area} = W*(5\lambda) \tag{8}$$

where λ is a scale factor associated with the process that is typically half of the minimum allowable drawn gate length and W is the drawn width of the transistor. Correspondingly, the drain periphery and source periphery are given by

$$P=(W+5\lambda)*2 \tag{9}$$

In the submicron process, the diffusion capacitance typically dominants the total node capacitance C. Thus minimizing the drain or source area will help to increase the VCO frequency.

For the conventional layout of Fig. 4, it follows that the total capacitance C seen on the output node is given by

$$C=C_{ox}W_1L_1+C_{sw}(P_1+P2)+C_{BOT}(A_{D1}+A_{D2}) \tag{10}$$

where C_{ox} is the gate oxide capacitance density, W_1 and L_1 define the channel geometry of M_1, P_1 and P_2 are the periphery of the drains of M_1 and M_2 respectively, A_{D1} and A_{D2} are the drain areas, and where C_{SW} and C_{BOT} are the sidewall and bottom capacitance densities respectively.

In this paper, an alternative layout technique is presented. Fig. 5 shows the concentric parallel cell layout. It is assumed that every transistor is divided into k parallel

cells, where k is an integer greater than or equal to 1. For every cell, the width and length are approximately 32λ and 2λ, respectively. Assuming the capacitance sensitive node is the drain and the drain is at the inside of the cell. It follows that the area and periphery of the drain and source are given respectively by

$$A_D=36\lambda^2$$

$$P_D==24\lambda$$

$$A_S=300\lambda^2$$

$$P_S=40\lambda \qquad (11)$$

Let us examine a simple example. Consider a transistor with a width of 64λ, and a length of 2λ. If the conventional layout structure is used, its drain area is $320\lambda^2$, and the periphery is 138λ. If the concentric parallel cell layout is used, the drain area is only $72\lambda^2$ and the drain periphery is 48λ. If used in a VCO, this reduction in diffusion capacitance will cause the VCO operation frequency increase substantially.

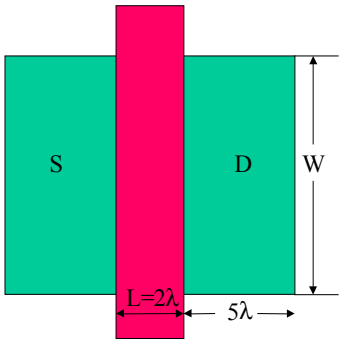

Fig. 4. Conventional layout structure

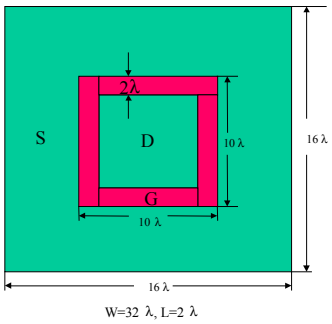

Fig. 5. Concentric parallel cell layout

Table 1 compares the VCO frequency for a conventional layout and the concentric layout for a 0.35 μm CMOS provided through the MOSIS service by Hewlett Packet. In this table, we selected $W_1=150\lambda$, $L_1=2\lambda$ and k for the load device from 2 to 6.

Form the simulation results, we can see that the improvement of the VCO frequency is about 23% by using the concentric layout technique.

TABLE1
THE INFLUENCE OF DIFFERENT LAYOUT

	Width of load transistor (μm)	VCO freq. convention layout(Hz)	VCO freq. Concentric layout
PMOS as active load	12.8	2.3G	2.8G
	19.2	2.7G	3.3G
	25.6	3G	3.7G
	32	3.2G	3.9G
	38.4	3.4G	4.1G

B. *Frequency enhancing with the NMOS load*

In the conventional differential delay stage, NMOS transistors are used as the input drive transistors and PMOS transistors are used as the active loads. From the discussion in Section II, we know that the VCO frequency increases with the transconductance per unit capacitance (gm/C) of the active load. Since the NMOS transistor has larger mobility than the PMOS transistor, the transconductance per unit capacitance of the NMOS transistors is larger than that of the PMOS transistors. So in order to further increase the VCO frequency, NMOS transistors are used as the active loads. Fig. 6 is the schematic of the modified delay stage.

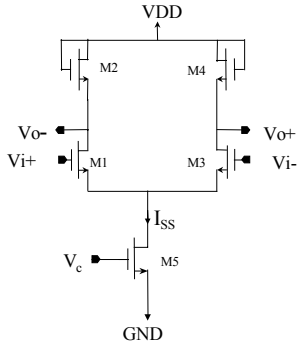

Fig. 6. delay cell using NMOS active load.

TABLE 2
THE INFLUENCE OF THE DIFFERENT LOAD

active load size (W)	VCO freq. @ PMOS as active load	VCO freq. @ NMOS as active load
25λ	N/A	2.4GHz
50λ	2.45GHz	3.5GHz
75λ	2.75GHz	4.2GHz
100λ	3GHz	N/A

Table 2 compares the VCO frequency at different active load for the conventional layout of Fig. 4. In order to make a fair comparison, the size of the input transistor was fixed to W_1=150λ and L_1=2λ.

From the simulation results, we can conclude that using NMOS transistor as the active load can increase the VCO frequency, provided that other conditions are kept the same as those when the PMOS transistor was used as the active load.

C. Frequency enhancement combining the (a) & (b)

Table (3) shows the results by combining layout technique and load selection technique. From these results, a 4.8GHz high operation frequency VCO is obtained using the 0.35μm CMOS process.

TABLE 3
THE FREQUENCY ENHANCING USING (A) & (B)

Width of load transistor (μm)	VCO freq. with Concentric layout
6.4	3.3G
12.8	4.7G
15	4.8G

D. Other issues in design the high speed VCO.

The differential-pair based VCO rejects power supply noise well, but the frequency adjustment range of operation may not be sufficient for some applications [1]. To widen the frequency adjusted range of differential-pair based VCO's, a current source can be paralleled with the load devices. The extra diffusion capacitance associating with implementation of the current source will degrade the frequency of operation.

The optimal gain of the delay cell also deserves attention. To insure oscillation, the gain should be kept greater than unity at the oscillation frequency. However, there is a trade off between the gain and the bandwidth of the amplifier. An exceedingly large gain would limit the maximum operation frequency of the VCO. Moreover, the timing jitter becomes larger when the gain of the delay cell increases [2]. So, in order to get a high operation frequency of the VCO, the gain of the delay cell should be minimized subject to the constrained that it be large enough to sustain oscillation.

IV. HIGH FREQUENCY VCO DESIGN

A high frequency voltage control ring oscillator based upon NMOS loads with all transistors using concentric layout has been designed. Emphasis was placed on maximizing the speed of operation while still maintain quadrature outputs. The quadrature output criterion restricted the minimum value of n to 4. Using a 0.35μm CMOS process. The VCO used 4-stages with W_5=270λ, W_1=W_3=150λ, W_2=W_4=50λ and all L= 2λ. Simulation results are shown in Fig. 7 and Fig. 8. From these simulations, it can be obtained that the frequency can be as high as 4.85 GHz and the tuning range is ±12%. If the quadrature output requires be sacrificed, further enhancement of the oscillation frequency can be achieved by reducing the number of stages to 3 or, with appropriate modifications, to 2.

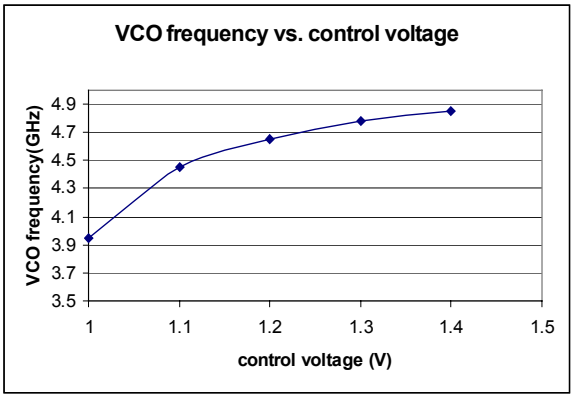

Fig. 7. VCO frequency vs. control voltage

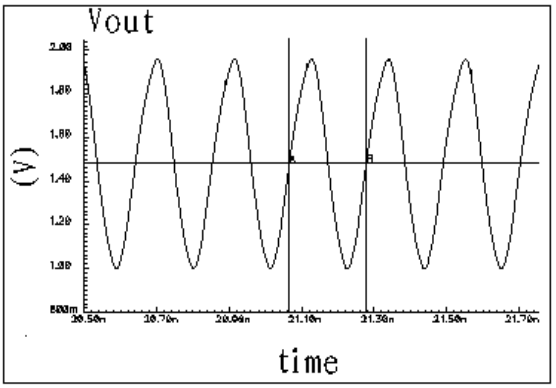

Fig. 8. VCO output waveform at 4.7GHz

V. CONCLUSION

In this paper, a high frequency voltage control ring oscillator design has been presented. This design achieves frequency enhancement through minimization of diffusion parasitics with concentric layout and the transconductance density optimization. A 4-stage VCO designed in a 0.35μm CMOS process can operate in the frequency of 4.5 GHz with a tuning range of ±12%.

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