Fast-Settling Amplifier Design Using Feedforward Compensation Technique

Jie Yan and Randall L. Geiger Department of Electrical and Computer Engineering Iowa State University Ames, IA 50011

Abstract-A feedforward compensation amplifier new architecture that provides very fast settling performance is introduced. The additional feedforward path introduces zeros in the open-loop transfer function which can be used to shape the overall frequency response. It is shown that a second-order bandpass feedforward path is useful for extending the unitygain-frequency of the overall amplifier. By choosing the proper gain, center frequency, and Q factor of the bandpass filter, the pole and zeros of the amplifier can be placed on top of each other thus eliminating the slow-settling component inherent in many feedforward compensation schemes. Simulation results of closed-loop amplifiers showing substantial improvements in rise time and settling behavior are presented.

INTRODUCTION

In many applications of op amps, the settling time of the amplifiers directly determines the system performance. For example, the limited settling time of the inter-stage amplifiers is one of the major obstacles limiting the performance of pipelined high sampling rate, high resolution ADCs. Feedforward compensation techniques has been used to stabilize operational amplifiers in low voltage applications. The feedforward signal path introduces zeros in the openloop transfer function that can be used to shape the overall frequency response typically by using the zeros for pole-zero cancellation. One undesirable property inherent in many feedforward compensation schemes is the existence of the slow-settling components in the step response of the amplifier. This is caused by mismatch between pole-zero pairs which results in imperfect pole-zero cancellation [1]. Several feedforward techniques have been presented [1], [2], [3], [4]. In these schemes, capacitors are used as feedforward elements connecting the input to the output or to intermediate output nodes. The exact pole-zero cancellation is affected by the parasitic capacitance. In this paper, a feedforward path that has a bandpass characteristic is added to a conventional amplifier. The LHP zeros are designed to exactly cancel with the lowest-frequency pole. As a result, the unity-gain frequency of the amplifier is greatly extended and an effective single-pole response is achieved. Formulas are derived for exact pole-zero cancellation. Simulation results show that the proposed amplifier structure has the potential to achieve a large unity-gain bandwidth and fast settling performance.

FAST SETTLING AMPLIFIER ARCHITECTURE

Fig. 1 shows the block diagram of the proposed fast-settling amplifier structure. The baseband path is denoted by a high gain amplifier with gain A(s) and the feedforward path is denoted by a bandpass filter with gain H(s). The compensated amplifier gain is given by



Figure 1 Block diagram of the proposed amplifier

Assume the basic amplifier A(s) is a single-pole amplifier that can be modeled by the transfer function

$$A(s) = \frac{A_0}{(1 + \frac{s}{\omega_{p1}})}$$
(2)

where A_0 is the DC gain and ω_{p1} is the bandwidth of the basic amplifier. Assume the bandpass filter is second-order modeled by the transfer function

$$H(s) = \frac{H_0 \frac{\omega_0}{Q} s}{(s^2 + \frac{\omega_0}{Q} s + \omega_0^2)}$$
(3)

where H_0 is the peak gain, ω_0 is the center frequency, and Q is the Q-factor of the bandpass filter.

From (1), the transfer function of the compensation amplifier is given by

$$A_{c}(s) = A(s) + H(s) = \frac{A_{0}}{(1 + \frac{s}{\omega_{p1}})} + \frac{H_{0}\frac{\omega_{0}}{Q}s}{(s^{2} + \frac{\omega_{0}}{Q}s + \omega_{0}^{2})}$$
(4)

The DC gain of the compensated amplifier remains the same as that of the basic amplifier. However, pole locations are changed and zeros are introduced by the feedforward path. The poles of the compensation amplifier $A_c(s)$ are given by $P1 = -\omega_{p1}$ 5(a)

$$P2 = \frac{\omega_0}{2Q} (-1 + \sqrt{1 - 4Q^2})$$
 5(b)

$$P3 = \frac{\omega_0}{2Q} (-1 - \sqrt{1 - 4Q^2})$$
 5(c)

The two zeros of the compensated amplifier are given by

$$Z_{1,2} = \frac{\omega_0}{2(A_0\omega_{p1}Q + H_0\omega_0)} (-A_0\omega_{p1} - H_0\omega_{p1} \pm \sqrt{A_0^2\omega_{p1}^2 + 2A_0\omega_{p1}^2H_0 + H_0^2\omega_{p1}^2 - 4A_0^2\omega_{p1}^2Q^2 - 4A_0\omega_{p1}QH_0\omega_0}$$
(6)

The position of the first pole is determined by the bandwidth of the basic amplifier while poles P2 and P3 are totally depended on the design parameters of the bandpass filter.

Assume ω_{p1} is the lowest-frequency pole so that the basic amplifier does not require a wide-bandwidth. $z_{1,2}$ can be designed so that z1 cancels with ω_{p1} . Different relationships can be used to achieve this pole-zero cancellation. One convenient way is to make the two zeros coincident and equal to P1. Equation (7) and (8) express the parameter relationships needed for this type of pole-zero cancellation.

$$\omega_{p1} = \frac{\omega_0 \omega_{p1}}{2(A_0 \omega_{p1} Q + H_0 \omega_0)} (A_0 + H_0)$$
(7)
$$\sqrt{A_0^2 \omega_{p1}^2 + 2A_0 \omega_{p1}^2 H_0 + H_0^2 \omega_{p1}^2 - 4A_0^2 \omega_{p1}^2 Q^2 - 4A_0 \omega_{p1} Q H_0 \omega_0} = 0$$
(8)

A manipulation of the above equations gives the following simpler but equivalent relationships

$$Q \le 0.5 \tag{9}$$

$$H_0 = A_0 \sqrt{1 - 4Q^2}$$
(10)

$$\omega_0 = \frac{2Q\omega_{p1}}{1 - \sqrt{1 - 4Q^2}} \tag{11}$$

If the above conditions are met, actually the two coincident LHP zeros will exactly cancel P1 and P2. This reduces the amplifier to a single pole amplifier with pole P3. It is observed that the bandwidth of the compensation amplifier will be

$$BW = -P3 = \frac{1 + \sqrt{1 - 4Q^2}}{1 - \sqrt{1 - 4Q^2}} \omega_{p1}$$
(12)

For Q<0.5, the bandwidth of the compensated amplifier will be larger than that of the basic amplifier. According to the derivation in [5], the compensated amplifier will have faster settling behavior than the basic amplifier. Fig. 2 shows the bandwidth enhancement(ω_{com}/ω_{p1}) and the gain and ω_o requirements for the bandpass network when Q changes. This plot shows the trade-off that must be considered when choosing Q. A small Q will result in a larger compensated amplifier bandwidth. However, this will require a high gain and high resonant frequency for the bandpass filter in the feedforward path.



Figure 2 Bandwidth and gain relationship with Q

SIMULATION RESULTS

In order to verify the settling performance of the proposed feedforward amplifier architecture, simulations were performed on a "10-bit" amplifier using Matlab. The basic amplifier should provide sufficient DC gain to ensure the required settling accuracy. For a "10-bit" performance, a minimum DC gain of 1000 will achieve 0.1% settling accuracy for a unity-gain feedback configuration. In this design, the DC gain of the basic amplifier was chosen to be 2,000. The bandwidth of the basic amplifier was chosen to be 3.5KHz. A pole Q of 0.2 which satisfies (9) was selected. H₀ and ω_0 were determined to be 1833 and 16.776kHz respectively.

The open-loop frequency response and the unity gain close-



Figure 3 Open-loop frequency response

loop frequency response of the basic amplifier and the compensated amplifier are shown in Fig. 3 and Fig. 4. The compensated amplifier has a single-pole response and its unity-gain bandwidth is much larger than that of the basic amplifier.



Figure 4 Unity-gain close-loop frequency response

Fig. 5(a) shows the unity-gain step responses of the basic amplifier and the compensated amplifier to a 1-V input step. Fig. 5(b) shows details of settling behavior at the 0.1% accuracy level.



Figure 5(a) Step response

Table 1 shows the unity-gain frequency, ω_{t} of the basic amplifier and the compensated amplifier for ω_{0} = 16.776kHz, H₀=1833 and Q=0.2. Table 2 summarizes the unity-gain step responses to a 1-V input step. Compared to the basic amplifier, it is clearly shown that the compensated amplifier has much faster settling performance.



Figure 5 (b) Expanded voltage scale

TABLE 1 BANDWIDTH COMPARISON OF COMPENSATED AND UNCOMPENSATED AMPLIFIER

	Basic	Compensated		
	amplifier	amplifier		
DC gain	2000	2000		
Unity-gain freq.				
(Hz)	7M	161M		
Phase margin	90 degree	90 degree		

TABLE 2 TRANSIENT RESPONSE

Time	Basic	Compensated	Improvement	
(ns)	amplifier	amplifier	ratio	
Rise time	50.1	2.1	23.86	
(10%-90%)				
2% settling time	89.4	3.8	23.53	
1% settling time	105.7	4.6	22.98	
0.2% settling time	147.6	6.4	23.06	
0.1% settling time	172.6	7.5	23.01	

Pole-zero mismatch plays an important role in high accuracy settling performance. In our design, this is controlled by the design parameters of the bandpass filter.

Imperfect pole-zero cancellation always introduces an additional settling term[5]. Since the proposed compensation technique cancels a low frequency pole, the imperfect pole-zero cancellation will introduce a long time constant which is generally referred to as a slow settling time constant. The slow settling time constant by itself, however, is not of concern. What is of concern is the magnitude of the resulting slow settling component in the output. If the magnitude of this slow settling component is sufficient small, the settling time of the compensated amplifier will be very fast. The robustness of the compensation technique must be considered to determine whether the improvements predicted in the simulations can be realistically achieved.

In order to test the robustness of the proposed amplifier structure, the design parameters H_0 , ω_0 and Q of the bandpass filter were all varied by $\pm 10\%$ from their ideal values. Fig. 6 shows the comparison of the settling time performance of the basic amplifier and the compensated amplifier when the design parameters of the bandpass are changed. This figure shows the rise time, and the time required for 2%, 1%, 0.2%, and 0.1% settling for various cases.



Figure 6 Comparison of the settling performance

These cases are defined as:

- Case 1: the basic amplifier,
- Case 2: nominal H_0 , Q, ω_0
- Case 3: H₀ increased by 10%
- Case 4: H₀ deceased by 10%
- Case 5: ω_0 increased by 10%
- Case 6: ω_0 decreased by 10%
- Case 7: Q increased by 10%
- Case 8: Q decreased by 10%
- Case 9: H_0 decreased by 10%, Q increased by 10%, and ω_0 decreased by 10%.

Figure 6 shows the design robustness of the compensated amplifier. Significant improvement in rise time and settling behavior is achievable even though the design parameters of the bandpass filter have a large variation.

CONCLUSION

A new amplifier architecture that uses bandpass feedforward compensation is presented. It is shown that a feedforward path that has a bandpass characteristic can be used to significantly extend the unity-gain-frequency of the overall amplifier. By choosing the proper gain, resonant frequency, and Q factor for the bandpass filter, the zeros can be placed on the top of the poles eliminating the slow-settling component. Simulation results predicted significant improvements in rise time and settling performance and demonstrated that the bandpass compensation scheme is reasonable robust.

ACKNOWLEDGEMENT

This work was supported, in part, by Texas Instruments Inc., RocketChips Inc. and R. J. Carver Trust.

References

[1] R. J. Apfel and P. R. Gray, "A fast-settling monolithic operational amplifier using doublet compression techniques," *IEEE J. Solid-State Circuits*, vol. Sc-9, No.6, pp332-340, Dec. 1974.

[2] W. Sansen and Z. Y. Chang, "Feedforward compensation techniques for high-frequency CMOS amplifier," *IEEE J. Solid-State Circuits*, vol.25, No.6, Dec. 1990.

[3] S. Setty and C. Toumazou, "Feedforward compensation technique in the design of low voltage opamps and OTAs," *IEEE ISCAS, vol. 1 pp464-467, 1998*

[4]R. Eschauzier and J. Huijsing, *Frequency Compensation Techniques for Low-Power Operational Amplifiers*. Boston, MA:Kluwer, 1995

[5] B. Y. Kamath, R. G. Meyer and P. R. Gray, "Relationship between frequency response and settling time of operational amplifiers," *IEEE J. Solid-State Circuits*, vol.sc-9, No. 6, pp347-352, Dec. 1974.