

# A Negative Conductance Voltage Gain Enhancement Technique for Low Voltage High Speed CMOS Op Amp Design

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**Abstract**-A new circuit technique for voltage gain enhancement in CMOS op amp design suitable for low voltage and high speed operation is presented in this paper. A negative conductance is used to cancel the positive output conductance of an amplifier thereby reducing the total equivalent output conductance and increasing the voltage gain of the amplifier. The negative conductance is derived from the output conductance of a transistor, as opposed to a transconductance or some other parameters, to enhance tracking over process and environment variations. A single stage CMOS op amp was designed using this technique that achieved a simulated DC gain of 83dB.

## INTRODUCTION

Op amps play an important role in many analog and mixed-signal systems. The realization of high-gain amplifiers with large Gain-Bandwidth-Products (GBW) in processes with decreasing supply voltage requires innovative circuit design techniques and advances in IC process technology. Since op amps are usually employed to implement feedback systems, the open-loop gain of an op amp determines the precision of the feedback system employing the op amp.

With a very high dc gain needed for precision applications, two approaches for gain enhancement have received considerable attention for many years. One is based upon gain multiplication achieved by cascading two or more lower gain stages. Although high dc gains are achievable, the excess phase shift introduced by the cascading introduces serious compensation requirements which limit the high frequency performance of cascaded amplifiers in feedback applications. The second approach achieves gain enhancement by increasing the output impedance of a basic gain stage. This approach has proven most effective at achieving high gains and high GBW with favorable power dissipation.

Three approaches for output impedance enhancement have been used. One uses cascoding, a second uses both cascoding and gain enhancement[1]. A third is based upon negative impedance compensation. Cascode topologies that exploit “stacking” of transistors were widely used in the past to achieve a high DC gain but they suffer from a limited output swing. As the feature sizes are reduced into the deep submicron region, the supply voltages are also decreasing. As the supply voltage is reduced, a key limitation that arises is a significant reduction in the number of devices that can be stacked between the power supply rails. For low supply

processes, traditional gain enhancement techniques such as cascoding become not viable. Another commonly used gain enhancement technique is gain-boosting [1]. Very high gains are achievable with gain-boosting but it still requires one level of stacking of devices thereby making it difficult to operate with low supply voltages. The gain-boosting amplifier also adds its own poles and consumes more power. Although negative impedance compensation offers potential for the most gain enhancement, low power dissipation, low voltage operation and excellent high frequency performance, the technique is seldom used commercially because of the high sensitivity of the gain to the negative compensating impedance inherent in existing negative impedance schemes.

In this paper, we exploit the negative impedance gain enhancement technique with an approach that significantly reduces the gain variability to the compensating impedance.

## NEGATIVE IMPEDANCE GAIN ENHANCEMENT

The basic well-known concept of gain enhancement by negative impedance compensation is shown in Fig.1(a). Negative resistor  $R_n$  is placed in parallel with the output impedance of the basic amplifier. It follows from the small signal equivalent circuit of Fig.1(b) that the dc gain of the amplifier is

$$A_v = \frac{V_o}{V_i} = \frac{-g_{m1}}{g_{ds1} + 1/R + 1/R_n} \quad (1)$$

$$\frac{1}{R_n} = -\left(\frac{1}{R} + g_{ds1}\right) \quad (2)$$

If  $R_n$  satisfies the equation (2), then the DC gain becomes, theoretically, infinite. Since the DC gain enhancement approach does not introduce additional internal nodes, it does not adversely reduce the high-frequency response of the basic

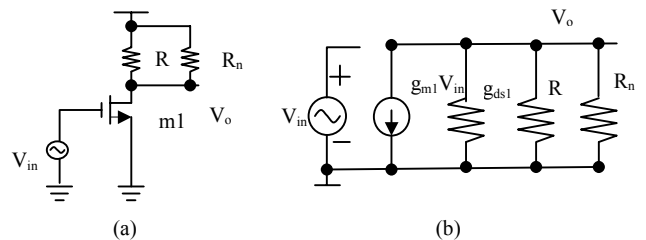


Figure 1 Basic concept of gain enhance by negative resistance  
 a) Basic amplifier stage b) small signal equivalent circuit

amplifier so wide bandwidth can be realized. Several researchers have proposed negative impedance gain enhancement circuits. One method of implementing the negative impedance discussed by Allstot is shown in Fig 2 [2]. It uses a cross-drain-coupled differential pair to generate the negative impedance. Assume the circuit is symmetrical and matched, a small signal analysis of this circuit gives the gain equation

$$A_d = \frac{V_o^+ - V_o^-}{V_i^+ - V_i^-} = \frac{g_{m1}}{g_{ds1} + g_{ds3} + g_{ds6} + g_{m3} - g_{m6}} \approx \frac{g_{m1}}{g_{m3} - g_{m6}} \quad (3)$$

Since the transconductance  $g_m$  is quite sensitive to temperature and process variations, any mismatches between  $g_{m3}$  and  $g_{m6}$  may cause the gain become infinity or actually cause gain sign reversal. If this occurs, the stage will operate

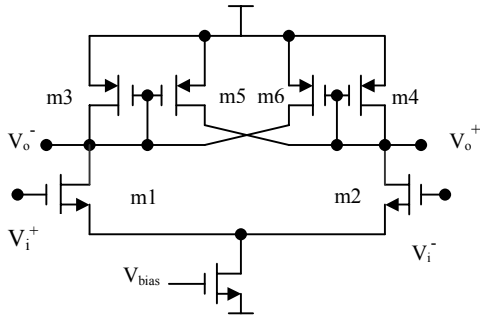


Figure 2 Drain-coupled differential pair

as a cross-coupled latch. A reasonable ratio between  $g_{m3}$  and  $g_{m6}$  is 0.75, which only increases the gain by a factor of 4 [3].

Nauta also applied negative resistance to a simple inverter transconductor in order to increase the DC gain of the transconductor. [4], [5]. In the Nauta circuit, the negative resistance is generated by applying differential output signals to matched inverters. The negative resistance is proportional to  $1/\Delta g_m$ . A DC gain of 46dB with a 10V power supply was reported. In [6], positive feedback was applied to generate an effective negative load conductance which is given by  $g_m * A + g_{ds}$ , where A denotes the amount of feedback applied to the gate. Although a gain of 80dB was reported in [6] with a 10V power supply voltage, the gain-bandwidth-product is only 12MHz for a 5pF capacitor load. The structure in [6] requires a high frequency, high differential gain stage to achieve conductance cancellation. This gain stage introduces internal nodes and thus limits the high-frequency response of the amplifier.

These structures all share a common characteristic, a negative transconductance is used to compensate for positive output conductances and/or transconductances and to achieve large gain enhancement, the negative transconductance must precisely compensate the positive output conductance. Major

drawback of using negative transconductance ( $-g_m$ ) to compensate the output conductance  $g_{ds}$  is the inability to accurately match these terms so gain enhancement is difficult to achieve. Also, both  $g_m$  and  $g_{ds}$  are sensitive to bias current, process and temperature but in much different ways [7]. Therefore, using a negative  $g_m$  to compensate for the positive output conductance  $g_{ds}$  offers little potential for practical applications.

In this paper, a circuit is proposed that generate a negative conductance that is only the function of  $g_{ds}$  and is not related to  $g_m$ . This negative conductance circuit is added at the output of a simple one-stage amplifier to practically achieve gain enhancement. A CMOS implementation of the proposed amplifier demonstrates a simulated DC gain of 83dB and a unit-gain bandwidth of 133MHz for a 2pF capacitor load with only 2.4mW of power dissipation.

### PRINCIPLE OF THE HIGH GAIN AMPLIFIER

A basic amplifier is shown in Fig. 3. The low-frequency voltage gain is given by

$$A_v = \frac{-g_{m1}}{g_{ds1} + g_{ds2}} \quad (4)$$

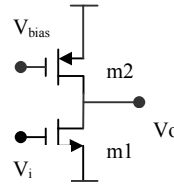


Figure 3 The basic amplifier

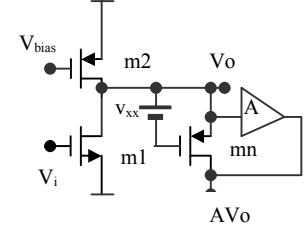


Figure 4 Proposed amplifier with the negative conductance

Fig. 4 shows the concept of the proposed negative conductance gain enhancement technique. A PMOS transistor mn is placed at the output of the basic amplifier. A low gain stage A is connected between the gate and the source of mn. Transistor mn is biased in the saturation region and its gate-source voltage is AC shorted. Body effects can be ignored if an n-well CMOS process is used. If the gain of the low gain stage A is larger than 1, then a negative conductance of  $(1-A) \cdot g_{dsmn}$  will be presented in parallel with the output conductance of the basic amplifier. The small signal dc gain of this circuit is given by the expression (5)

$$A_v \approx \frac{-g_{m1}}{g_{ds1} + g_{ds2} + g_{dsmn}(1-A)} \quad (5)$$

If  $g_{ds1} + g_{ds2} = (A-1) \cdot g_{dsmn}$ , the gain of the amplifier will be infinite.

## CIRCUIT IMPLEMENTATION AND SIMULATION RESULTS

Fig. 5 shows the transistor-level schematic diagram of an operational amplifier designed using the negative conductance gain enhancement technique. The circuit consists of the basic differential amplifier, the low gain stage A, the negative  $g_{ds}$  generator transistor and the biasing circuit. The basic amplifier is composed of transistors m1-m4 and m16. It is a differential-input, single-ended-output gain stage. The low gain stage A consists of transistors m8-m13. It has two common-source stages with diode-connected loads. m12 and m13 form a source-follower for voltage level shifting. The negative  $g_{ds}$  generator transistor is m5. m6 and m7 provide biasing current for m5. m14 and m15 provide biasing gate-source voltage for m5.

The overall DC gain of the amplifier can be derived as

$$A_v \approx \frac{g_{m1}}{g_{ds2} + g_{ds4} + g_{ds6} + (1-A)g_{ds5}} \quad (6)$$

$$\text{where } A = \frac{g_{m8}}{g_{m9}} \cdot \frac{g_{m11}}{g_{m10}} \cdot \frac{g_{m12}}{g_{m12} + g_{mb12}} \quad (7)$$

A is designed to be between 2.5 to 3.0. If A is designed too large, it will show output swing limitations when a large input step is applied.

The circuit was designed with a 0.35um CMOS process and simulated in HSPICE. Level39 models were used and parasitic effects of transistors were included in the simulation.

Without negative impedance compensation, the basic amplifier achieves a DC gain of only 46 dB. Fig. 6 shows the plot of overall open-loop AC response of the high gain amplifier. Simulation results indicated a DC gain of 83 dB and a unity-gain frequency of 133MHz were achieved when driving a 2pF load. Since the implementation of gain enhancement does not introduce additional internal nodes, the wide-bandwidth of the basic amplifier is preserved.

The amplifier has been simulated as a unity-gain voltage-follower. Fig. 7 shows the unity-gain feedback transient step response. With a 0.5V step input, the amplifier settles to its final value at 0.1% accuracy in 10.5ns.

The performance of the amplifier is summarized in Table 1.

TABLE 1. OP AMP PERFORMANCE

Supply voltage	3V
Process	CMOS 0.35um
DC Gain	83dB
Power dissipation	2.4mW
Unity-gain frequency	$C_L=2pF$ , 133MHz $C_L=5pF$ , 71MHz
Phase margin	$C_L=2pF$ , 53 degree $C_L=5pF$ , 65 degree
0.1% Settling time (100mV step input)	$C_L=2pF$ , 6.9ns $C_L=5pF$ , 11.3ns
0.1% Settling time (500mV step input)	$C_L=2pF$ , 10.5ns $C_L=5pF$ , 13.3ns

## CONCLUSION

A gain enhancement technique based on conductance cancellation was introduced. Simulation results of an example circuit showed a 37dB gain enhancement and a unity-gain bandwidth of 133MHz when driving a 2pF load. The technique offers potential for gain enhancement with very low power supply voltages while maintaining a high gain-bandwidth-product.

## ACKNOWLEDGEMENT

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## REFERENCES

- [1] K.Bult and G.J.G.H. Geelen, "A Fast-Settling CMOS Amplifier for SC Circuits with 90-dB DC Gain," *IEEE J. of solid-state Circuits*, vol.25, pp. 1379-1384, Dec1990
- [2] D.J. Allstot, "A Precision Variable-Supply CMOS Comparator", *IEEE J. Solid-State Circuit*, SC-17 (6), pp1080-1087, 1982
- [3] R.Gregorian, *Introduction to CMOS Op-Amps and Comparators*, John Wiley & Sons, 1999
- [4] B.Nauta and E.Seevinck, "Linear CMOS Transconductance Element for VHF Filters", *Electron.Lett.*, 1989, 25, pp448-450
- [5] B. Nauta, "A CMOS Transconductance-C Filter Technique for Very High Frequencies", *IEEE J. Solid-State Circuits*, vol. 27, No.2, pp142-153, Feb. 1992.
- [6] S.L. Wong and C.A.T. Salama, "Voltage Gain Enhancement by Conductance Cancellation in CMOS Op Amps", *ISCAS' 1984*, pp1207-121.
- [7] Xiaole Chen, US patent No.5570049

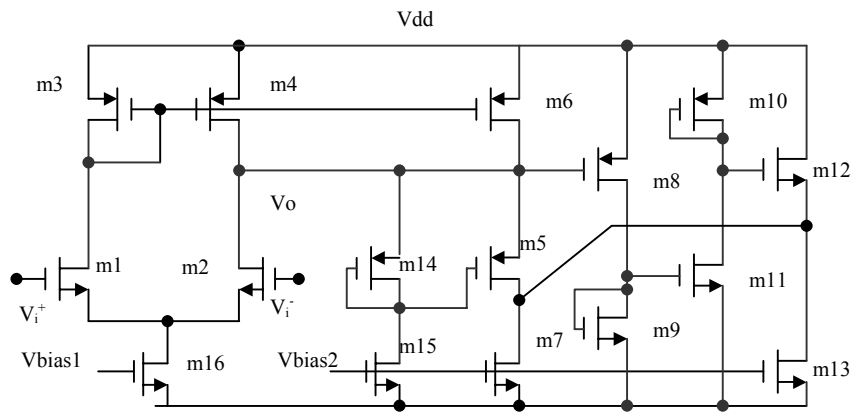


Figure 5 Schematic of the designed amplifier

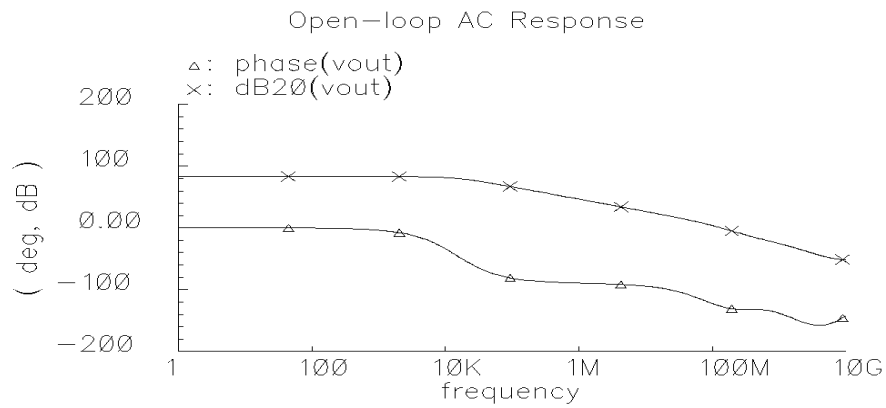


Figure 6 Open-loop frequency response of the designed amplifier

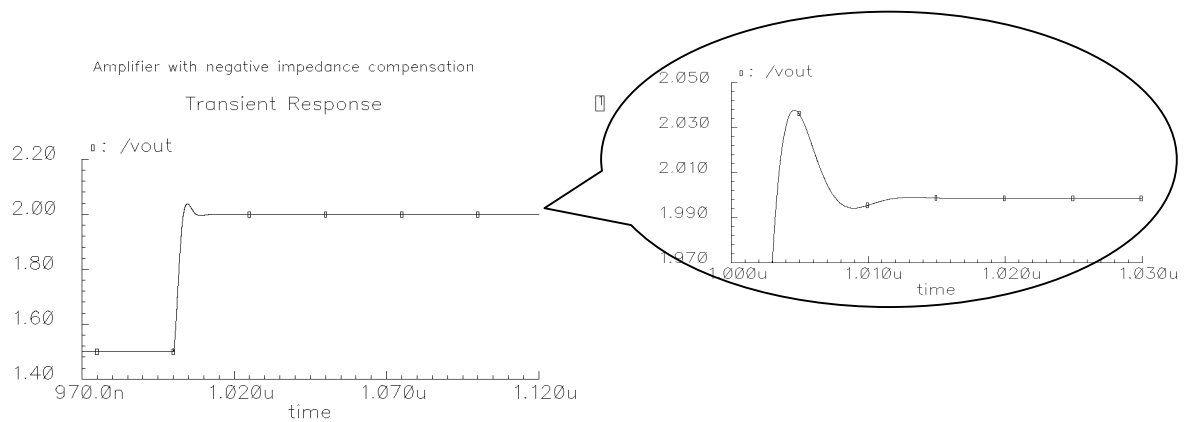


Figure 7 Unity-gain step response of the designed amplifier