Unambiguous characterization and specification of D/A converter performance*

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Abstract – **Existing parameters used to characterize the performance of D/A converters are often not rigorously defined or are based upon ambiguous nested definitions. This makes it difficult for the user to determine how a particular D/A will really perform in a specific application and leaves some room for uncertainty when testing D/As. Key performance parameters that affect the static and low frequency performance of Nyquist Rate Converters are unambiguously defined in this paper. Emphasis is on definitions that realistically predict how a D/A will perform and that make parameter measurements in the laboratory practical.**

I. INTRODUCTION

The exponential growth witnessed recently in the area of digital communication equipment used in wireless communications has resulted in a great deal of interest in the design of data converters. This has led to a rapid growth of data converter markets, with the availability of devices having a wide range of performance parameters. Even though all D/A and A/D converters of a given resolution ideally exhibit identical transfer characteristics, they differ in practice by considerable amounts.

Often the appropriate selection of hardware for a given application becomes a difficult task due to the shortcomings in the way these devices are characterized. Though many manufacturers/authors have tried to define even the most basic performance parameters, there still exists considerable ambiguity in the way the parameters are specified. The need exists to precisely define converter performance parameters to enable the user to choose an appropriate device based on their actual performance requirements.

Another factor driving the need for a standard performance characterization is the pending emergence of Built-In-Self-Test (BIST) structures for data converters. With the cost of silicon in many data converter products becoming dominated by testing costs, Built-In-Self-Test (BIST) structures offer potential for not only reducing the direct cost of testing, but also reducing the indirect cost associated with production time. Although some variants in performance characterization parameters may not adversely affect the characterization of a converter, the implications of these variants on testing algorithms and testing time on existing testers can be substantial but the implications on BIST implementations can be even more significant. For BIST for data converters to become viable, it is desirable that testing schemes and structures be as simple as possible. Since data converters traditionally have a long product life, it is also desirable to have the data converter design community agree on specifications that will not change often. This requires identification of the key parameters and precise definitions of these parameters.

Several different terms are widely used when discussing the performance of D/A converters. These include "Resolution", "Integral Nonlinearity (INL)", and "Differential Nonlinearity (DNL)" along with several others. These terms are so commonly used that one would be tempted to assume that there is universal agreement on what they mean and how they should be defined. However, not only are there differences in definition from one source to another, but also, most attempts to define these parameters involve parameters that are not precisely or unambiguously defined. Of course, if these alternate definitions resulted in differences in perception about the overall performance of the D/A that were inconsequential, the imprecise nature or ambiguity would be only of academic interest. Unfortunately, the differences are of sufficient magnitude to cause possible misinterpretation of the real performance of a D/A in some applications.

In what follows, several key performance features for D/A converters are discussed, comparisons are made between alternate parameters that are used to characterize these features and unambiguous and consistent definitions of parameters are proposed that both capture the basic essence of key performance features and make measurement of the parameters manageable.

II. SPECIFICATIONS

A. Resolution

This is one of the most basic terms. In [1] it is defined as

"…the number of distinct analog levels corresponding to the different digital words. Thus, an N-bit resolution implies that the converter can resolve 2^N distinct analog levels";

In [2] it is defined as

"An N-bit binary converter should be able to provide 2^N distinct and different analog output values corresponding to the set of N-bit binary words. A converter that satisfies this criterion is said to have a resolution of N bits",

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whereas in [4] it is defined by

" Resolution is the smallest level separation (input levels for A/D and output levels for D/A) that is unambiguously distinguishable over the full-scale range of the converter".

The first two definitions imply more or less the same central idea; a converter with N-bit resolution has 2^N outputs (in the case of a D/A). The first two definitions are totally determined by architecture and need not be measured. They provide little insight into performance. They are also dimensionless. The third is much different. It requires measurement and will have units of either volts or amps.

In the first two definitions, no mention is made about whether N is an integer although that assumption is often made as well. Though almost all D/A converters available in the market today deal with an integer number for resolution ('N' input bits and 2^N output levels), the concept of 'N' being an integer is traditional. Applications abound in which the number of distinct levels required at the output of a D/A is not an integer power of 2. A device which outputs a temperature value in 1^oC degree increments from 0^oC to 100^oC or a percent value is an example where the number of required output levels equals 100. While using a 6-bit converter is not sufficient due to the maximum availability of 64 output levels, the use of 7-bit converter will result in an extra 28 levels which are not required and the quantization levels of the N-bit converter will likely not be aligned with those of the 100-level system.

A slightly modified definition based upon the philosophy behind the first two definitions which is suitable from a testing perspective is to define resolution based upon the number of transitions encountered while testing by the relation

$$R = \log_2(S+1) \qquad (1)$$

where S is the number of distinct transitions. With this definition, R can be either an integer or a real number depending on the value of S.

B. Effective Resolution

The resolution as defined by (1) gives little indication about the resolving capability of a D/A. The concept of the effective resolution which is conveyed in the third definition [4] above does address the resolving capability. We will define the resolving capability as the smallest increment that can be guaranteed to be resolved with increasing input codes or the smallest decrement that can be guaranteed to be resolved with decreasing input codes.

This definition of resolving capability is motivated by the philosophy on which many control applications operate. These applications are based upon algorithms which increase the output of the DAC by increasing the input code or decrease the output of the DAC by decreasing the input code. The effective resolution will now be formally defined. To do this, consider the output levels for consecutive input codes as depicted in Fig.1. that are given by the sequence δ.

$$\delta = < X_0, X_1, X_2, \ldots\ldots\ldots X_k, X_{k+1} \ldots X_S > \qquad (2)$$

where the element X_k corresponds to input code C_k.

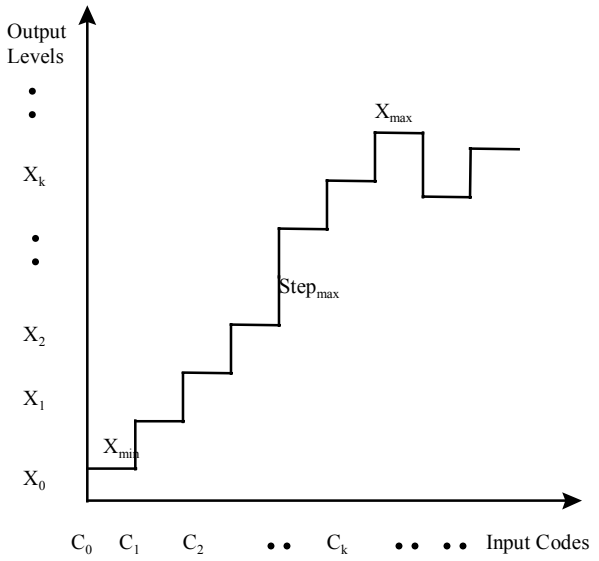

Fig.1. DAC Transfer Characteristics

In an ideal DAC, the sequence δ is not only monotonic but also the elements in the sequence increase linearly with the input code. In an actual DAC, the linear increase with input code is not guaranteed and the sequence may actually become non-monotonic. Consider now the two new sequences obtained from δ by rank ordering the elements of δ in increasing order and decreasing order. Denote these two sequences by

$$\delta_I = < Y_0, Y_1, Y_2, \ldots\ldots\ldots Y_S > \qquad (3)$$

and

$$\delta_D = < Z_S, \ldots\ldots\ldots Z_2, Z_1, Z_0 > \qquad (4)$$

Note the arbitrary elements Y_k and Z_k no longer correspond to the input code C_k. Since the input codes corresponding to the elements of the sequence in δ_I may not be in increasing order, a new monotone sequence $\hat{\delta}_{Inc}$ is derived from δ_I. The new sequence, $\hat{\delta}_{Inc}$ has the property that both the output levels and the corresponding input codes show an increasing trend. The new sequence $\hat{\delta}_{Inc}$ will be obtained by the following iterative procedure:

(1) Let $h = 0$

(2) Define the sequence $\hat{\delta}_{Inc}(0) = \delta_I$

(3) Check the input code of $\hat{\delta}_{Inc}(h)$ for monotonicity (assume the elements of $\hat{\delta}_{Inc}(h)$ are denoted as Y_{hi} for $i = 1,2,\ldots\ldots,S_h$)

(a) If the input code of $\hat{\delta}_{Inc}(h)$ is monotonically increasing, define $\hat{\delta}_{Inc} = \hat{\delta}_{Inc}(h)$.

(b) If the input codes for $\hat{\delta}_{Inc}(h)$ are not in increasing order, then

(A) Locate Y_{hi} which is the smallest element of the sequence $\hat{\delta}_{Inc}(h)$ where there exists a $Y_{hj,}$ $j > i$, where the input code of Y_{hj} is less than the input code of Y_{hi}.

(B) Define the new sequence $\hat{\delta}_{Inc}(h+1)$ to be the sequence obtained by eliminating Y_{hi} from the sequence $\hat{\delta}_{Inc}(h)$.

(C) Increase h by 1.

(D) Return to the start of Step 3.

The new sequence obtained is then,

$$\hat{\delta}_{Inc} = < \hat{Y}_0, \hat{Y}_1, \hat{Y}_2, \ldots\ldots\ldots \hat{Y}_{L-1} > \quad (5)$$

Define the sequence of step sizes by

$$Step+ = <S_{0+}, S_{1+}, S_{2+}, \ldots\ldots S_{k+}, \ldots\ldots S_{(L-2)+}> \quad (6)$$

where $S_{k+} = \hat{Y}_{k+1} - \hat{Y}_k$, $k \in \{0,1,\ldots L-2\}$
and define $Step_{max+}$ by,

$$Step_{max+} = Max \{ S_{0+}, S_{1+}, S_{2+}, \ldots S_{k+}, \ldots\ldots S_{(L-2)+}\} \quad (7)$$

We now define the effective resolution (for increasing input code) by

$$R_{eff+} = \log_2((\hat{Y}_{L-1} - \hat{Y}_0)/ Step_{max+} + 1) \quad (8)$$

and the number of effective transitions to be

$$T_{eff+} = L - 1 \quad (9)$$

Similarly, a new sequence $\hat{\delta}_{Dec}$ is obtained from δ_D such that the output levels and the corresponding input codes show a decreasing trend. The new sequence obtained is then,

$$\hat{\delta}_{Dec} = < \hat{Z}_{M-1}, \ldots\ldots\ldots, \hat{Z}_2, \hat{Z}_1, \hat{Z}_0 > \quad (10)$$

Define the sequence of step sizes by

$$Step- = <S_{(M-2)-}, \ldots\ldots\ldots, S_{k-}, \ldots\ldots S_{1-}, S_{0-}> \quad (11)$$

where $S_{k-} = \hat{Z}_{(k+1)} - \hat{Z}_{(k)}$, $k \in \{M-2,\ldots,1,0\}$
and define $Step_{max-}$ by,

$$Step_{max-} = Max \{ S_{(M-2)-}, \ldots\ldots\ldots, S_{k-}, \ldots\ldots S_{1-}, S_{0-}\} \quad (12)$$

We now define the effective resolution (for decreasing input code) by

$$R_{eff-} = \log_2((\hat{Z}_{M-1} - \hat{Z}_0)/ Step_{max-} + 1) \quad (13)$$

and the number of effective transitions to be

$$T_{eff-} = M - 1 \quad (14)$$

The effective resolution of the converter is then defined to be

$$R_{eff} = Min\{R_{eff+}, R_{eff-}\} \quad (15)$$

and the number of effective transitions to be

$$T_{eff} = Min\{T_{eff+}, T_{eff-}\} \quad (16)$$

C. X_{LSB}

X_{LSB} is a term closely related to resolution and is defined in [1] as

"….the voltage change when 1LSB changes"

where X is a voltage signal, and is mathematically given by

$$\hat{X}_{LSB} = X_{ref}/2^N \quad (17)$$

Even though the definition is seemingly simple, whether this relationship between a reference signal and the constant N really represents an LSB is not apparent. X_{ref} is usually the input reference signal (can be any physical quantity like voltage, charge or current). Ideally the output voltage of a D/A converter for maximum input (all bits '1') is related to the reference signal by

$$X_{omax} = X_{ref}(1-2^{-N}) \quad (18)$$

But when a device is tested, seldom does the output of the converter actually equal this value of $X_{ref}(1-2^{-N})$ for maximum input code. Thus the definition of X_{LSB}, based on the ideal X_{ref} value is not quite correct. It is more reasonable to relate X_{LSB} to the maximum signal value reached at the output of the converter while testing. X_{LSB} can be defined as

$$X_{LSB} = (X_{max} - X_{min})/T_{eff} \quad (19)$$

where X_{max} is the maximum output, X_{min} is the minimum output and T_{eff} is the number of effective transitions as given in (16). This definition, although similar to the existing ones, deals more clearly with the practical case and is convenient to measure from a testing point of view.

D. Offset Error & Gain Error

Offset error is defined in [1] as

"In a D/A converter, the offset error, E_{off}, is defined to be the output that occurs for the input code that should produce zero output"
mathematically

$$\hat{X}_{Off} = X_{out}|_{00...00} / \hat{X}_{LSB} \quad (20)$$

A minor modification would be to define this in terms of X_{LSB} as per (19), and the new definition is

$$X_{off} = X_0 / X_{LSB} \quad (21)$$

Gain error in LSB is defined in [1] as

"…the difference at the full-scale value between the ideal and actual curves when the offset error has been reduced to zero."

For a D/A converter, the gain error, in units of LSBs, is

$$\hat{E}_{gain} = (X_{out}|_{11\ldots1} - X_{out}|_{00\ldots0}) / \hat{X}_{LSB} - (2^N - 1) \quad (22)$$

or equivalently,

$$\hat{E}_{gain} = (X_{(2^N-1)} - X_0) / \hat{X}_{LSB} - (2^N - 1) \quad (23)$$

Since the number of transitions in a D/A may not necessarily be one less than an integral power of 2, we will define the gain error by

$$E_{gain} = (X_S - X_0) / X_{LSB} - T_{eff} \quad (24)$$

E. Differential Nonlinearity (DNL)

INL and DNL are two closely related parameters which are usually specified and are considered as critical performance parameters. In [1] the author defines DNL as

"DNL is defined as the variation in analog step sizes away from 1LSB (typically, once gain and offset errors have been removed)"

while in [2] the author states it as

"In a D/A converter, any two adjacent digital codes should result in measured output values that are exactly 1LSB apart (2^{-N} of full scale for an N-bit converter). Any positive or negative deviation of the measured "step" from the ideal difference is called Differential Nonlinearity, expressed in (sub)multiples of 1LSB."

Often, DNL is specified as the worst case deviation obtained from 1LSB. In terms of the modified definition of X_{LSB}, DNL of i_{th} element is defined as

$$DNL_i = (Stepactual_i / X_{LSB}) - 1, \quad (25)$$

where

$$Stepactual_i = X_{i+1} - X_i \quad (26)$$

DNL is then

$$DNL = Max\{DNL_i\} \quad (27)$$

F. Integral Nonlinearity (INL)

INL is defined in [1] as

"INL error is defined to be the deviation from a straight line"

where two different methods of obtaining straight line based on either end points of the converter's transfer characteristics or a best-fit line such that the mean squared error is reduced, has been described.

and in [3] as

"….the deviation of the output signal or output code of a converter from a straight line drawn through zero and full scale. Output signals or output codes must be corrected from a possible zero offset".

The straight line drawn can either be "end-point line" connecting the end points of the characteristics or a "best-fit line". There can be different "best-fit" lines but the minimum mean square fit is often used. Each one has its own pros and cons, and there is no single factor specifying one to be superior to the other. While the "end-point line" is easy to measure (from testing perspective), it does not provide good insight into converter operation. On the other hand, the "best-fit line", though more tedious to measure, gives a better indication of the Total Harmonic Distortion (THD) that will be exhibited. DNL and INL are related as

The INL of any code is the summation of DNL of all codes below it.

$$INL_i = \sum_{j=0}^{i} DNL_j \quad (28)$$

INL is then,

$$INL = Max\{INL_i\} \quad (29)$$

Both DNL and INL are important as they are sensitive to different issues. INL is more sensitive to cumulative effects while DNL is more sensitive to individual codes.

G. Monotonicity

Monotonicity is one another parameter usually specified for any converter. Monotonic converter as defined in [1] is

"A monotonic D/A converter is one in which the output always increases as the input increases. In other words, the slope of the D/A converter's transfer response is of only one sign. If the maximum DNL error is less than 1LSB, then a D/A converter is guaranteed to be monotonic "

whereas in [3] it is defined as

"Monotonicity of a converter means that the output of, for example, a D/A converter never decreases with an increasing digital input code. A minimum increase of zero is allowed for a 1LSB increase in input signal in a D/A converter".

Monotonicity is guaranteed if the DNL_i is not more negative than -1LSB for all 'i' but it can be more positive than 1LSB. Equivalently, a D/A is monotonic iff,

$$Stepactual_i >= 0; i = 1….S \quad (30)$$

III. Conclusion

A comparison of basic specifications of Data Converter performance has been made and the ambiguities related to them has been addressed. An attempt has been made to present a precise, realistic, easily measured and unambiguous definitions of the key performance parameters. Although not all the parameters have been dealt with, most of the key issues relating to a converter's static performance (in particular D/A's) have been considered.

References

[1] David A. Johns and Ken Martin. *Analog Integrated Circuit Design*. John Wiley & Sons, Inc., 1997.

[2] Analog Devices. *Analog-Digital Conversion Handbook.* Prentice Hall, Englewood Cliffs, New Jersey, 1986.

[3] R. Van de Plassche. *Integrated Analog-to-Digital and Digital-to-Analog Converters*. Kluwer Academic Publishers, Dordrecht, the Netherlands, 1994.

[4] S.K.Tewksbury et al., *Terminology Related to the Performance of S/H, A/D and D/A Circuits*, IEEE Transactions on Circuits and Systems, CAS-25, Vol.CAS-25, pp.419-426, July 1978.sf