Minimization of Area in Low-Resistance MOS Switches

Saqib Q. Malik and Randall L. Geiger
Iowa State University
Department of Electrical and Computer Engineering
Ames, IA 50010

Abstract - Several different layout schemes that are useful for implementing low resistance switches with MOS transistors are discussed and characterized. A comparison of the area required for implementing a switch with a standard alternating bar approach is made with layouts using waffle structures, serpentine structures, and modified waffle structures. Analytical design equations for these non-conventional geometries are introduced. The comparisons show that in typical processes, area reductions of over 40% are readily achievable with the modified waffle structures.

I. Introduction

The effective resistance of MOS transistors operated as switches is affected by several parameters. The four that generally receive the most attention are the W/L ratio, the excess bias, the series diffusion resistance, and the contact resistance. For MOS transistors used as switches that must achieve extremely low on-resistance, large effective W/L ratios are used along with multiple contacts to the drain and source diffusions. For most layouts of the switch, the total resistance of the switch can be expressed as the sum of three resistances. One, termed R_{FET}, represents the "on" resistance associated with the channel of the transistor itself and is determined by the effective W/L ratio and the excess bias. A second, termed R_{via}, is due to the contact resistance to the drain and source diffusions of the switch. The third, termed R_{diff}, is due to the series resistance in the diffusions between the edge of the channel and the via. The resistance associated with the metal interconnects is generally negligible compared to these three resistances. Thus, a single-transistor MOS switch can be modeled by a resistor expressed as

$$R_{sw} = R_{FET} + R_{via} + R_{diff} \qquad (1)$$

For the simple MOS switch driven on with a control voltage of V_{DD} and with the layout shown in Fig. 1a, the three parts are approximately given by

$$R_{FET} = \frac{1}{K' \cdot \frac{W}{L} \cdot (V_{DD} - V_T)} \qquad (2)$$

$$R_{via} = 2 \cdot R_{cont} \qquad (3)$$

$$R_{diff} = R_{sq} \cdot \frac{a+b}{W} \qquad (4)$$

where R_{cont} is the contact resistance, K' is the transconductance parameter of the MOSFET, R_{sq} is the diffusion sheet resistance, and V_T is the threshold voltage. For a minimum-sized n-channel transistor in a typical process with W = L, a = b = 2·W, R_{sq} = 5Ω/ , $K' = 230\mu$ A/V^2, V_T = 0.5V, V_{DD} = 2.5V and R_{cont}=7Ω, the total switch resistance as given by (1) becomes:

$$R_{sw} = 2173 + 14 + 20 = 2207 \qquad (5)$$

The contributions due to R_{via} and R_{diff} thus represent about 0.63% and 0.91% of the total resistance respectively. It can be concluded that for this simple structure, the contact resistances and the diffusion resistances are negligible. On structures with very large W/L ratios, the term R_{FET} can be driven to arbitrarily low values. Simultaneously, with most common layout schemes, multiple vias will be made to contact the diffusions thus driving R_{via} and R_{diff} down as well. With a little care in layout, these two resistances will scale approximately linearly with R_{FET} thus keeping their contribution to R_{sw} negligible.

Some applications require switch resistance in the few ohms range or even smaller. From (5), it is apparent that very large effective W/L ratios are required to achieve this. For example, a switch with an on-resistance of 1 Ω would require an effective W/L ratio of about 2200 in the process detailed above. The silicon area implications associated with such a resistor are significant. Major improvements in area efficiency over what is achievable by the serpentined structure or the alternating bar structure are possible by judicious layout schemes. These layout schemes can offer economic benefits where a substantial portion of a part is devoted to switches that must have low on resistance. These will be discussed after developing a method for comparing alternative layout structures.
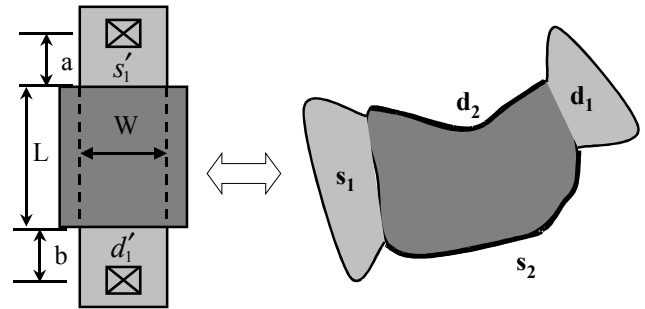

Fig. 1 (a) Typical Layout (b) An irregular transistor

II. Layout Comparison Methods

Most layouts of large transistors are based upon attempts to replicate not just the large W/L ratio of the transistor but also the rectangular aspect of the transistor. The layout methods discussed here will not be based upon any association with a rectangular gate region for the transistor. Two important conclusions from a theorem in [1] will be used instead. First, corresponding to any arbitrary shaped device that has two disconnected diffusion regions separated

by a channel region, there is a rectangular MOS transistor that has the same I-V characteristics. Second, for any transistor, the effective W/L ratio can be obtained either from the transistor of interest or by taking the reciprocal of the effective W/L ratio of the reciprocal transistor. Consider Fig. 1b for instance. According to the theorem, there is an equivalent rectangular device corresponding to the irregularly shaped transistor with source and drain shown by s_1 and d_1 respectively. A reciprocal transistor is formed by the regions s_2 and d_2 as the source and drain respectively. According to the theorem, the effective W/L of the device formed by s_1 and d_1 is the reciprocal of the effective W/L of the reciprocal transistor formed by s_2 and d_2.

To effectively utilize layouts that are not based upon the rectangular transistor, it is necessary to determine the effective W/L ratio and area of the nonrectangular structure. In what follows, we will see all large structures of interest in this work can be represented as the parallel interconnection of an arbitrary number of identical smaller structures, termed reference cells. We will thus characterize the effective W/L ratio of the reference cells and the area of the reference cells and from this determine the effective W/L of the actual transistor.

If R_{des} is the desired resistance of the switch, then if via and diffusion resistances are neglected, the area needed to achieve this resistance is given by the expression

$$A = \frac{R_{ref} \cdot A_{ref}}{R_{des}} \tag{6}$$

where R_{ref} is the resistance of the reference cell and A_{ref} is the area of the reference cell. The resistance of the reference cell is given by the expression

$$R_{ref} = \frac{1}{K' \cdot \left(\frac{W}{L}\right)_{eff} \cdot (V_{DD} - V_T)} \tag{7}$$

where $\left(\frac{W}{L}\right)_{eff}$ is the effective W/L ratio of the reference cell. From (6) and (7), it follows that the normalized reference area, $A_{ref,n}$, defined by

$$A_{ref,n} = \frac{A_{ref}}{\left(\frac{W}{L}\right)_{eff}} \tag{8}$$

is a figure of merit for comparing different layout structures with the total area being proportional to $A_{ref,n}$. With this figure of merit, structures with a smaller $A_{ref,n}$ will result in more area efficient layout than structures with larger $A_{ref,n}$. Expressions for $(W/L)_{eff}$, A_{ref}, and $A_{ref,n}$ for several different layouts will be given.

III. LAYOUT STRUCTURES

Several different layout structures will be discussed in this section. Some of the geometric structures that will be presented are based upon the design rules of the process. The critical feature sizes are denoted by $d_1 \ldots d_7$ as described in Table 1. Often λ-based design rules are used. If λ-based design rules are used, the relationship between them and the feature sizes are as shown in Table 1.

Table 1: Design rules for MOS switch layouts

Rule (minimum)	Name	Size
Poly Width	d_1	2λ
Diffusion Width	d_2	3λ
Contact Opening	$d_3 \times d_3$	$2\lambda \times 2\lambda$
Contact-Poly Spacing	d_4	2λ
Diffusion Overlap of Contact	d_5	1.5λ
Contact-Contact Spacing	d_6	2λ
Poly-Poly Spacing	d_7	2λ

A. Alternating Bar Structure

The Alternating Bar structure is shown in Fig. 2a without metal. If the periphery of the overall cell is neglected, the structure is the parallel interconnection of the reference cell identified in the center of Fig. 2a and is expanded in Fig. 2b
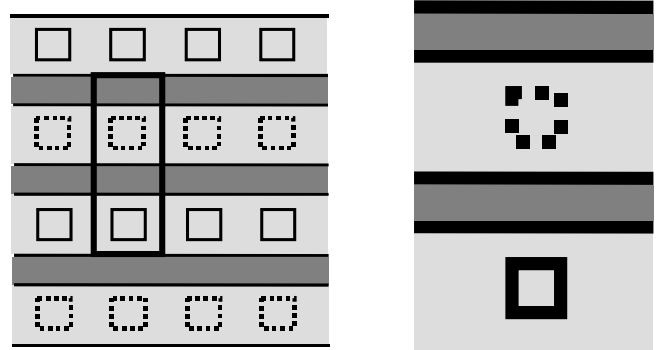

Fig. 2: (a) Alternating bar   (b) Reference cell

The area, $(W/L)_{eff}$ and $A_{ref,n}$ for this reference cell are given respectively by:

$$A_{ref} = 2(d_3 + d_6) \cdot (d_1 + d_3 + 2d_4) \tag{9}$$

$$\left(\frac{W}{L}\right)_{eff} = 2 \cdot \frac{d_3 + d_6}{d_1} \tag{10}$$

$$A_{ref,n} = d_1 \cdot (d_1 + d_3 + 2d_4) \tag{11}$$

B. Waffle Structure

The Waffle structure is shown in Fig. 3a without metal. If the periphery of the overall cell is neglected, the structure is the parallel interconnection of the reference cells identified in Fig. 3a. and expanded in Fig. 3b.
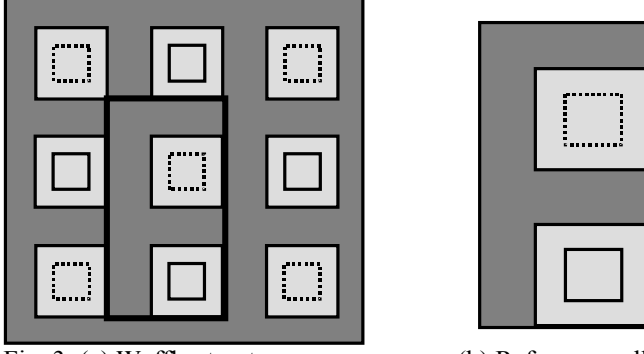
Fig. 3: (a) Waffle structure   (b) Reference cell

This structure is well known [2]-[5] and is similar to the structure used in vertical power MOSFETS [3]. For this reference cell, $(W/L)_{eff}$ is not readily attainable directly but from results presented in [1], the equivalent W/L ratio of the reciprocal transistor can be obtained and by taking the reciprocal of this, the W/L ratio of the desired transistor is found. The effective area and an estimate of $(W/L)_{eff}$ for this reference cell are given respectively by:

$$A_{ref} = 2 \cdot \left(d_1 + d_3 + 2d_4\right)^2 \tag{12}$$

$$\left(\frac{W}{L}\right)_{eff} = 2 \cdot \frac{2(d_3 + 2d_4) + 0.55d_1}{d_1} \tag{13}$$

$$A_{ref,n} = \frac{d_1 \cdot \left(d_1 + d_3 + 2d_4\right)^2}{2(d_3 + 2d_4) + 0.55d_1} \tag{14}$$

In this derivation and what follows, it was assumed that a 90° bend in a channel contributes 0.55 W/L units to the overall W/L.

C. Serpentine Structure

The Serpentine structure is shown in Fig. 4a without metal. If the periphery of the overall cell is neglected, the structure is the parallel interconnection of the reference cells identified in the center of Fig. 4a. and expanded in Fig. 4b. The area, the estimate of $(W/L)_{eff}$ and $A_{ref,n}$ for the reference cell in Fig. 4b are given respectively by:

$$A_{ref} = 2 \cdot \left(d_1 + d_2\right) \cdot \left((x+3) \cdot d_1 + d_3 + 2d_4\right) \tag{15}$$

$$\left(\frac{W}{L}\right)_{eff} = 2 \cdot \frac{(2.1 \cdot d_1 + d_2 + x \cdot d_1)}{d_1} \tag{16}$$

$$A_{ref,n} = \frac{d_1 \cdot \left(d_1 + d_2\right) \cdot \left((x+3)d_1 + d_3 + 2d_4\right)}{2.1 \cdot d_1 + d_2 + x \cdot d_1} \tag{17}$$

For $x = 0$, (17) reduces to

$$A_{ref,n}\big|_{x=0} = \frac{d_1 \cdot \left(d_1 + d_2\right) \cdot \left(3d_1 + d_3 + 2d_4\right)}{2.1 \cdot d_1 + d_2} \tag{18}$$
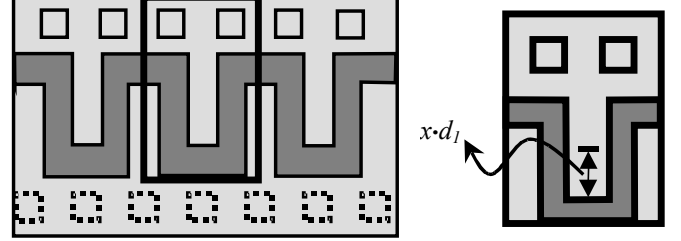

Fig. 4: (a) Serpentine Structure   (b) Reference cell

The deep Serpentine structure is obtained by increasing the depth of the fingers by selecting x in Fig. 4b to be 2. With this change, we obtain from (17)

$$A_{ref,n}\big|_{x=2} = \frac{d_1 \cdot \left(d_1 + d_2\right) \cdot \left(5d_1 + d_3 + 2d_4\right)}{4.1 \cdot d_1 + d_2} \tag{19}$$

The infinitely deep Serpentine structure, obtained by making the fingers arbitrarily long (i.e., letting x approach infinity in (17)), is characterized by

$$\lim_{x \to \infty} A_{ref,n} = d_1 \cdot \left(d_1 + d_2\right) \tag{20}$$

D. Star Zag

The Star Zag is shown in Fig. 5a and the expanded reference cell for this structure is shown in Fig. 5b.
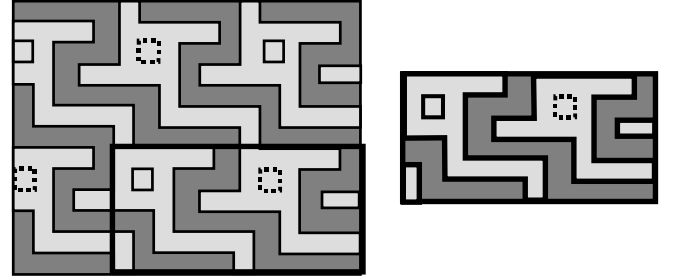

Fig. 5: (a) Star Zag structure   (b) Reference cell

Following the same analysis approach as was used for the Serpentine structure, it can be shown that

$$A_{ref} = 2 \cdot \left(4d_1 + 2d_2\right) \cdot \left(3d_1 + 3d_2\right) \tag{21}$$

$$\left(\frac{W}{L}\right)_{eff} = \frac{16.6d_1 + 10d_2}{d_1} \tag{22}$$

$$A_{ref,n} = \frac{d_1 \cdot \left(4d_1 + 2d_2\right) \cdot \left(3d_1 + 3d_2\right)}{8.3d_1 + 5d_2} \tag{23}$$

E. Fingered-Waffle

The Fingered-Waffle is shown in Fig. 6a and the reference cell for this structure is shown in Fig. 6b. The distance x shown in the reference cell is a variable and can take on any non-negative value.
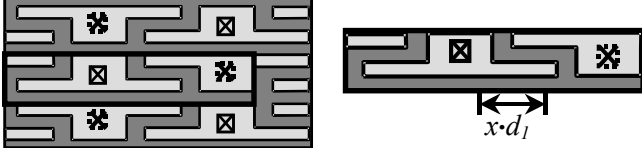
Fig. 6: (a) Fingered-Waffle   (b) Reference cell

Using the same techniques as earlier, this structure is characterized by the equations (for $x \geq 1$):

$$A_{ref} = 2 \cdot \left((1+x)d_1 + d_3 + 2d_4\right) \cdot \left(2d_1 + 2d_2\right) \quad (24)$$

$$\left(\frac{W}{L}\right)_{eff} = \frac{2 \cdot (2x-1)d_1 + 2d_2 + d_3 + 2d_4 + 3 \cdot 0.55d_1}{d_1} \quad (25)$$

$$A_{ref,n} = \frac{d_1 \cdot \left((1+x)d_1 + d_3 + 2d_4\right) \cdot \left(2d_1 + 2d_2\right)}{(2x-1)d_1 + 2d_2 + d_3 + 2d_4 + 3 \cdot 0.55 \cdot d_1} \quad (26)$$

IV. PERFORMANCE COMPARISON

A quantitative comparison is necessary to determine how much benefit is achievable from utilizing the more complicated layout structures. For large area resistors, the area associated with the periphery of the resistor is small compared with the area where geometric periodicity is achieved. The comparisons in this section will thus be restricted to comparing the performance of the reference cells. The alternating bar structure of Fig. 2 will serve as a reference and area savings of all other structures will be compared with that of the alternating bar structure. The relative area requirements are dependent upon the specific design rules for a given process with some variations from vendor to vendor in the design rules listed in Table 1.

Table 3 shows the comparison in performance for several different design rule scenarios (defined in Table 2). Considering the λ-based MOSIS scenario, it is seen that a reduction of 38.9% in area is achievable with the Waffle structure, 17% with the Star Zag, and nearly a 35% reduction with the Fingered-Waffle structure. For a current TSMC 0.35μ process, the savings become 40%, 29%, and 43% respectively. These substantial reductions in area are achieved while still maintaining a large number of via contacts and a small source resistance. The area savings for a modified set of λ-based design rules are also shown in Table 3. As can be seen, even more area savings are possible with the modified λ-based design rules.

Table 2: Different layout scenarios

		MOSIS	Modified	TSMC
d_1		2	2	1.7
d_2		3	2	2.1
d_3		2	2	2.1
d_4		2	2	1.7
d_5		1.5	1.5	1.0
d_6		2	2	2.1

Table 3: Area Comparison of Different Layout Structures

		MOSIS	Modified	TSMC
1.Alt. Bars		16.0	16.0	12.5
2. Waffle		9.8	9.8	7.5
	%incr	-38.9	-38.9	-39.7
3.Serpentine				
Normal		16.7	15.5	12.3
	%incr	4.2	-3.2	-1.2
Deep		14.3	12.5	10.2
	%incr	-10.7	-21.6	-18.4
Infinite		10.0	8.0	6.6
	%incr	-37.5	-50.0	-47.1
4. Star Zag		13.3	10.8	8.9
	%incr	-16.9	-32.3	-29.0
5. Fingered Waffle				
$x = 0$		9.8	9.8	7.5
	%incr	-38.9	-38.9	-39.7
$x = 2$		11.3	9.9	7.9
	%incr	-29.6	-37.8	-36.4
$x = 4$		10.9	9.4	7.6
	%incr	-31.7	-41.4	-39.3
$x = 10$		10.5	8.7	7.1
	%incr	-34.3	-45.4	-42.8

V. CONCLUSIONS

When designing low-resistance MOS switches, substantial reduction in area is achievable by using Waffle structures or modified Waffle structures. A reduction in area of over 40% was demonstrated for a typical process. Although these structures are geometrically intricate, closed-form design equations have been presented which will facilitate the utilization of these structures.

REFERENCES

[1]   P. Grignoux and R. L. Geiger, "Modeling of MOS transistors with nonrectangular-gate geometries," *IEEE Trans. on Electron Devices*, Vol 29, pp.1261-1269, August 1982.

[2]   K. Laker and W. Sansen, *Design of Analog Integrated Circuits and Systems*. New York, NY: McGraw Hill, 1994

[3]   D.A. Grant and J.G. Gowar, *Power MOSFETS Theory and Applications*. New York, NY: Wiley, 1989.

[4]   S. R. Vemuru, "Layout comparison of MOSFETs with large W/L ratios," *Electron Letters*, Vol. 28, pp.2327-2329, December 1992.

[5]   J. Bastos, M. Steyaert, B. Graindourze, W. Sansen, "Matching of MOS transistors with different layout styles," *Proc. IEEE Int. Conference on Microelectronic Test Structures*, vol. 9, pp17-18, 1996.