Cascode Current Mirrors with Low Input, Output and Supply Voltage Requirements

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***Abstract*--Modified wide-swing cascode current mirrors are introduced that achieve low input and output voltage drops. The new structures can be used in low-voltage environments and provide even higher output impedance than regular cascoded current mirrors. With dynamic biasing, high current accuracy and high output impedance can be maintained over a large operating current range.**

I. INTRODUCTION

The current mirror is one of the main building blocks of analog and mixed-signal integrated circuits. A host of current mirrors with high accuracy and high output impedance have been introduced. The cascode current mirror, the Wilson current mirror and the regulated cascode current mirror [1] are widely used. However, they are not suitable for low-voltage applications due to their limited signal swing. The wide-swing cascode current mirror was proposed [2] to enhance the output voltage swing. It can provide a large output swing while maintaining cascode-type precision and output impedance. However, the voltage drop at the input terminal of this current mirror is larger than V_t+V_{EB} (V_t is the threshold voltage of a transistor and V_{EB} is the minimum drain-source voltage required for transistors to maintain operation in the saturation region), which is unacceptably large for use in some low-voltage circuits. Low input voltage drop is particularly important in current sensing circuits [6].

Four new mirror structures are proposed that not only maintain the advantages of wide-swing at the output, but also a low input voltage drop and the capability of operating in low voltage environments. Dynamic biasing techniques [3]-[5] are applied to keep the cascoded transistors always operating in the saturation region so that the high precision and high output impedance can be maintained over a large operating range.

II. CIRCUIT DESCRIPTION

Several recently reported techniques and topologies can be used to reduce the input and supply voltage requirements of current mirrors. However, some of them have special fabrication requirements such being bulk driven [7], some can only been used in switched circuits [8], and some utilize feed-back amplifiers which limit the bandwidth of the current mirrors and may cause stability problems [9][10].

The simplest method of establishing a low voltage input characteristic that results in low distortion and wide bandwidth is to use a DC level-shifter as shown in the simple mirror structure of Fig.1. To keep both transistors in the saturation region and minimize the input-voltage drop of the current mirror, the voltage V_s should equal the threshold voltage of M1.

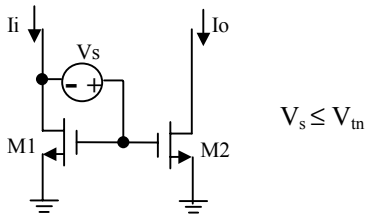

Fig.1 Conceptual schematic of DC level-shifter

Two level shifters are shown in Fig.2 (a) [6] and (b). In the circuit of Fig.2 (a), the voltage Vs is the difference of two V_{EB} making it difficult to accurately relate this to the V_t of M1. The circuit also has a rather high supply voltage requirement since it can be shown that $V_{dd} \ge V_{tn}+|V_{tp}|+3V_{EB}$ to maintain saturation region operation. The mirror of Fig.2 (b), believed to be new, also requires matching of V_{EB} to V_t but offers potential for operation at reduced supply levels of $|V_{tp}|+3V_{EB}$. Biasing schemes to precisely match Vs to V_{tn} for this circuit will be discussed elsewhere.

The level-shifter in Fig.3 [11] is larger than $V_{tn,}$ hence the two transistors M1 and M2 (assuming they are matched) are always operating in the triode region and

$$V_{ds1} = V_{ds_2} \approx V_{EB_2}(1-\sqrt{1-k}) \qquad (1)$$

where $k = \dfrac{(W/L)_{s2}}{(W/L)_{s2}+(W/L)_2} \le 1$.

Transistor M3 is added to form a negative feedback so that a cascode-type output impedance is achieved, which is approximately given by

$$r_{out} \approx k g_{m_3} r_{o_3} r_{o_{s1}} \qquad (2)$$

The advantage of M1 and M2 operating in triode region is that the input and output voltage requirements can be very low. The circuit also operates at a very low supply voltage of $V_{tn} + 2V_{EB}$. The disadvantages are: first, the output impedance of the current mirror is limited since r_{os2} is not large and since k<1; second, the current mirror accuracy is very sensitive to the mismatch between the drain-source voltages of M1 and M2, which, for example, may results from the mismatch between transistor Ms1 and Ms2. Even with good transistor matching, since the drain voltage of Ms1

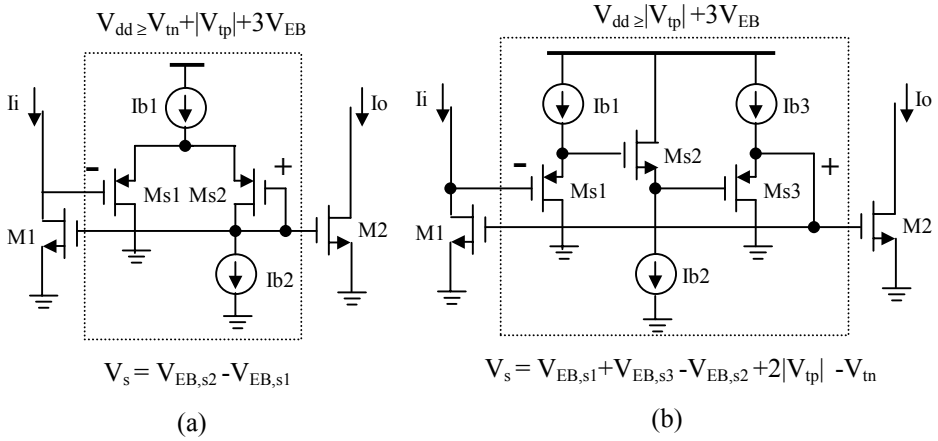

Fig.2 Level-shifters which require matching between NMOS and PMOS

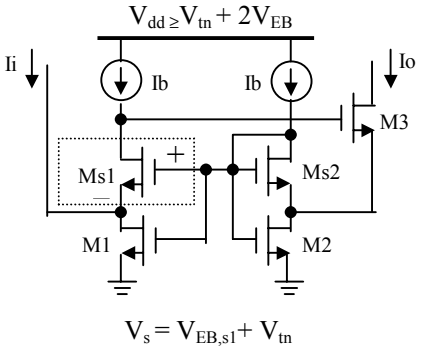

Fig.3 Triode-region CM (Triode CM)[11]

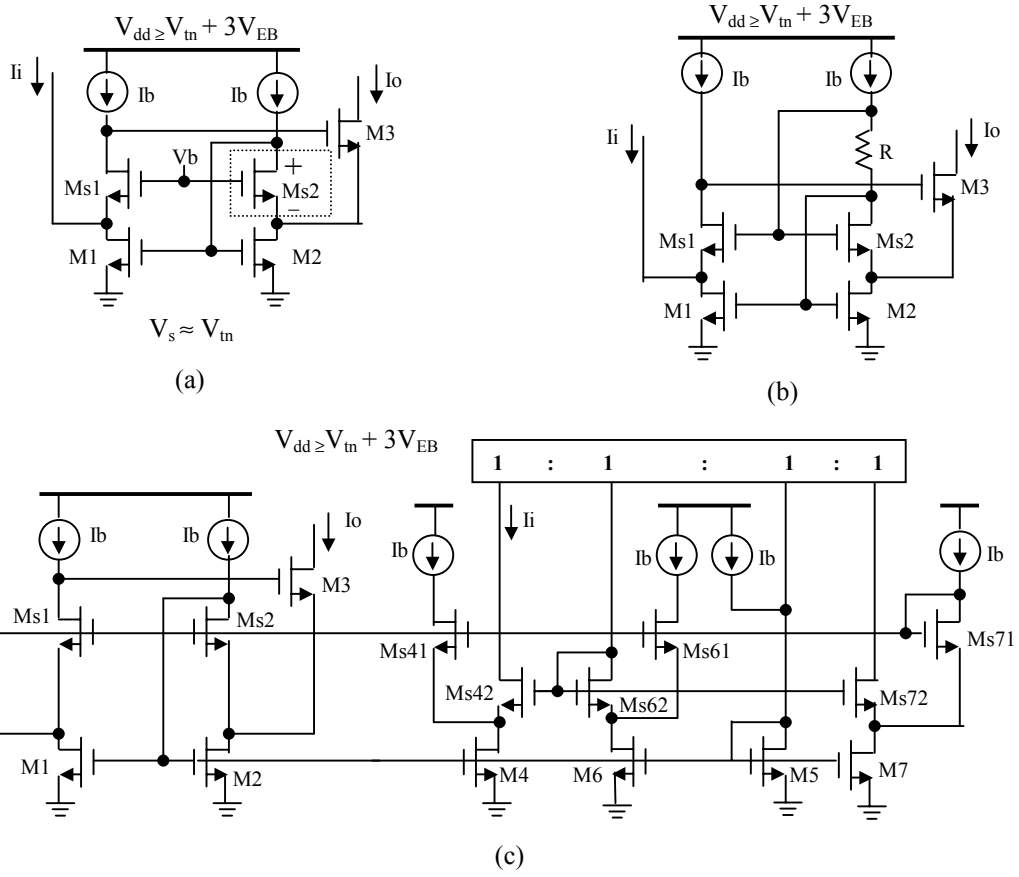

Fig.4 Proposed saturation-region current mirrors (Sat. CM) with (a) fixed bias (b) self-biasing and (c) dynamic biasing

is always higher than that of Ms2, the drain-source voltage of M1 is a little higher than that of M2, hence the output current is always lower than the input current.

These disadvantages can be reduced if the structure in Fig.4 (a) is used. With an accurate bias voltage V_b, transistor M1 and M2 can both work in the saturation region and their drain-source voltages can be set equal to V_{EB}. Transistor M3 is added to enhance the output impedance, which in this case is approximately given by

$$r_{out} \approx (g_{m_{s1}} r_{o_1}) g_{m_3} r_{o_3} r_{o_{s1}} \qquad (3)$$

Note that r_{out} in (3) is higher than that in (2). Since M1 and M2 are in saturation region, the accuracy of this current mirror is not so sensitive to the mismatch between the drain-source voltages of M1 and M2. The current offset due to the

drain voltage difference of M_{s1} and M_{s2} is also reduced. The input and output voltage requirements and supply voltage requirements are attractive but a little higher than those of the circuit in Fig.3.

As in the "wide-swing cascode" current mirror[2], to maintain the high accuracy and high output impedance over a large operating current range, the bias voltage $V_{b,}$, must be able to dynamically track the changing of $V_{gs1,2}$ so that $V_{ds1,2}$ is always equal to $V_{EB1,2}$ ($V_{EB1,2}$=$V_{gs1,2}$-V_{tn}). This can be achieved by simply adding a resistor as shown in Fig.4 (b), which is the so-called "self-biased" current mirror [12]. The resistance R is chosen so that

$$I_b R = V_{EB_{s2}} = \sqrt{\frac{2I_b}{\mu_n C_{ox}(W/L)_{s2}}} \qquad (4)$$

However, this requires matching between the resistor and the transistors. An alternative is to simulate the resistor with a triode-region transistor[3]. However, a PMOS transistor has to be used if the power supply voltage is less than 1.5V. In this case, matching between this triode-region PMOS transistor and the NMOS transistors are required. The resistance of the triode-region PMOS transistor can not be fixed since its drain and source voltages always change with the input current.

Many circuits have been proposed for the biasing of the cascode transistors [3]-[5][12], but few of them can provide accurate dynamic biasing in low-voltage environment. In our cases, this becomes even harder because the currents flowing through the cascode transistor M_{s1} and M_{s2} (equal to I_b) are not the same as the currents flowing through M1 and M2 (equal to I_b+Ii). An accurate but fixed biasing was established in [3] and this circuit can also operate with a low supply voltage. Dynamic biasing can be achieved by combining this bias circuit with the replicas of the output current. The final bias circuit is shown in the right part of Fig.4 (c), where the cascode transistors (denoted as M_{sxx}) can be classified into two parts: Those conveying bias current I_b are denoted as $M_{sx1.}$ They have the same size, share the same bias voltage as M_{s1} and M_{s2}, and hence have the same gate-source voltages; Those conveying the replica of the output current are denoted as $M_{sx2.}$ They also have a common size, common bias and common gate-source voltages. The currents flowing through transistor M4-M7 as well as M1 and M2 are all equal to I_b+Ii and their $V_{ds,}$ except V_{ds5}, are also equal. The optimum condition V_{ds1} =V_{ds2} =V_{ds4}=V_{EB} can be achieved if the transistors are sized as follows:

$$\begin{aligned} &L1=L2=L4=L5=L6=L7 \\ &W1=W2=W4=W \\ &W6=W7=W' \end{aligned} \qquad (5)$$

and W5 satisfies the relationship

$$\frac{W5}{W'} = 1-(1-\sqrt{\frac{W5}{W}})^2 \qquad (6)$$

subject to the constraint W5<W'.

W' is chosen larger than W5 so that transistor M6 and M7 are always in the triode region. For example, if W5=W/4, then W'=W/3.

III. Simulation results

Hspice simulations of the three current mirrors using the HP0.35u Level49 Model are shown in Fig.5. The three current mirrors are the Triode CM (Fig.3), the Sat. CM with self-biasing (Fig.4(b)) and the Sat. CM with dynamic biasing (Fig.4(c)). The transistors are sized as follows: all NMOS transistors except M5-M7 in Fig.4(c) which can be determined according to (6) had W/L=40/1; all PMOS transistors which implement all current sources and replicas had W/L=80/2. The resistance in the Triode CM is chosen according to (5) and the bias current I_b was set to 5uA. Except as noted below, the supply voltage was 1.5V.

Fig.5 (a) shows the gain error and linearity of the three current mirrors without considering transistor mismatch. They all achieve high accuracy over a large input current range. As expected, the output currents are always a little lower than the input currents. The error for the two saturated current mirrors are less than 0.1% for 20uA≤I_i≤220uA, while the error for the Triode CM is limited to within 0.15%~0.35%.

Fig.5 (b) shows over the same input range how the input voltages vary with the input current. As expected, the input voltage drop of the Triode CM is lower than that of the Sat. CMs. The input impedance of all three are similar.

The output impedance of the three current mirrors when I_i=50uA are shown in Fig.5 (c). To keep the transistors in the saturation region, the Sat. CMs require higher output voltages (about 0.3V) than the Triode CM(about 0.2V). However, with increases of the output voltage, the output impedance of the Sat. CMs are 3 times higher than that of the Triode CM.

Fig.5 (d) shows that the performance of the three current mirrors at lower supply voltages. In those simulations the input current was fixed at 50uA. From the simulations, it can be seen that the mirrors can achieve high accuracy with Vdd down to 1.1V.

IV. Conclusions

New current mirrors with low input, output and supply voltage requirements have been introduced. The proposed saturation-region current mirrors with dynamic biasing can achieve higher accuracy and higher output impedance than the triode-region current mirror with the penalty of a little higher input and output voltage requirements. They also maintain low distortion and high output impedance over a

large input current range with the supply voltage as low as 1.1V.

ACKNOWLEDGEMENT

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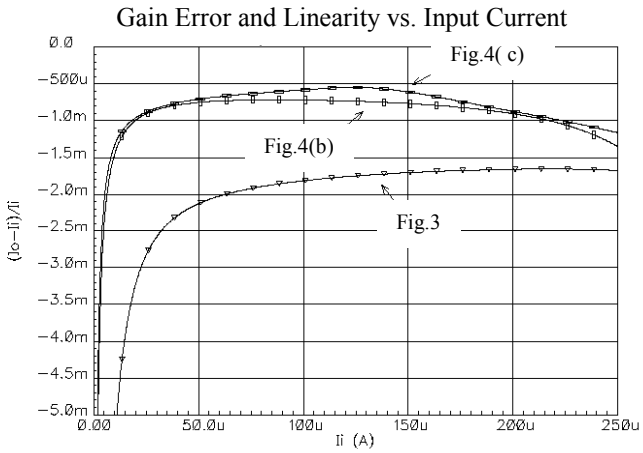

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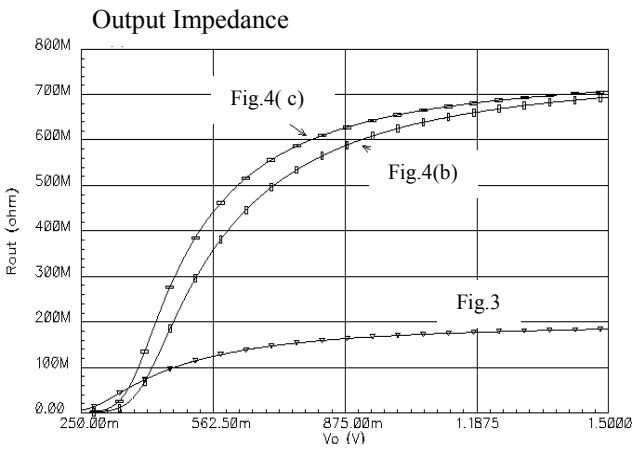

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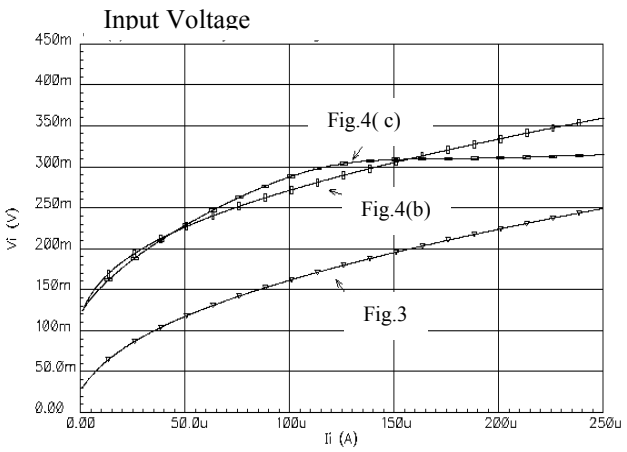

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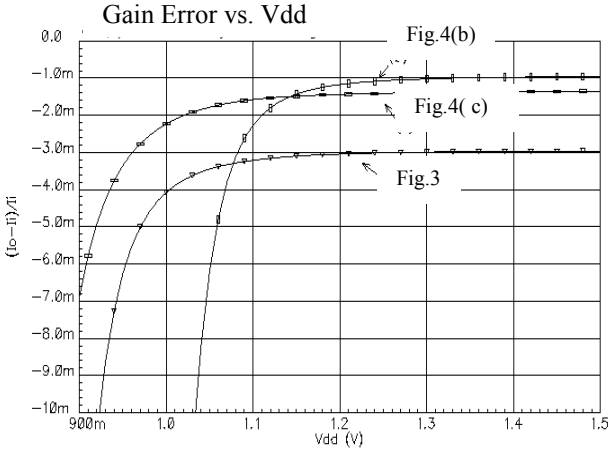

(d)

Fig.5 Hspice simulation results for current mirrors of Fig.3, Fig.4 (b) and (c)